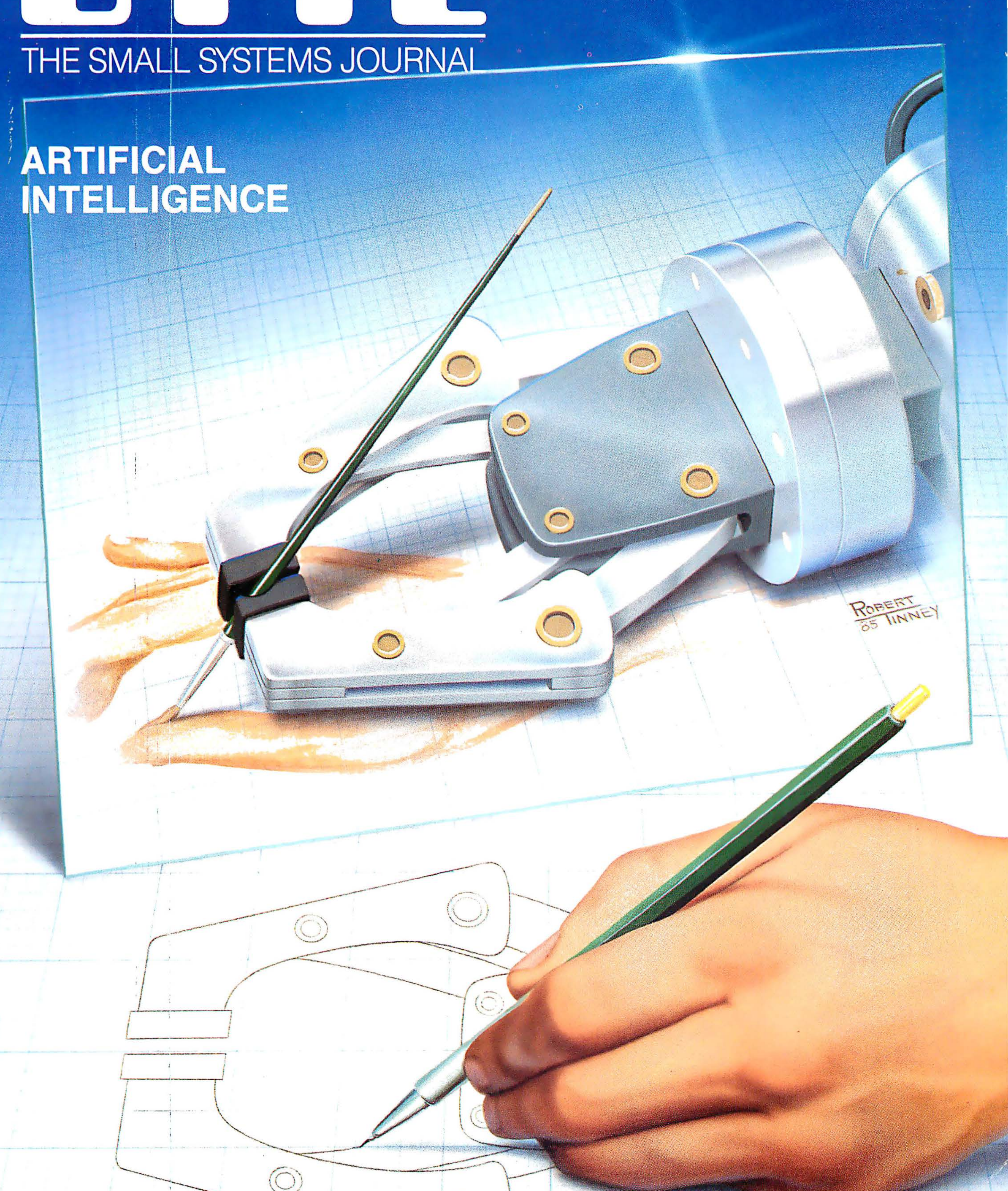
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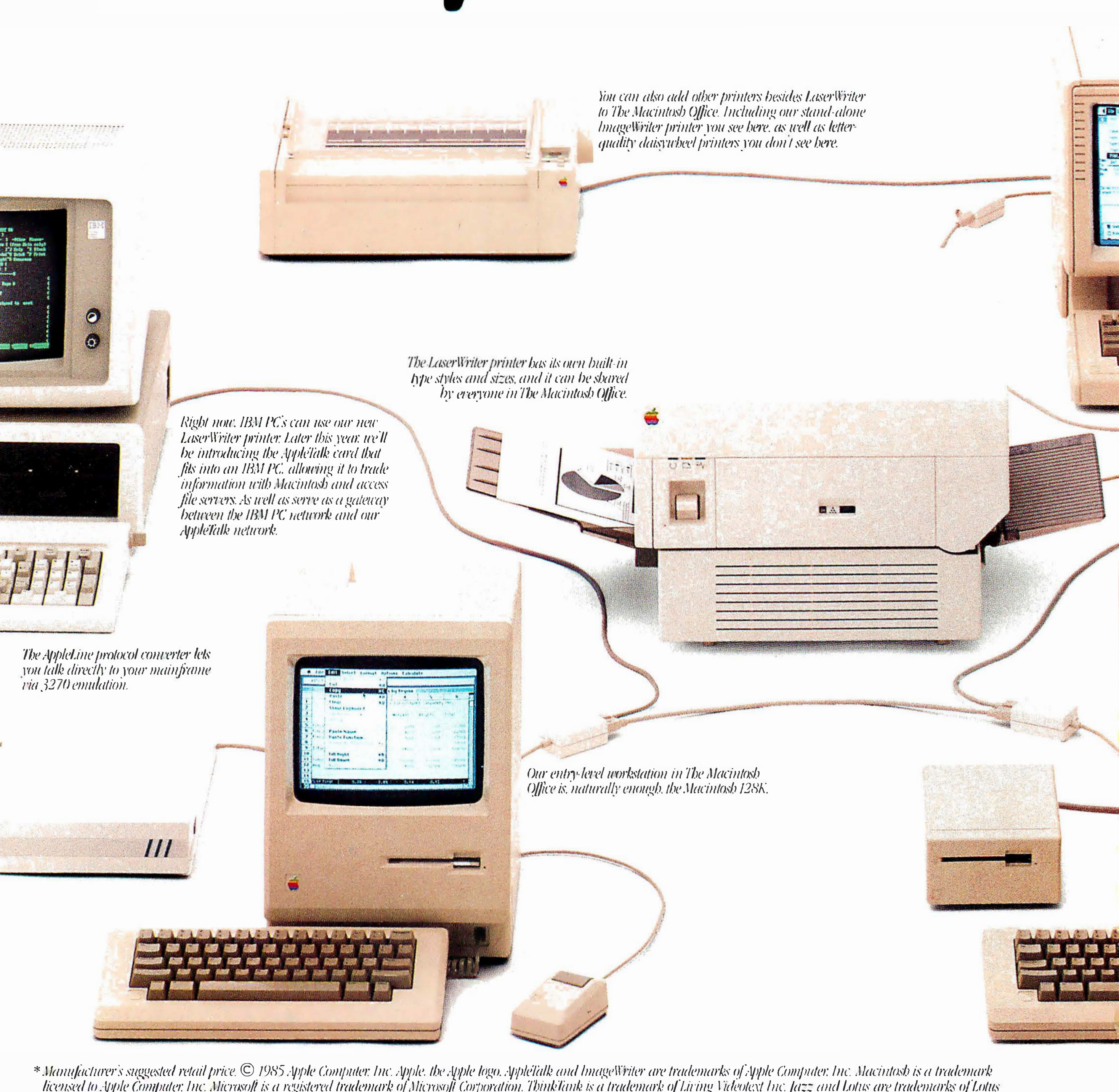
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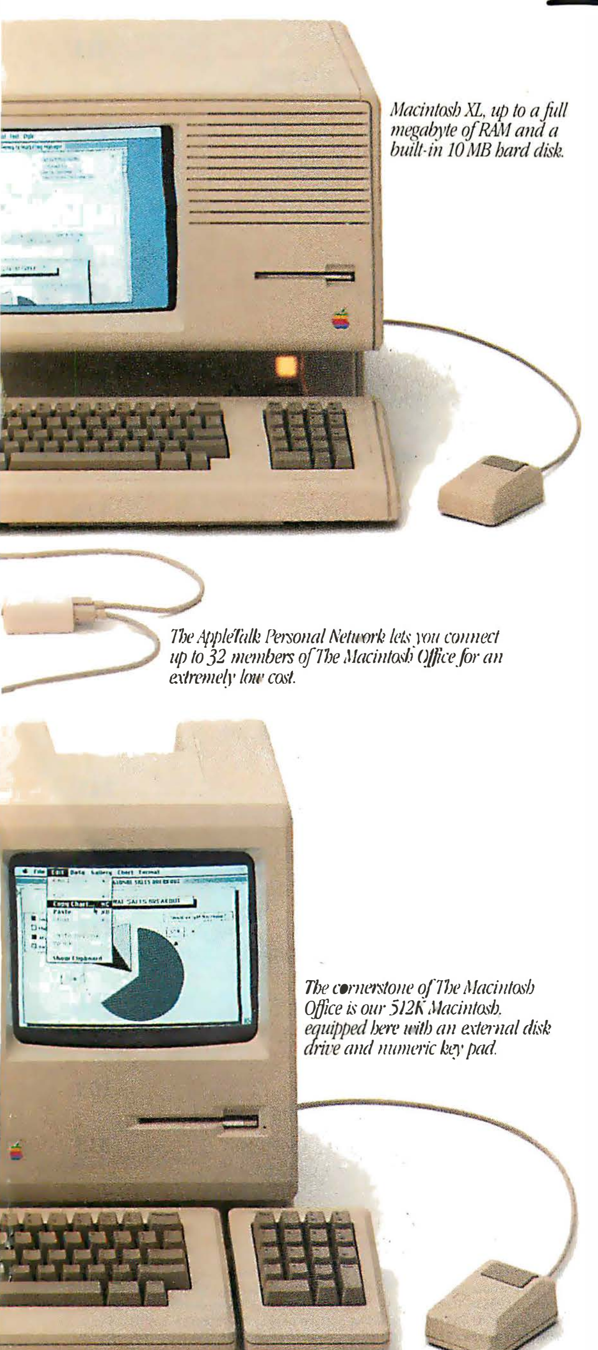


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Macintosh Office.
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The cornerstone of The Macintosh Office is our 512K Macintosh, equipped here with an external disk drive and numeric key pad.

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But the kind of people who already make up most of your office.

Managers and professionals. People who spend most of their time selling products, services or, most importantly, ideas.

Because, unlike traditional office computer solutions, we didn't design The Macintosh™ Office around a mainframe. We designed it around an idea.

The idea that people, not mainframes, are the most important information centers in an office. And that most things in business are really accomplished by teams of 5 to 25 people who need to share information with each other. What we call the *workgroup*.

That's why we put Macintosh at the heart of The Macintosh Office. Its powerful, 32-bit technology reduces the time it takes to become productive with a computer from well over a work week, to just under a lunch hour.

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Third party developers are also working on The Macintosh Office. Next month,



ArchitecturalDesign | Issue #12 | Winter

Arch News

The Society of Architects
1400 New York Avenue
Washington DC 20018

Value is what the 1985 SOA National Seminar in Atlanta is about-- and it's what you'll find in greater quantity and greater quality than ever before at the convention's 1985 SOA Exhibit of New Technology and Products.

The biggest convention exhibit in SOA history will present you with a demanding challenge: Find a way to decide which products, services and technologies you want to learn more about:

- Computer Technology
- Software, Hardware
- Contract Furniture
- Interiors, Exteriors
- Practice Systems

You'll find it all--plus a convention schedule that lets you see it all--at the 1985 SOA Display of New Products and Design.

The Art of the Dormer, a retrospective look at 19th Century dormers. At the Seattle Architectural Gallery through the 19th of the month.

This page was created with Hayden's Da Vinci, Aldus' PageMaker and the Apple LaserWriter.

"Architecture... has its own validity. It needs no reference to any other discipline to make it viable or to justify its value."
--Philip Johnson

Chr. Wren

Conferences, seminars, workshops:

May 21-25 25th Annual Meeting. The Society of Architects, 1400 New York Avenue, Wash. DC 20006.

June 10 Deadline, call for 500-word abstracts, "Designing and Managing Commercial Buildings: An Intensive Workshop."

June 25 American International Solar Conference and Exhibition. Thomas Convention Center, Dallas, TX.

Call (206) 555-1919 for details and register early for the 1985 SOA National Seminar, March 9-12, in Atlanta.

"Architecture aims at eternity; and therefore is the only thing incapable of modes of fashions in its principles."
--Christopher Wren

Master Architect

The man featured in this month's issue may well be one of Vancouver's best kept secrets. You may not know his face, but if you live in Vancouver you know his work - that is, if you've ever visited Simon Fraser University, The Museum of Anthropology, Robson Square/The Law Courts, or any of a number of other governmental, commercial and residential buildings. The man is Arthur Erickson, Architect, and he has called Vancouver home for most of his life.

While the layperson may not recognize his face or name, during a remarkable and prolific career spanning more than 30 years, Arthur Erickson has received dozens of honorary degrees and virtually every major professional and personal award. To list them all

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they'll be offering shared storage devices that let your workgroup share information. And they're writing a whole new generation of business software to go along with the 350 programs Macintosh already runs. Including Microsoft® Word, ThinkTank™ 512 and the new Jazz™ from Lotus.®

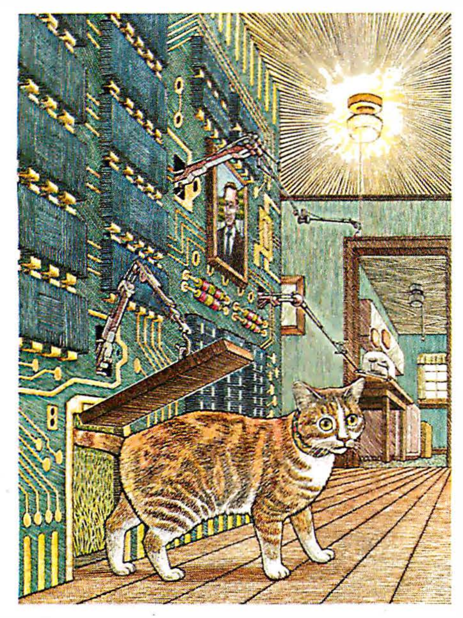
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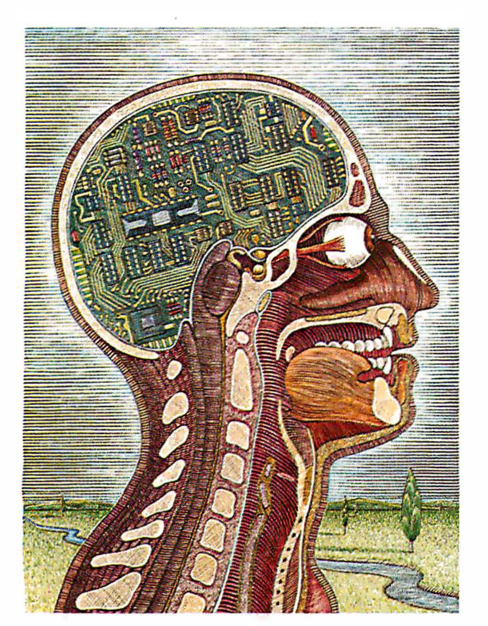
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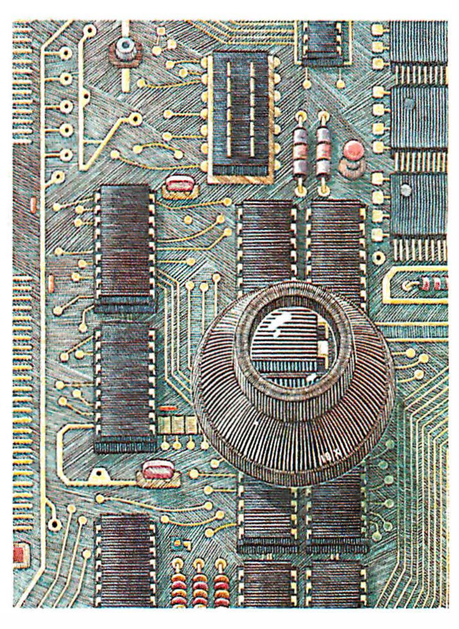
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BYTE April

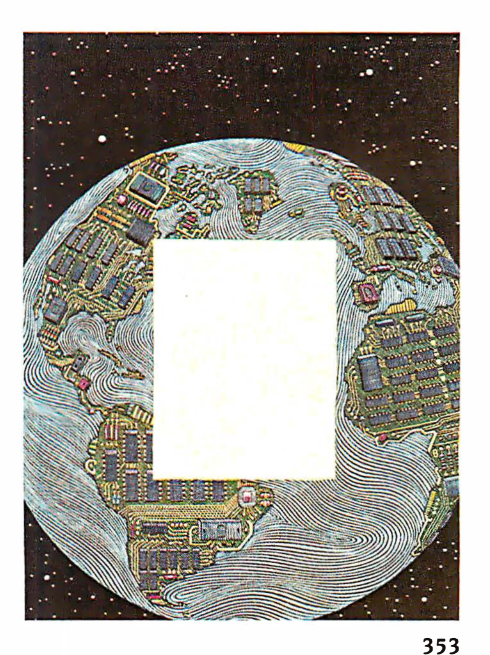
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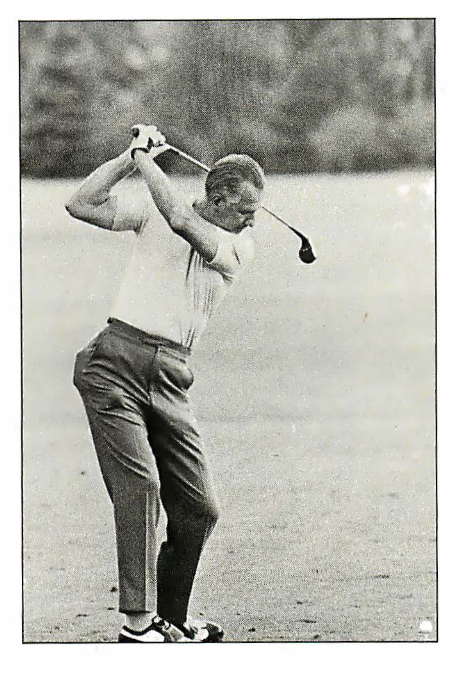
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GOLFERS AND HACKERS

It must no longer go unremarked that many of the criminals who threaten the foundations of our society are golfers. Golfers persist in attacking our personal, financial, and military security. Many golfers, like the famous one caught in the act in photo 1 (Spiro Agnew), have been involved in extortion, bribery, or other forms of corruption.

Some golfers have been known to hit out of bounds as a pretext for trespassing in residential communities. Such forays easily turn into incidents of voyeurism and burglary.

VIOLENCE

Other golfers use the harmless-looking little white balls to inflict injuries on bystanders, propelling the dangerous projectiles at speeds in excess of 120 miles per hour. The danger of head injuries is obvious. Golf's careless disregard for the safety of other people hardens our children to violence. The idea that shouting a single, obscure word makes it all right to bop some innocent person on the head with a hard projectile has brought our society to the brink of savagery. Last week in a major American city a thug shouted "Fore!" and then mugged a grandmother as if it were the most natural thing in the world.

GOLFING ARCADES

Perhaps the most distasteful thing about golfers is their use in recent years of golfing arcades. These so-called "driving ranges" allow addicts to rent baskets containing dozens or even hundreds of golf balls so that the addicts can bombard surrounding land at rates previously unthinkable. Although the fences sometimes used around these golfing dens may protect people outside from physical injury, the fences do nothing to stop the spread of the moral rot associated with the trancelike concentration of the golfer on the little white ball. That little ball means more to the golf addict than honor, mother, or country.

The money squandered at golfing arcades, golf courses, and pro shops could buy a personal computer for every child in America or pay off the national debt, depending on national priorities.

NATIONAL SECURITY IMPLICATIONS

The parliament of King James II of 1457 banned golf because its addicts neglected to practice the use of the crossbow, then the chief means of national defense. Today in this country, golfers neglect the most advanced weapons systems in history. This neglect could nullify all the technical progress recently seen in weapons research. What good is an orbital-beam weapon if the operator is busy selecting a club?

It doesn't take a genius to see that avoidance of golf is a cornerstone of Soviet military strategy. This gives the Soviets a tremendous advantage in daytime warfare. If the Soviets launch an attack at 3 p.m. EST on a weekday in June, approximately 20 percent of American manpower will be uselessly deployed in fairways, sandtraps, and rough. Even those in bunkers will be in the wrong kind of bunkers. At 3 p.m. on a weekend, as much as 50 percent of our manpower might be trying to avoid bogies rather than to shoot them down.

CALL TO ACTION

Because of the threats that golfers pose to national security and our moral fiber, we are proposing that all golfers be arrested as soon as possible.

UNFAIR?

If the foregoing attack on golfers seems unfair (and, of course, the analogy is not perfect), it is little more so than the attack in the general press on hackers of another kind—computer hackers. Some national publications have used the term "hacker" incorrectly as a synonym for "criminal." Hackers are people who play with computers at a technical level because they enjoy doing so. There are many thousands of hackers in North America. A few hackers use their computer skills for pranks, and fewer still use their skills to commit crimes. But the chances are excellent that far more hackers are helping build defenses around databases than trying to penetrate them. If even one percent of hackers started trying to invade our databases, problems would be far more serious than those sensationalized in the general press.

It wasn't being a golfer that got Spiro Agnew into trouble. Just being a hacker won't get anyone into trouble, either. Hackers are as entitled to the presumption of innocence as golfers and other common special-interest groups. Hackers are also entitled to the continued correct use of the authentic, distinctive, and colorful name that they gave themselves.

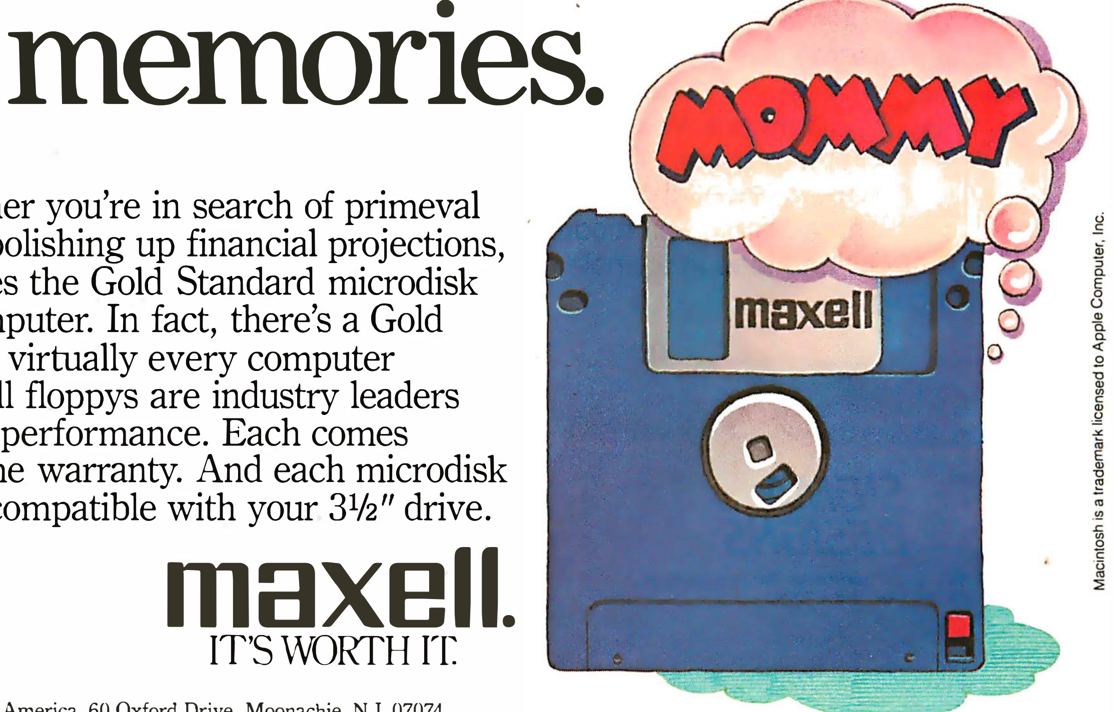
—Phil Lemmons, Editor in Chief

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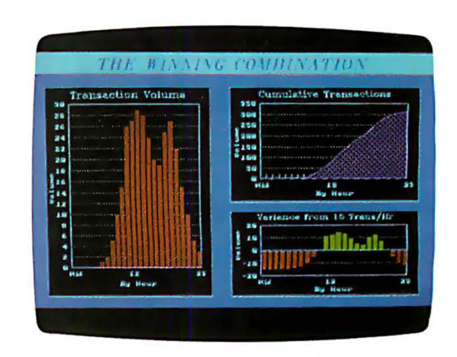
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COLOR 400

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See how impressive this state-of-the art image can be on your own PC system. Visit your local retailer today and ask about this new color graphics team. Princeton Graphic System's SR-12 and Sigma Designs' Color 400. An unmatched, brilliant combination.





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Staff-written highlights of late developments in the microcomputer industry.

Macintosh Users Get IBM PC Emulator

Dayna Communications, Salt Lake City, UT, has announced MacCharlie, a hardware-and-software system that allows Macintosh users to run IBM PC software. Two hardware components are included: one adds 10 function keys and an 18-key numeric keypad/cursor pad to the Macintosh keyboard; the other has one or two 5¼-inch disk drives, memory, an IBM-compatible ROM chip, and an 8088 processor, as well as serial and parallel ports and a bus-extender port for an optional expansion chassis. Also included is a Macintosh program that handles all keyboard and display processing—and it can still be used to access the Mac's desk accessories from within IBM PC applications. MacCharlie emulates all features of the IBM monochrome graphics card except for light-pen support.

The Macintosh can be set atop the matching MacCharlie unit, which adds four inches to the Macintosh's width and one inch to its height. The Macintosh keyboard fits into the keyboard extender; the numeric keypad can be used as a standard Macintosh numeric keypad when in Macintosh mode. The bus-extender port allows use of an optional expansion chassis so that IBM cards can be installed; with an additional cable, IBM's expansion chassis can be used. With one 5¼-inch disk drive and 256K bytes of memory, MacCharlie is $1195; with two drives and 640K, it's $1895.

New Mac Products Shown

Several companies unveiled new products for the Macintosh at the MacWorld Expo in San Francisco. While many new software titles were demonstrated, memory-expansion and hard-disk-drive exhibits drew much attention.

Micro Conversion, Arlington, TX, and Levco Enterprises, Del Mar, CA, both offer complete 512K-byte upgrades for $400, including installation, and also sell uninstalled kits. Levco also sells a $60 kit with all necessary parts except the 256K-byte chips.

In addition to already-announced hard-disk products, new drives from Paradise Systems Inc. and Micro-Design were shown in prototype form. Not surprisingly, most exhibitors used hard disks and 512K-byte Macs to demonstrate their software.

Hayden Software showed Ensemble, an integrated package for the 128K-byte Mac. Database, spreadsheet, graphics, and text-processing features are included in the $300 program, which was developed in France. A number of new database programs were also exhibited at the show.

Paragon Courseware, Del Mar, CA, offers two font sets: a $50 Scientific Typing font and a $100 Electronic Circuits font.

Micro Focus Inc. now offers MacCOBOL, a COBOL development system.

Microsoft Releases Its Own C Compiler

Microsoft has released Microsoft C version 3.0, which replaces the Lattice-developed C previously sold by Microsoft for the IBM PC. Microsoft's C compiler provides file-sharing and record-locking features for use in network environments; a separate Windows Toolkit will help C programmers develop applications to run under Microsoft Windows. Microsoft says that source and object code can be linked to run directly under MS-DOS or XENIX without modification. Microsoft C is $395.

New LCD Portables Use Backlit Display

Zenith Data Systems is expected to introduce a lap-top portable computer with a backlit liquid-crystal display (LCD). The 16-pound Z-175 will include one or two 5¼-inch disk drives, 256K bytes of RAM, and an 80C88 processor for less than $3000.

To counter the viewing angle and lighting problems caused by LCDs, Morrow Design also changed the 16-line by 80-character display on its Pivot computer, switching to backlit LCDs rather than relying on room light, despite the extra power consumed by the backlighting.

(continued)

Proteon Adds 80-megabit-per-second Network

Proteon, which markets the ProNET token-passing star/ring hybrid local-area network, now offers a faster network. While ProNET used a 10-megabit-per-second data rate, ProNET-80 transfers information at 80 megabits per second. Proteon expects it to be used in applications using multiple minicomputers and mainframes or in connecting graphics workstations with large file sizes. The network will be available for Unibus and Multibus systems for about $8000 per node.

Intel Will Sell CalTech's Hypercube Multiprocessor Computer

Intel has licensed the hypercube computer design from the California Institute of Technology and will sell a computer based on that multiprocessor architecture. The computer consists of a multiprocessor cube and a cube manager. The cube includes 32, 64, or 128 computational nodes, each of which includes an 80286 processor, an 80287 math coprocessor, and 512K bytes of memory. Each node in the cube can communicate with five adjacent nodes and with the cube manager through 10-megabit-per-second communications channels. The cube manager is an Intel 286/310 microcomputer with 2 megabytes of RAM and a 40-megabyte hard-disk drive. Intel claims a performance range from 2.5 to 10 million floating-point operations per second with an efficiency of 80 to 99 percent. Prices range from $150,000 to $520,000.

Torus Prepares to Launch LAN Software

Torus Systems Inc., Redwood City, CA, plans to introduce icon-based user-interface software for IBM PC network environments this month. The product will be based on Icon, the network software it says it has been selling since July in England for systems using 3Com's Ethernet network cards.

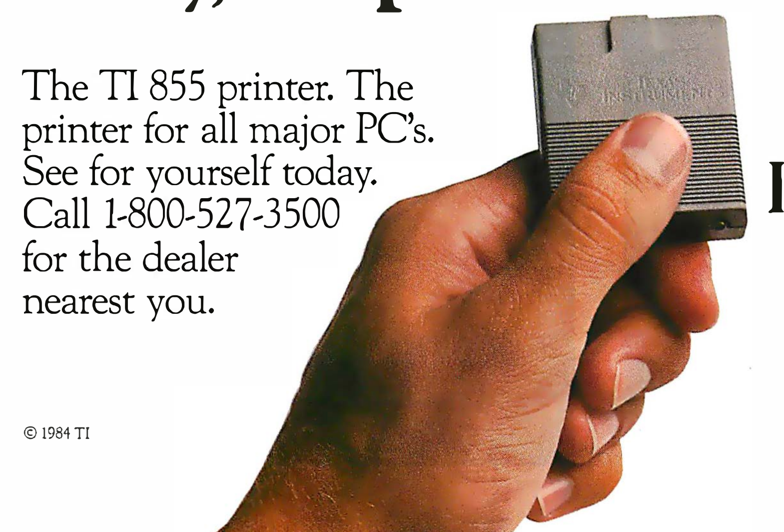
The program will include intranetwork electronic mail, telecommunications, file locking and sharing, and other network software features; users will also be able to run standard MS-DOS programs under the environment, either from local disks or from a file server.

NANOBYTES

While announcing the Macintosh Office in late January (see February BYTE, page 120), **Apple** also announced the Macintosh XL, which is simply the Lisa renamed. . . . **Software Publishing Corporation** has added XMODEM file-transfer and remote computer access features to its $140 pfs:Access program. . . . **Kensington Microware**, which advertised its Quick Cursor and Printer Buffer for Apple's Macintosh last year, has canceled development of those products. The company will continue to sell other "Maccessories." . . **Mostek**, **Toshiba**, **Hitachi**, and **AT&T's Bell Labs** presented papers on CMOS 1-megabit RAM chips at the International Solid State Circuits Conference (ISSCC) in February; **IBM**, **NEC**, **Mitsubishi**, **Toshiba**, and **Fujitsu** discussed NMOS 1-megabit RAMs. Image-sensor chips were discussed by **Mitsubishi** and **Sharp**, and engineers from **AT&T's Bell Labs** discussed the development of a 32-bit floating-point digital-signal-processing chip. . . . **Mother Jones' Son's Software**, Reno, NV, is selling MJ, a set of background utility programs. In addition to redefining the PC's keys, MJ expands the IBM's keyboard buffer from 16 to 1000 keys, permits the cursor speed to be changed, and includes a password protection option. MJ costs $30, or $70, including source code. . . . **Digital Equipment Corporation** acknowledged in February that it had stopped manufacturing the Rainbow personal computer but said it will continue to ship from inventory and plans to announce a new version later this year. . . . **Syntech**, Canoga Park, CA, has announced a MIDI (musical instrument digital interface) adapter card for IBM, Apple, and Commodore computers. For the Apple or Commodore, the card is $100; for the IBM PC, it's $195. . . . **The Library Corporation**, Washington, DC, is selling a complete CD ROM system for the IBM PC, including a disc with records for a million English-language books, for $2930. . . . **Corvus Systems Inc.**, San Jose, CA, has replaced its line of Omnidrive hard-disk drives with a single model that can be used with IBM PC; Apple II, III, and Macintosh; DEC Rainbow; and Zenith Z-100 computers. Corvus also dropped prices by about 30 percent. An 11-megabyte drive is now $1995. . . . **Hammer Computer Systems Inc.**, Larkspur, CA, announced E-Z-DOS-IT, a $200 program that allows up to eight MS-DOS programs to execute concurrently. . . . **Gold Hill Computers** has enhanced its Golden Common LISP interpreter and will also offer a GC LISP compiler in the summer. A large-memory-model version will also be available for the IBM PC AT.

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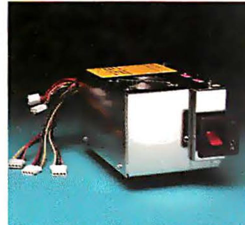




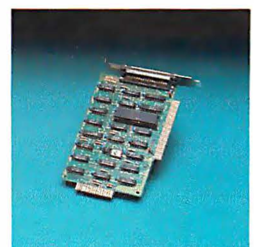
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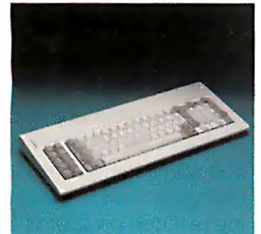
SUPER CONTROLLER
Controls up to 4 Floppy drives Comes W/Cables for 2 Drives



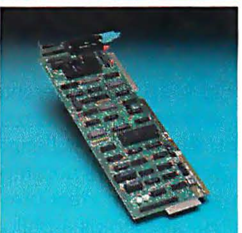
SUPERBOX
Fully BUS compatible
Adds 10 slots. 135 W Power supply for Hard Disk and Add-Ons
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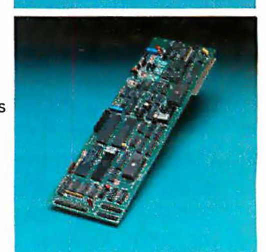
KEYBOARD
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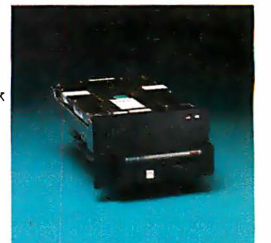
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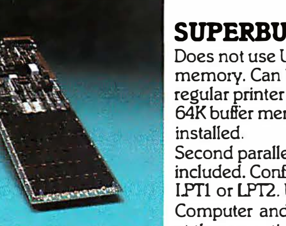
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Disk Controller and cable.
Clock/calendar Parallel, Serial and Game ports.
RAM Disk emulator.
Super Spooler software



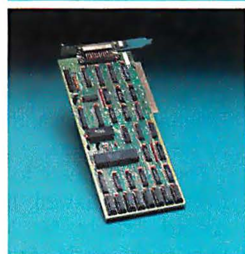
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Unlimited storage
Bootable from either fixed or removable hard disk



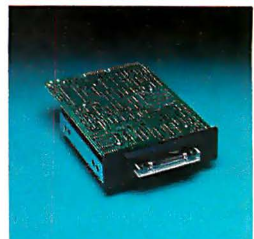
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RAM disk and print spooler software included



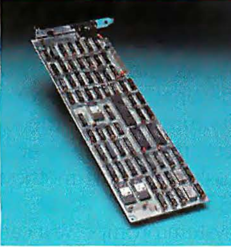
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Does not use User's memory. Can be used as regular printer port W/O 64K buffer memory installed.
Second parallel port included. Configurable as LPT1 or LPT2. Use Computer and print at the same time



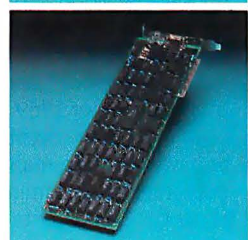
TAPE BACKUP
Backs up 10 Mb within 3 minutes
Uses regular floppy controller



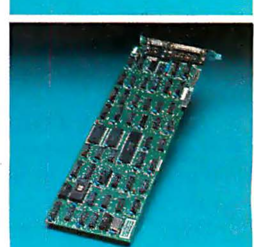
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SUPERCOLOR CARD
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16K display memory
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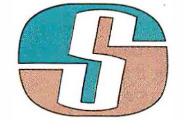
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Covering Advanced Systems

I have now been using a Fujitsu Micro 16s (8086 processor) for the past eight months, and I don't know how I got this far without some kind of micro. I am already planning for my next system, which will have either a 68020, a 16032, or a 32032 processor running UNIX.

Along with Jay Steinbrunn (Letters, August 1984, page 23), I too would like to see BYTE raise its sights and start to cover this future marketplace. Tell us what's happening out there so I can start putting money into my "purchase" account. I've seen a few inklings of this advanced micro technology at some of the shows, namely Saber Technology's use of the NS32032.

There are probably more of us out there that are interested in these advanced systems than you realize.

William H. Mestler
Tarzana, CA

Phil Lemmons replies:
We will keep an eye out for real 32-bit microcomputers at reasonable prices.

An Apple for BYTE

I want to compliment you on your special articles on the Apple computers (*The BYTE Guide to the Apple Personal Computers*, December 1984). The length of the articles showed that your company spent many hours choosing articles that would be enjoyed by the majority of readers. The articles were not only enjoyable, but they were also very informative. They showed an extreme amount of quality, which was the biggest impression I had after reading them. I commend your writers and company on a job well done.

Kevin Hoekman
Lakewood, CA

Where Credit Is Due

I have just read your December 1984 issue. I was impressed by "High-Speed Dial-up Modems" by Kim Maxwell (page 179). I found the article very informative and timely. Kim Maxwell's writing style is always very informative. He also manages to keep the reader interested throughout any articles he writes.

But I must challenge the description of Mr. Maxwell's accomplishments. Mr. Maxwell is the current president of Racal-Vadic. He also holds a philosophy degree from Stanford. The remainder of the description is not correct.

Racal-Vadic was founded in April 1969 by seven individuals: Ted Saunders, Bob Stires, Jay Tutt, Tom McShane, Jim Barrick, Larry Taylor, and Kim Maxwell. The company was then known as Vadic. The ideas and circuits used to start Vadic were Ted Saunders's.

The very first full-duplex 1200-bps modem was invented and designed by John A. C. Bingham in 1972 during his employment at Vadic. Bingham must be given credit where credit is due. Mr. Bingham's talents and contributions need to be recognized.

This is not meant to take anything away from Kim Maxwell. It is just to set the record straight. Mr. Maxwell's contributions to the world of data communications are numerous, too numerous to list. He has peers in this group, but very few.

An an engineer and investor at Vadic from November 1969 to November 1984, I saw most of the events during that period and was party to many. I also worked for both men and admire their talents and contributions to data communications.

Duane Marcroft
San Carlos, CA

WordStar's .BAK Extension

I read Vincent Alfieri's "WordStar as a Programming Tool" (November 1984, page 505) with some enjoyment. I have long used WordStar for both program development and correspondence, and I agree with Dr. Alfieri's verdict that it is a program hard to beat in power and versatility. Even after several years of using WordStar, including writing patches and modifications to the program itself, it still manages to surprise me with its power.

I know that the problem that Dr. Alfieri has experienced with limited disk space is frustrating; I used to have the same problem myself. While my ultimate solution was to move to 8-inch disks, there are more immediately applicable fixes. The problem stems from the fact that WordStar saves the old version of an edited file, changing the file extension to .BAK. Having rescued program files from otherwise hopeless oblivion by the use of this feature, I am quite willing to put up with its rather extravagant use of disk space.

It is an almost undocumented feature of WordStar that allows you to specify a disk drive to receive all work files and the final edited file other than the drive on which the original file resides. This can be done in either of two ways. From the Opening Menu, simply choose "D" or "N," as appropriate, and when asked for the name of the file to edit, reply with the filename, but follow it with a space and a drive designator. For example, to edit the file TEST.DOC, which resides on drive B:, and save the final, edited version on drive A:, answer the "Name of file to edit?" question with B:TEST.DOC A:. When you end the editing session, you will be left with the file TEST.BAK on drive B:, and the file TEST.DOC on drive A:. For subsequent editing, it will be necessary to use drive A: as the source drive and B: as the destination. The second way to invoke this feature is from the CP/M (or MS-DOS) command line. To accomplish the same task using this method, simply type WS B:TEST.DOC A: at the A> operating-system prompt. You can change the mode (document or nondocument) to which WordStar will default using this method by using WINSTALL.COM.

If this still leaves you with insufficient room on the A: drive, WordStar can be run without the file WSMSGS.OVR on the

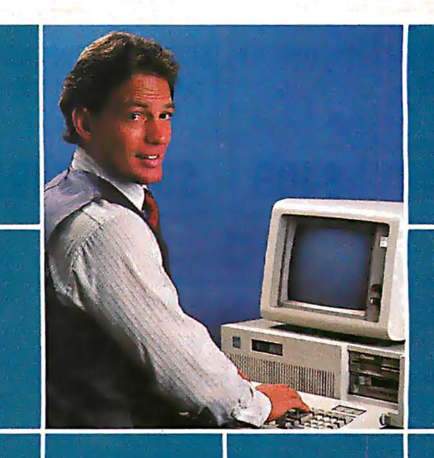
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LETTERS POLICY: *To be considered for publication, a letter must be typed double-spaced on one side of the paper and must include your name and address. Comments and ideas should be expressed as clearly and concisely as possible. Listings and tables may be printed along with a letter if they are short and legible.*

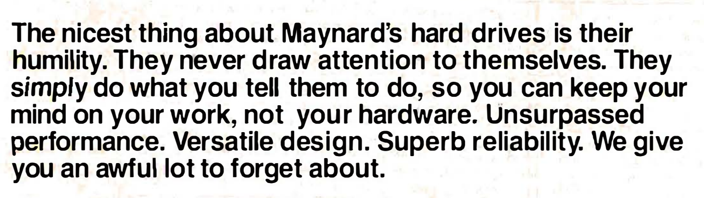
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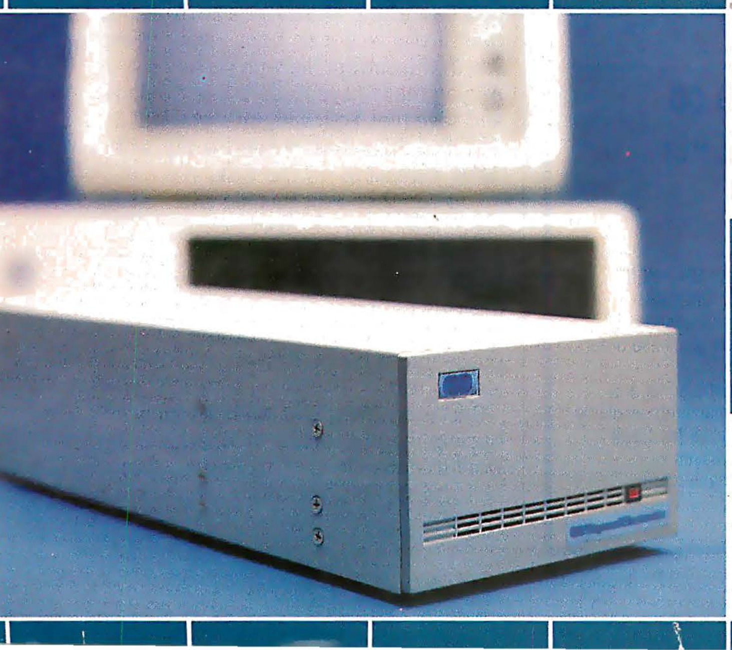




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system disk. All messages, including menus, will appear as "@@@@" in the upper left-hand corner of the screen, but if you have sufficient knowledge of WordStar's command structure, that shouldn't be more than an inconvenience.

As I mentioned, this feature is not well documented and, I must admit, it is of limited usefulness, except in certain situations when it makes the impossible possible.

NICK BURKITT
Long Beach, CA

As someone who uses WordStar professionally on a nearly a daily basis, both at work (as a technical writer) and at home (as a freelance writer), I was flabbergasted at several pieces of misinformation and bad advice offered by Dr. Vincent Alfieri in "WordStar as a Programming Tool."

Late in the article, Dr. Alfieri describes WordStar's "strange habit of keeping a backup file every time you edit an existing file. This means, in effect, that you must maintain a great deal of disk space for the necessary backup files."

So backup files (denoted by the .BAK extension) are bad, since they eat up disk space. Or are they?

Dr. Alfieri's attitude toward the WordStar backup procedure is perplexing, especially since one can justify WordStar's backup procedure by simply providing a better solution to a problem "solved" by Dr. Alfieri early on in the article. There, he recommends that, if you have recently saved and accidentally delete an important line of code, you can use the ^KQ (quit without saving file) command. He is silent on what to do if you haven't, which is frequently the case if you are on a roll.

However, thanks to WordStar's backup procedure, the situation isn't bad at all, even if you've got an hour's work behind you in the current file with no saves at all. All you really have to do is use ^KD (quit and save file). Following this, you will find that WordStar has created a file with a .BAK extension on the disk.

You can then edit this file (after changing or removing the .BAK extension). This allows you to find the missing text and block write it to disk. You can then reedit the original file, find the location of the missing text, and read it off the disk. This procedure is quick, easy, and involves no loss of text.

But even WordStar with its powerful backup feature cannot defeat those who work to defeat it, as Dr. Alfieri does when he suggests using files distinguished solely

(continued)

LETTERS

in terms of extensions (he suggests "P.1," "P.2," "P.3," etc.). Yes, in this case WordStar will keep only one backup for each of those files. That's great, if you're sure you'll never need a backup of any but the most recently edited file. I, for one, am not so confident.

Obviously, I think there are good reasons for backup files. Dr. Alfieri reminds us to keep *separate* backup files, but I know from nearly 10 years of working with computers and six years of working with WordStar that most people forget to back up their work, especially if they haven't lost any work lately. We WordStar users tend to be less sorry than most.

Finally, I am puzzled by Dr. Alfieri's contention that "You can actually get *more* pages on a disk with many small files than with one large file." This isn't entirely true, of course, except during an actual editing session.

Every file has overhead, and many systems allocate disk space in 2K-byte increments, including a minimum 2K-byte file size. Thus, it's easy to eat up disk space by having numerous files with somewhere between a few bytes and 2K bytes of unused bytes per file. Let's say that it's 1K byte on the average.

Then, if you take our example 180K-byte disk again and put 30 files of nominally 4K bytes each on it, it adds up to 120K bytes "used" and 60K bytes "free." The truth, however, is that about 30K bytes of disk space is eaten up in overhead. That's about 15 pages of text! If your system allocates in 1K-byte increments, that's still 15K bytes!

When you're editing a backed-up file, WordStar can require about three times the capacity of the file on the disk (one old backup, one working backup, and the file being edited). This means that on a disk with 180K bytes (formatted), you might want to avoid editing a file of 55K bytes or greater, especially if you expect to be expanding it by much.

The best solution is probably to work on one disk and keep a separate disk for file saves. If you save to this disk after each edit, then you can delete the .BAK files as you go, meaning that on a 180K-byte disk, you can safely edit a much larger file of 80K bytes or more.

THOMAS H. HUNSCHER
Tigard, OR

NEWS FOR SORCERER OWNERS

May I suggest that BYTE try to mention the many orphans that have arisen in the

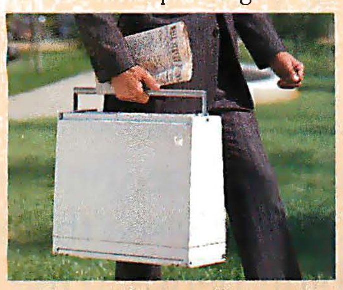
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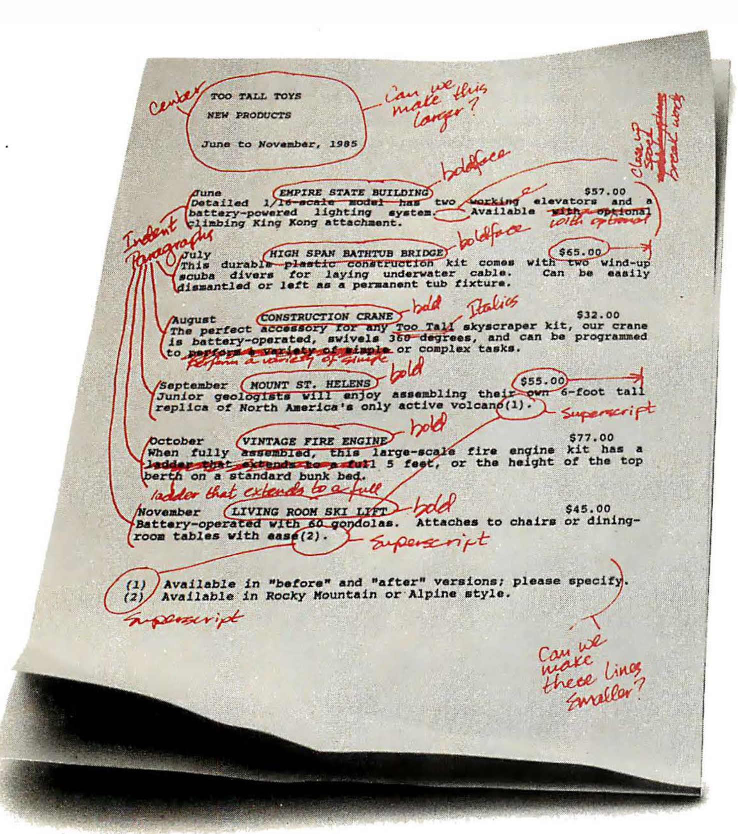
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NEW PRODUCTS

June to November, 1985

June EMPIRE STATE BUILDING $57.00
Detailed 1/16-scale model has two working elevators and a battery-powered lighting system. Available with optional climbing King Kong attachment.

July HIGH SPAN BATHTUB BRIDGE $65.00
This durable plastic construction kit comes with two wind-up scuba divers for laying underwater cable. Can be easily dismantled or left as a permanent tub fixture.

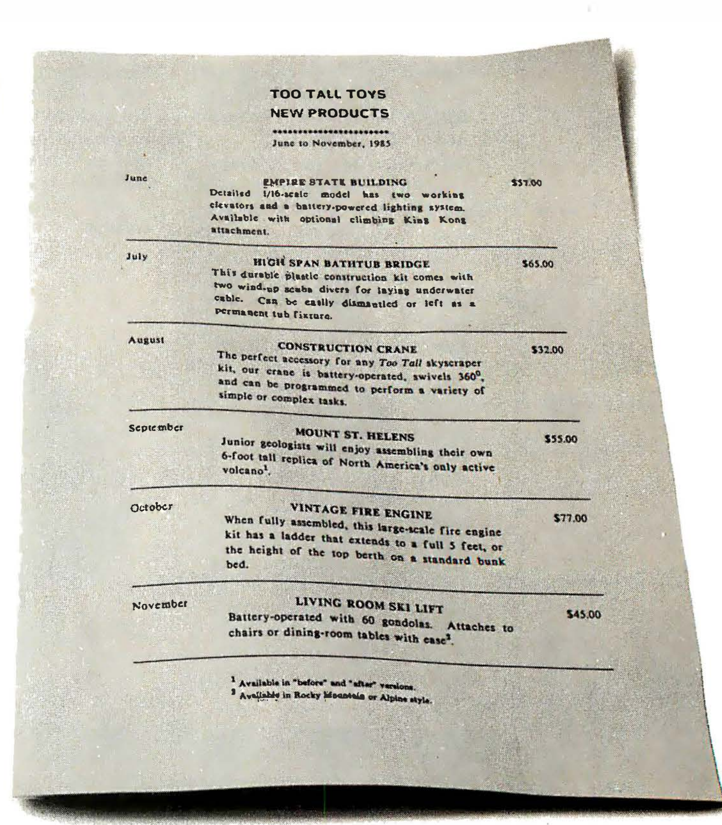
August CONSTRUCTION CRANE $32.00
The perfect accessory for any Too Tall skyscraper kit, our crane is battery-operated, swivels 360 degrees, and can be programmed to perform a variety of simple or complex tasks.

September MOUNT ST. HELENS $55.00
Junior geologists will enjoy assembling their own 6-foot tall replica of North America's only active volcano(1).

October VINTAGE FIRE ENGINE $77.00
When fully assembled, this large-scale fire engine kit has a ladder that extends to a full 5 feet, or the height of the top berth on a standard bunk bed.

November LIVING ROOM SKI LIFT $45.00
Battery-operated with 60 gondolas. Attaches to chairs or dining-room tables with ease(2).

(1) Available in "before" and "after" versions; please specify.
(2) Available in Rocky Mountain or Alpine style.



TOO TALL TOYS

NEW PRODUCTS

June to November, 1985

June	**EMPIRE STATE BUILDING** Detailed 1/16-scale model has two working elevators and a battery-powered lighting system. Available with optional climbing King Kong attachment.	$57.00
July	**HIGH SPAN BATHTUB BRIDGE** This durable plastic construction kit comes with two wind-up scuba divers for laying underwater cable. Can be easily dismantled or left as a permanent tub fixture.	$65.00
August	**CONSTRUCTION CRANE** The perfect accessory for any *Too Tall* skyscraper kit, our crane is battery-operated, swivels 360°, and can be programmed to perform a variety of simple or complex tasks.	$32.00
September	**MOUNT ST. HELENS** Junior geologists will enjoy assembling their own 6-foot tall replica of North America's only active volcano[1].	$55.00
October	**VINTAGE FIRE ENGINE** When fully assembled, this large-scale fire engine kit has a ladder that extends to a full 5 feet, or the height of the top berth on a standard bunk bed.	$77.00
November	**LIVING ROOM SKI LIFT** Battery-operated with 60 gondolas. Attaches to chairs or dining-room tables with ease[2].	$45.00

[1] Available in "before" and "after" versions.
[2] Available in Rocky Mountain or Alpine style.

Their first draft vs. our first draft.

be dirty.

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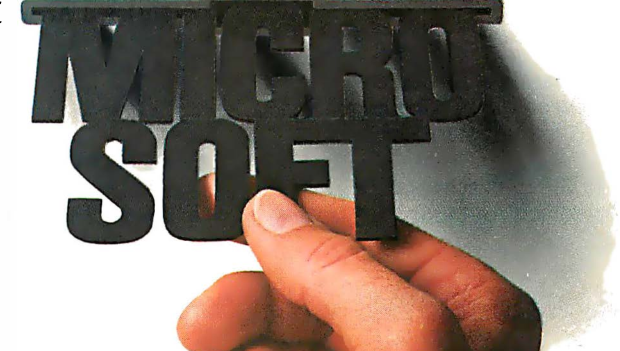
Word also includes a computer-based training disk that gets you up to speed quickly. Plus, a new comprehensive manual.

100% money-back guarantee.

You don't have to take our word about Word. Buy the new Microsoft Word from a participating dealer and if you're not satisfied for any reason, return it to the dealer within 30 days and he'll give you your money back.*

How do we get higher performance out of the PC? Simple, our MS-DOS® operating system tells the IBM PC how to think. And our BASIC is the language spoken by nine out of ten microcomputers worldwide.

So, if you want to clean up your act, act quick. Call (800) 426-9400. In Washington State, Alaska, Hawaii and Canada, call (206) 828-8088. And ask for the name of your nearest Microsoft dealer.



*Offer good in the United States on IBM PC versions of Microsoft Word purchased on or before August 31, 1985.

computer field. There are many micros that have no support now, and users who still have them are looking for help.

Ah, nostalgia! Remember Superbrain, TRS Model 1, IMSAI, Videobrain, and Exidy Sorcerer? Some people still have them but think they are frozen in time.

For some machines, that is not so.

The Exidy Sorcerer was still being made in 1984, under license in Holland. And there are still many fan magazines with software and hardware notes being published.

For the Exidy Sorcerer here are some of the magazines being published. (Write for subscription rates and possibility of back issues.)

European Sorcerer Club
Back issues only
Died with issue 43 in June 1984
Index in issue 26

Colin Morle
32 Watchyard Lane
Formby
Near Liverpool L37 3JU
England

Sorcerer Group International
c/o Don Gottwald
POB 33
Madison Heights, MI 48071
U.S.A.

Back issues from Gottwald at:
19967 Rosin Dr.
Mt. Clemens, MI 48044
U.S.A. (about $18 per volume for vols. 2 to 5)

now **Sorcerer Group International**
(8 times a year)
Tommy Stokes (or Ed King)
Route 1, Box 121
Everton, AR 72633
U.S.A.

Sorcerer Computers Users of Australia
(12 a year/Airmail)
Box 2402
Melbourne, Victoria 3001
Australia

Southern California Sorcerer Users Group
(4 to 6 a year casually)
c/o Cary E. Stewart
529 South Beachwood Dr.
Burbank, CA 91506
U.S.A.

ISIS (12 a year)
c/o Maurice Dow
84 Camberley Crescent
Brampton, Ontario L6V 3L4
Canada

Sorcerer User Group of South Australia (12 a year)
c/o Don Ide
14 Scott Rd.
Newton, South Australia 5074
Australia (index in issue 51)

Exidy Sorcerer Gebruikers Group
(6 a year)
Published in Dutch with full English cover-to-cover translation a month later
Index in issue 15

Redactie ESGG
P/a Postbus 510
NL-1000 Amsterdam
The Netherlands

Sorcerer User Group Schweiz
Monthly/in German

CH 3038 Kirchlindach
Switzerland (index in issue 50)

Sorcerer Computer Users of New Zealand
Monthly, some Sorcerer material

c/o Selwyn Arrow
POB 6210
Auckland, New Zealand

I won't give prices since they will change and many of the above don't know rates to the U.S. since no one has asked before.

Here are some software sources for the Sorcerer that you might want to keep on file:

Arrington (Ensign) Software
7337 Northview
Boise, ID 87304
U.S.A.

Howard Arrington
Suite E, 2312 North Cole Rd.
Boise, ID 87304
U.S.A. (This is an old address.)

COMTRO Software Development
Rec. Bonsel Str. 10
NL-6433 EP Hoensbroek
The Netherlands

Roger Hagan
1146 Fairview Ave. North
Seattle, WA 98109

System Software
1 Kent St.
Bicton, Western Australia 6157
Australia

Nigel Yeo
24 Bodmin Ave.
Macclesfield, Cheshire
England

Caicom BV
Nijverheidsstraat 22
NL-2802 AL Gouda
The Netherlands

Softdeal
Postbus 85
NL-1135 ZJ Edam
The Netherlands

Computer Collectief
Amstel 312 (t.o. Carre)
NL-1017 AP Amsterdam
The Netherlands

And some hardware help, firmware, and repair services:

B. J. (Bob) Freeman
414 Olive Way
Seattle, WA 99202
or
POB 1258
Seattle, WA 98111-1258
U.S.A.

Ion Weather
Morristown Municipal Airport
Morristown, NJ 07960
U.S.A.

Tercentennial Technical
70 Tercentennial Dr.
Billerica, MA 01821
U.S.A.

South Valley Electronics Inc.
Suite E, 2110 Walsh Ave.
Santa Clara, CA 95050
U.S.A.

Mentzer Electronics
590 South Hill Boulevard
Daly City, CA 94014
U.S.A.

The Brothers Van Montfort
(Gebroeders van Montfort)
Smedestraat 13
NL-6411 CR Heerlen
The Netherlands

DANIEL SAY
Vancouver, BC, Canada

APPLE II BLUES

I happened on Mr. Dennis Doms's letter ("A Call for Better Apple Support," September 1984, page 14) and but for near-identical circumstances, I would have dismissed it as one of those individual quirks in product support. I fully endorse Mr. Doms's comments. His perceptiveness of the ProDOS documentation problem is particularly commendable when one considers the fact that he is experienced in DOS 3.3!

In early March of this year our information-processing group decided that a small "user-friendly" micro might provide quick turnaround for some of our project record-keeping applications. Although the senior program manager was a Kaypro owner, he carefully avoided imposing his own preference on the organization. An Apple II+ owner made a seemingly sound recommendation that we get an Apple IIe with duodisk and a small dot-matrix printer.

Two days later, the Apple IIe arrived with its display, an Epson printer, and the duodisk. VisiCalc and two PFS packages also were provided to get things started. A seeming ton of books accompanied the units. A quick pilot run with VisiCalc and PFS was made, and a short training session was held for floor engineers and project managers.

People experienced losses of whole files, mutilation of data, and I/O errors using PFS. The possibility of human error was explored, and new data backup procedures were instituted. Repair of the duodisk decreased the variety of I/O errors but did not eliminate them. Substitution of the duodisk with two standalone drives did not help. The Apple technician blamed the problem on PFS. The salesman who had originally sold us the Apple and the software then sold us Appleworks. The users read Appleworks documentation, more training sessions were held, new files were established, data was reentered. Within a day there were more I/O errors and losses of data reported. The Apple dealer then replaced the main logic board and again worked on

(continued)

the duodisk. This finally solved the problem (both Appleworks and PFS work well now).

A task request arrived on my desk to write some printer set-up utilities and a project accounting package for the Apple. Coming from a CP/M-86, TRSDOS, and IBM-VS background, I didn't instantly see the relationship between the Apple DOS and BASIC. The undocumented "loading of Integer BASIC" was disturbing. My first effort on the printer routines worked well enough (after I found that I/O had to be directed to physical card slots and that the Apple did not support logical devices!). Since the design for the project accounting task involved multiple files and several large arrays, I broke out the books.

As in Dennis Doms's case, we had received a ProDOS users manual and an Apple IIe owners manual. These had no substantive information that documented the machine or Apple's software. The paper quality was nice; the indexes and tables of contents had errors. The ProDOS manual talked about differences from DOS 3.3 and seemed aimed at people familiar with Apple DOS. The ton of books also included books for the 80-column card, the Apricot printer card, a duodisk manual, a pamphlet for the display, and several excellent manuals for VisiCalc, PFS, and the Epson printer.

I called our dealer and was told that we deserved a ProDOS *Programmer's Manual* since it had been out of stock when we bought the machine. He did not have one but would special-order one for us. I described my needs for documentation and was told I would need the Applesoft and DOS 3.3 manuals and that these were extra-cost items. I was told to ignore all references to Integer BASIC since it was an "archaic tongue" and no documentation was in print for it. (Undocumented modules of an operating system bother me!) The pricing was confused, but a total of $70 plus tax finally went on our purchase order. We soon received a bill. Two trips to the dealer and multiple phone calls over a six-week period failed to produce the manuals. There was talk of them being in a warehouse, then being back-ordered from Apple, then being out of print. Finally, with a Friday promise that they would be mailed on Monday, Accounting paid the bill. Two weeks later the dealer produced an explanation that the required manuals were unavailable from Apple and there was no projected delivery date.

Two months after the first phone call about documentation, our "free" ProDOS *Programmer's Manual* arrived. It was much as Mr. Doms describes—dependent on the DOS 3.3 and Applesoft documentation. The senior program manager visited the Apple dealer and with some hostility offered an invitation to small-claims court. The salesman then gave us his personal copies of the DOS 3.3 and Applesoft manuals. We then considered that the purchase order had been filled!

Our company's purchasing agent will ensure that no more business is directed to the Apple dealer who sold us the IIe. Apple's viability in the microcomputer business is doubted by every engineer, project manager, and technician who has been associated with our IIe. We now have three more Kaypro owners. At the office I'm pleased by the Displaywriter with its

(continued)

If you don't have a Hercules Graphics Card, you could end up looking like this:

"I know, because one day it happened to me...

"I was running some routine tests on a non-Hercules monochrome graphics card when I was struck by a severe case of *low resolutionitis*. I'm the president of Hercules and that's me exhibiting the symptoms of the disease in its advanced stages. Not a pretty sight, is it?

"What causes *low resolutionitis?* Experts point to ordinary monochrome graphics cards with coarse, hard-to-read graphics. A bad case of eyestrain may develop if action is not taken immediately.

"Fortunately for me, a Hercules Graphics Card was nearby. A quick change brought soothing 720 x 348 graphics. That's twice the resolution of ordinary 640 x 200 graphics cards.

"Which means better graphics for Lotus™ 1-2-3™, Symphony™, Framework™, pfs:Graph®, Microsoft® Chart and Word, SuperCalc3®, AutoCad™, and dozens of other programs.

"Including Microsoft Flight Simulator, now Hercules compatible!

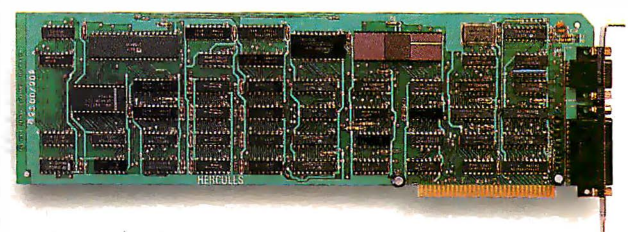
"Oh, and don't forget that a parallel printer port is standard on the Hercules Graphics Card, not an extra cost option.

"Now, if you're worried about buying a new product that hasn't had all the bugs worked out, relax. Hercules has sold more monochrome graphics cards for the IBM® PC, XT™ and AT™ than anyone else in the world.

"So... you're convinced that you should buy a Hercules Graphics Card. Now, steer clear of cheap imitations. You may save a few bucks, but you won't get all of these five essential features which only Hercules has:

"1) A safety switch that helps prevent damage to your monitor, 2) the ability to keep an IBM or Hercules Color Card in your system, 3) the ability to use the PC's BASIC to do graphics, 4) a Hercules designed chip that eliminates 30% of the parts that can go wrong, and 5) a two year warranty, because we think reliability is something you should deliver and not just talk about."

Call **1-800-532-0600 Ext 408** for the name of the Hercules dealer nearest you and we'll rush you our free info kit.



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p-System. I am quite happy with my TRS-80 at home. Recent clamorings by my offspring for Macintoshes coincided with the IIe problems. Both kids and their friends understand why I hesitated then made another choice for them.

This is my first experience with an Apple. I have no personal need to make it more detailed or extended in time. I find the documentation to be shallow, the I/O implementation crude (even when measured against 1980 standards), and the service haphazard. I more carefully assess what Apple owners and users have to say about their machines.

My feelings might not be quite so strong if only the hardware or the documentation had been screwed up. The infant mortality in the hardware combined with documentation hassles have heavily underscored the flaky sales support and the mediocrity of the operating system and language. Color Apple with a worm in it!

By contrast, Digital Equipment Corporation provides us with singularly outstanding support for our Rainbow. That system is supported by an excellent certification program for third-party software. If DEC says that a particular package such as CTOS or Lotus 1-2-3 will run on the Rainbow, you can bet the company has tried it and within the range of their tests has found no implementation bugs. Our IBM Displaywriters use CP/M-86 and UCSD p-Systems that have outstanding support from D/R and Softtech as well as IBM. My TRS-80 came with a language reference manual and DOS manual as well as owners/operators manuals. The additional technical reference manuals were readily available from the dealer at nominal charges. Every Tandy manual was well written, pretty much stand-alone, and had a good reference appendix. The indexes and table of contents did not contain errors in page numbers.

Just out of curiosity, I priced documentation at our local Commodore dealer and at a nearby Tandy Computer Center. Much of it is free with the system, and the prices on the remainder are moderate—what's more, it's readily available.

PAUL M. HINE
San Diego, CA

When a manufacturer sells a computer and withholds information on that computer, the computer's worth is in direct proportion to the amount of information one receives. No information means the computer is worthless. A computer is unique in this regard. If you buy a car, someone can always drive it or fix it without a shop manual. Try programming a computer to do something you want it to do without information on the I/O ports or the memory map. Try getting a computer fixed that no one has schematics for. Of course, somebody can always charge you three or four hundred dollars and replace the entire main circuit board when only a twenty-cent chip may be defective. You don't need a schematic to do that. After all, the manufacturer makes a lot of money selling you a new circuit board for $400 when you don't need one.

I have an Apple IIc. I was originally interested in the compact Apple IIc because of its built-in disk drive and its ability to be powered from a 12-volt car battery. Apple computer promised some day Real

(continued)



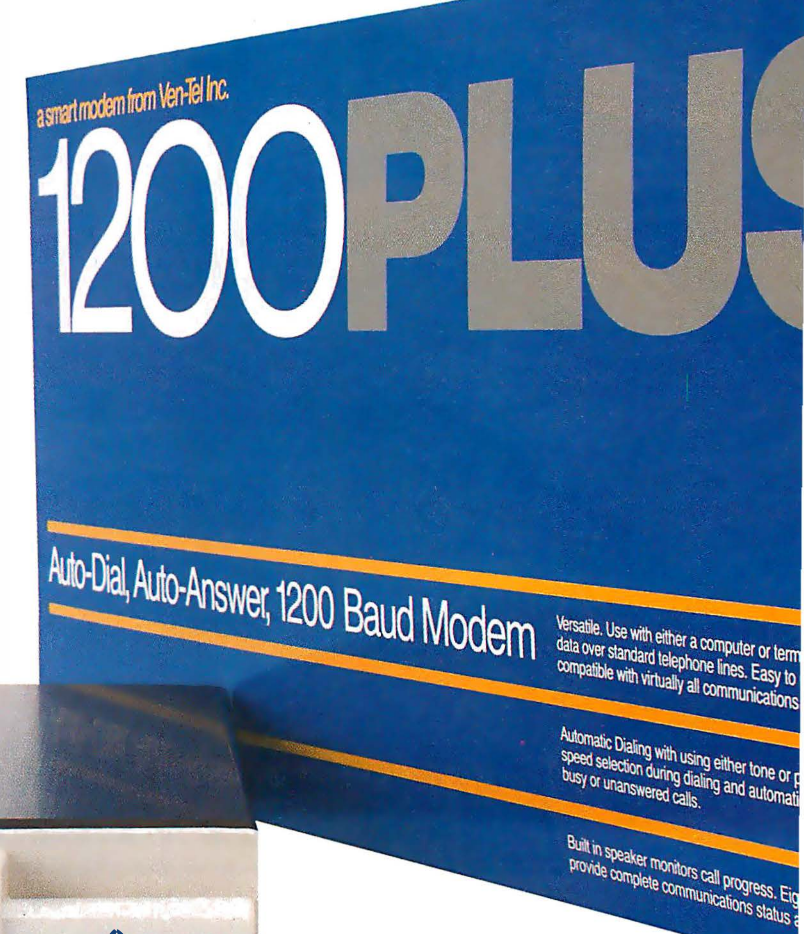
A few smart reasons to buy our smart modem:

Features	Ven-Tel 1200 PLUS	Hayes
1200 and 300 baud, auto-dial, auto-answer	Yes	Yes
Compatible with "AT" command set	Yes	Yes
Can be used with CROSSTALK-XVI or Smartcom II software	Yes	Yes
Regulated DC power pack for cool, reliable operation	Yes	**No**
Eight indicator lights to display modem status	Yes	Yes
Speaker to monitor call progress	Yes	Yes
Attractive, compact aluminum case	Yes	Yes
Two built-in phone connectors	Yes	**No**
Compatible with The Source and Dow Jones News Retrieval	Yes	Yes
Unattended remote test capability	Yes	**No**
Phone cable included	Yes	Yes
Availability	Now	
Price	**$499**	**$699**

The Ven-Tel 1200 PLUS offers high speed, reliable telecommunications for your personal computer or terminal. Whether you use information services or transfer data from computer to computer, the Ven-Tel 1200 PLUS is the best product around. Available at leading computer dealers and distributors nationwide.

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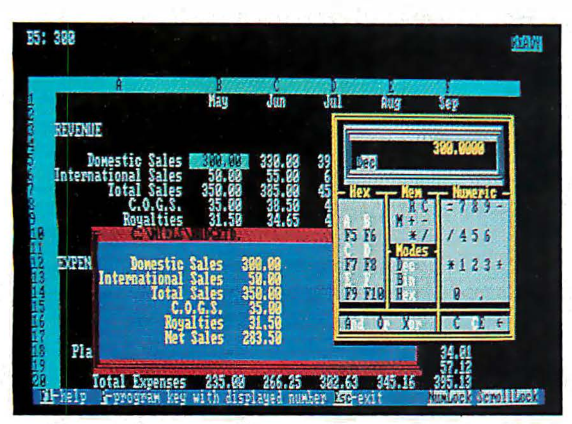
Ven-Tel Inc.
2342 Walsh Avenue
Santa Clara, CA 95051
(408) 727-5721

SIDEKICK

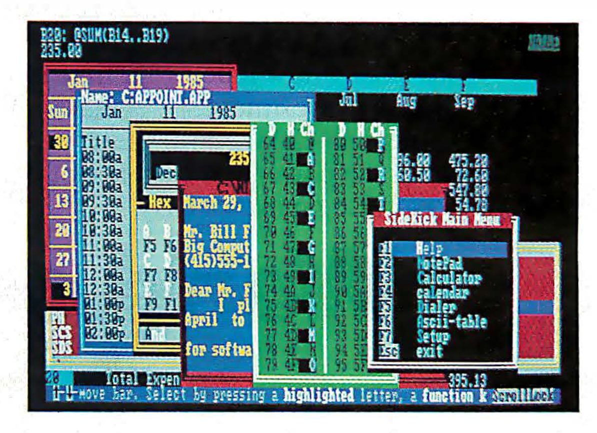

NOTES
* Bill - 303-7421
* Stocks
* Mr. Wilson is contact at Acme Hardware
JANUARY
TRADE SHOW
ASCII TABLE
ASCII TABLE
IBM
IBM
IBM
ROBERT 84 TINNEY

Borland's SideKick Software Product of the Year

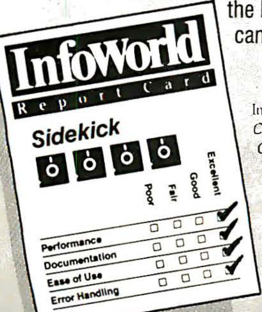
SideKick is InfoWorld Software Product of the Year. It won over Symphony. Over Framework. Over ALL the programs advertised in this magazine. Including, of course, all the "fly-by-night" SideKick imitations. SideKick . . . . Simply the best.



Here's **SideKick** running over Lotus 1-2-3. In the SideKick **Notepad** you'll notice data that's been imported directly from the Lotus screen. In the upper right you can see the **SideKick Calculator**.



All the **SideKick** windows stacked up over Lotus 1-2-3. From bottom to top: SideKick's **"Menu Window", ASCII table, Notepad, Calculator, Appointment Scheduler/Calendar,** and **Phone Dialer**. Whether you're running WordStar, Lotus, dBase, or any other program, SideKick puts all these desktop accessories instantly at your fingertips.



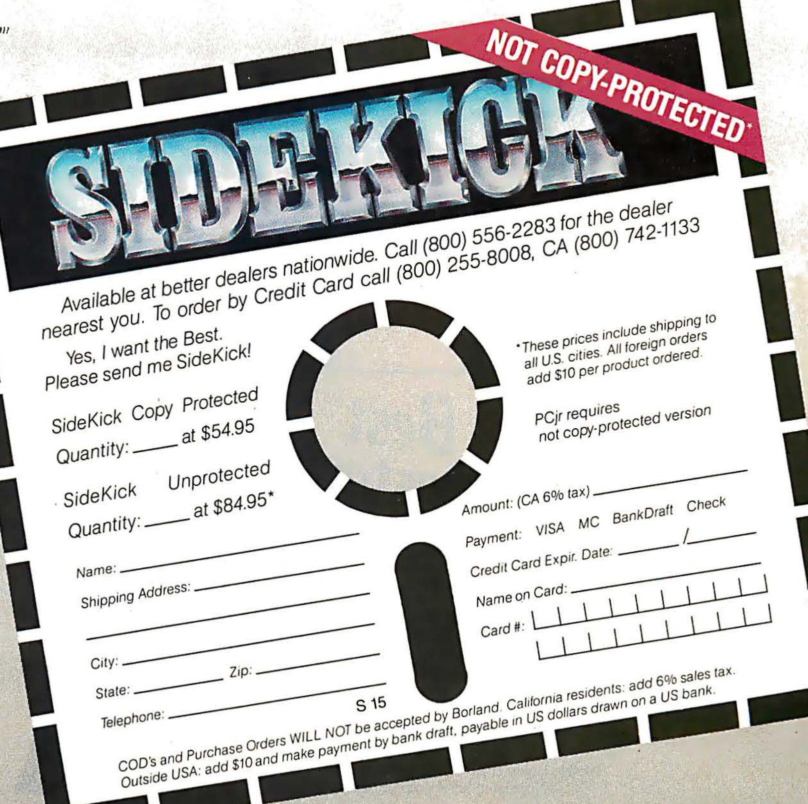
InfoWorld *Report Card* 1984 *by Popular Computing, Inc., a subsidiary of CW Communications Inc. Reprinted from* InfoWorld, *1060 Marsh Road, Menlo Park, CA 94025.*

Jerry Pournelle, BYTE: *"If you use a PC, get SideKick. You'll soon become dependent on it."*

Garry Ray, PC Week: *"SideKick deserves a place in every PC."*

Charles Petzold, PC Magazine: *"In a simple, beautiful implementation of WordStar's block copy commands, SideKick can transport all or any part of the display screen (even an area overlaid by the notepad display) to the notepad."*

Dan Robinson, InfoWorld: *"SideKick is a time-saving, frustration-saving bargain . . . ."*



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Amount: (CA 6% tax) ____
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Credit Card Expir. Date: ____/____
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S 15

COD's and Purchase Orders WILL NOT be accepted by Borland. California residents: add 6% sales tax. Outside USA: add $10 and make payment by bank draft, payable in US dollars drawn on a US bank.



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Scotts Valley, California 95066
TELEX 172373

LETTERS

Soon Now to have a liquid-crystal display that would draw very little power and operate from a battery.

The first snag I ran into was when I tried to find out from the Apple IIc manuals what the pin connections were for the nonstandard serial-port connector. No luck. Nowhere in the manuals that came with the computer could I find the connections for the serial interface.

The next thing I did was call Apple long distance. I was put on hold for five minutes listening to some music. Needless to say, it was not high-fidelity. Finally, Patty came on the line and told me I had to call another long-distance number in another part of the country. Get this, I am in L.A. Well, I called that number, and an answering machine came on the line telling me to leave my name and phone number and my question and they would get back to me within 24 hours. Since I am in and out of the office all day and no one else at my office is knowledgeable enough to ask intelligent technical questions about RS-232C interfaces, that might be a problem. If Apple personnel happened to call back while I was out of the office, at least another 24 hours would go by before I could ask the first question. At this rate, a year or more would go by before I could write this assembly-language program to talk to the Apple IIc. The answering machine also advised me to contact my nearest dealer.

We have a lot of Apple dealers here in L.A. I contacted three of them. None of them knew anything more about it than I did. One advised me to go to all of the bookstores and get a book on the Apple IIc. I did just that; in fact, I bought three books. So far, I have spent at least 40 hours of my valuable time, $40 on books, and $50 on long-distance phone calls. I now know the pinouts on the connectors, but that is all the useful information those three books could tell me. Absolutely nothing else of any value. No memory locations for setting up the RS-232C interface chip or how to write code to send or receive data from the RS-232C interface in assembly language or BASIC. Nothing.

Has Apple management grown so greedy that it doesn't want people to buy any device to hook up to an Apple IIc unless they buy it from Apple? Does Apple want anyone to write and sell software other than Apple Computer? Is Apple management so paranoid that someone will copy the IIc that it is afraid to document the ROM? Why does Apple have an army of lawyers ready to sue

(continued)

NEW PRODUCT NEWS FROM TELETEK

Systemaster II. Responding to market demand for speed and increased versatility, Teletek is proud to announce the availability of the next generation in 8-bit technology — the new Systemaster II! The Systemaster II will offer two CPU options, either a Z80B running at 6 MHz or a Z80H running at 8 MHz, 128K of parity checked RAM, two RS232 serial ports with on-board drivers (no paddle boards required), two parallel ports, or optional SCSI or IEEE-488 port. The WD floppy disk controller will *simultaneously* handle 8" and 5¼" drives. A Zilog Z-80 DMA controller will provide instant communications over the bus between master and slave. Add to the DMA capability a true dedicated interrupt controller for both on-board and bus functions, and the result is unprecedented performance. Systemaster II will run under CP/M 3.0 or TurboDOS 1.3, and fully utilize the bank switching features of these operating systems.

SBC 86/87. As the name indicates, Teletek's new 16-bit slave board has an Intel 8086 CPU with an 8087 math co-processor option. This new board will provide either 128K or 512K of parity checked RAM. Two serial ports are provided with individually programmable baud rates. One Centronics-compatible parallel port is provided. When teamed up with Systemaster II under TurboDOS 1.3, this 5MHz or 8MHz multi-user, multi-processing, combination cannot be beat in speed or feature flexibility!

Teletek Z-150 MB. Teletek is the first to offer a RAM expansion board designed specifically for the Z-150/Z-160 from Zenith. The Teletek Z-150 MB is expandable from 64K to 384K. Bring your Z-150 up to its full potential by adding 320K of parity checked RAM (or your IBM PC, Columbia, Compaq, Corona, Eagle, or Seequa to their full potential). The Teletek Z-150 MB optionally provides a game port for use when your portable goes home or a clock/calendar with battery backup!

Evaluate the Systemaster II, SBC 86/87 or Teletek Z-150 MB for 30 days under Teletek's Evaluation Program. A money-back guarantee is provided if not completely satisfied! All Teletek products carry a 3-year warranty.

(Specifications subject to change without notice.)

EXTRA! TELETEK TIMES EXTRA!
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Tel: 221-6033 (P A B X)
Telex: 1123888 CICP BR

TELETEK

4600 Pell Drive
Sacramento, CA 95838
(916) 920-4600
Telex #4991834
Answer back — Teletek

Inquiry 382

SBC-I
SBC-II
SYSTEMASTER
HD/CTC

Yes, I'm interested in information regarding:
☐ Systemaster II
☐ SBC 86/87 ☐ Z-150
☐ Evaluation Program
☐ Teletek's S-100 Board Lir

Name ____
Company ____
Address ____
____

anyone if the company even hints of manufacturing a machine that will run Apple software? Hasn't Apple management learned that the more information you supply in the box with the computer, the less money it takes to support the product? Is the well-documented IBM PC outselling Apple everything?

One would think that Apple had learned its lesson with the Apple III. The Apple III came with no real documentation as well. We all know what happened to the Apple III. From what I have seen of the Macintosh documentation, the Mac is in the same boat. I would not use a Mac if you gave me one.

The next problem I found was that the RS-232C data-transmission rate in the Apple IIc was off frequency by just enough to prevent the RS-232C from working properly. Apparently Apple divided down the microprocessor clock crystal to save the $3 cost of a data-transmission rate crystal. If the IIc had a schematic in the owners manual, any competent computer technician would know about the transmission-rate problem before purchasing the computer. I guess that is one of the reasons Apple did not put a schematic in the owners manual in the first place. The man on the Apple hotline told me to take the IIc into any Apple computer dealer, who would fix it at no cost. None of the three dealers I contacted had heard of this repair program, nor would they do it at no cost.

If you buy an Apple other than the IIe, you need your head examined.

A Commodore 64, although it costs much less than the Apple IIc, is worth at least 100 times as much because you can use it. You can get a vast quantity of programming and technical information on the Commodore 64 in great detail. Information that is necessary to program and interface all the things that people need a microcomputer for.

I now own a $1200 paperweight.

PAUL LAMAR
Redondo Beach, CA

WHERE ARE APPLE'S MANUALS WHEN YOU NEED THEM?

Last night I tried to order an *Apple IIc Reference Manual* at my local dealer. I was told that the manual costs $50, could be ordered only in boxes of five, and if I would order five that they would be glad to handle my order. Of course I thought that I would go elsewhere.

When I arrived home, some back issues of *Apple Assembly Line* had come in the mail. I discovered that Texas Apple dealers had the same policy and that it extended to ProDOS and IIe manuals as well. Eventually I learned that these manuals could be ordered by mail from a dealer in New York (212-512-4100).

Providing access to the fundamental hardware manuals for the machine is the most minimal level of dealer support possible. Perhaps K-Mart does not provide access to manuals for the computers it sells, but every self-respecting computer dealer must do this.

The poor availability of these manuals must in part stem from the fact that they are seen as manuals only a hacker or professional software developer would want or need. Apparently Apple believes that its customers are not likely to grow in

(continued on page 436)

Inquiry 198

UPDATE

C Changes Quickly

Our December 1984 article "C-Language Development Tools" by G. Michael Vose (page 119) brought several new C interpreter vendors out of the woodwork. We also learned of a name change for one of the article's previewed products.

The Safe C Compiler from Catalytix Corporation (55 Wheeler St., Cambridge, MA 02138) is now called the Safe C Runtime Analyzer. The product's functions have not changed, only the name, to distinguish it from production compilers.

Catalytix also announced the release of its Safe C Standalone Interpreter. The interpreter is a complete C implementation that allows the use of any text editor and source-code formatting or cross-referencing utilities. Code interactively written and debugged within the interpreter can subsequently be compiled into executable files, using any complier that conforms to the Kernighan & Ritchie (K&R) C-language specification. Currently available for the IBM PC and other MS-DOS machines, the Safe C Standalone Interpreter sells for $400. A Macintosh version is under development.

Age of Reason Company (318 East 6th St., New York, NY 10003) has announced the availability of RUN/C—a C interpreter for MS-DOS computers. Distributed by Lifeboat Associates (1651 Third Ave., New York, NY 10128), RUN/C costs $150.

RUN/C features a built-in line editor similar to the Microsoft BASIC editor, plus the capability to use an outside editor. You can even compile your C programs from *within* the RUN/C interpreter. RUN/C fully implements the K&R specification for C, but this interpreter has a limit of 2000-line programs.

Gimpel Software (3207 Hogarth Lane, Collegeville, PA 19426) markets a C interpreter called C-terp, also for the IBM PC and work-alikes using MS-DOS 2.x. C-terp costs $300; a demonstration disk is available for $45. C-terp also fully implements the Kernighan & Ritchie C-language specification, includes an editor, and offers batch-mode operation. C-terp supports small or large memory models.

Lastly, Computer Innovations (980 Shrewsbury Ave., Tinton Falls, NJ 07724), purveyors of the C86 C Compiler, offers Introducing-C, a C interpreter designed to help the programming novice learn C as her/his first language.

Introducing-C does not fully implement the K&R C specification, but it documents the differences in a 10-page appendix. For example, Introducing-C does not support multidimensional arrays, #defines, struct and union data structures, the typedef declaration, and several other components of C. Future revisions to the interpreter will provide many of the features currently missing. Introducing-C's interpreter is upward-compatible with the C86 compiler.

Computer Innovations claims that Introducing-C is suitable for learning structured programming and most of C and for developing "medium-sized, non-scientific programs." Available for the IBM PC, Introducing-C costs $95.

FEEDBACK

Printer Buffer Messaged

In the June 1984 BYTE there were several errors in the article "Build a Printer Buffer" by John Bono (page 142). Richard Carlsen from Upton, New York, built the printer buffer, encountered and overcame some difficulties, and wrote us about his travails. Here are some excerpts from his letter:

I noticed corrections in the November 1984 BYTE on the ROM listings (page 34), but I haven't seen any hardware updates, so here are some suggestions for improving John Bono's project.

In listing 1 on page 453 (June BYTE), line 13 should show EQU 0FFFFH (zero, not "oh") and line 17 should be A, 0FFH.

In the schematic on page 450, IC 14 is incorrectly labeled 74LS00 at the top of the page. IC 14 is a 74LS367A. (I should also note that I tried both the 74LS367s and 74LS367As, and they both work fine.) Input pins 4 and 10 of IC 14 should be tied high or at least not left floating as those sections are unused. Floating leads are not good practice and could cause some occasional errors.

On the middle left on page 450 the data lines are in inverse order. D0 should be D7, D6 should be D1, and so on until D7 is D0. They are labeled correctly at the Z80 and 2716.

A useful item to add is a reset switch across the 68-μF (microfarad) cap on pin 26 of the Z80. I added a 47-ohm resistor in series with the switch so discharge of the 68-μF cap is a little more gentle.

At the lower right on page 452 you'll find IC 13 and IC 24 (printer acknowledge FF). A signal is missing (G6) at IC 13, pin 9. Remove pin 4 of IC 24 from +5 V. Leave IC 24, pin 2 connected to +5 V. Now connect pin 4 of IC 24 to pin 9 of IC 13. This will allow D306 at line 26 on page 453 to reset the printer's acknowledge flip-flop.

On page 452, data lines, strobe, busy, and acknowledge to the left of IC 9 should be labeled "TO COMPUTER." At the right of IC 15 they should be labeled "TO PRINTER."

Be aware that all 4164 RAM chips are not created equal. They come in different speeds usually designated by a -2 or -3 suffix. I have had no trouble with either. However, some companies require 128 refresh cycles over a 2-microsecond period. Others may require 256 refresh cycles over a 4-microsecond period. I used NEC 4164-2 chips and Mostek 4564-2 chips successfully, both of which require 128 cycles. Others requiring 256 refresh cycles gave me occasional errors.

Another pointer: Watch the power wir-

(continued)

ing to these RAM chips. Pin 16 *is* ground and pin 8 *is* +5 V. This is not as you would usually expect with 16-pin chips, and I sure got caught wiring these wrong.

On my unit I used a crystal oscillator at 1 MHz hooked to pin 6 of the Z80. If you do this, a 1K pull-up resistor or so at pin 6 will ensure that the "1" levels are 4.0 to 4.5 V as the Z80 requires there.

Not all printers and computers handle Centronics interfacing in the same manner. My Kaypro 2, for example, does not use the ACK signal. The buffer works fine with my Okidata 92 with the Kaypro using just the busy signal. Your computer may also use other signals such as the "Paper Out" line. Consult your printer and computer manuals or dealer about your printer and computer parallel ports before starting this project. In most cases you should be able to work things out with the available signals supplied by the buffer.

Some new ideas have been suggested by other readers of this article for improving the project and I'll pass them on.

1. Multiple dumps by the use of a repeat printout switch would be useful. This would allow extra copies of a document to be printed from the buffer's memory without disturbing the computer. Recoding of the RAM and some minor hardware additions would be necessary.
2. Self-check of memory. This would also require some additional ROM coding.
3. A printer code preloader, which would let you change printer functions (such as compressed print mode, character pitch, or near letter quality) by sending the printer prewritten codes stored in the printer-buffer ROM. These could be selected by thumb-wheel switch and entered to the printer by a push-button switch using the remaining port 7 select at G7 pin 7 of IC 13 as a means of addressing this feature.

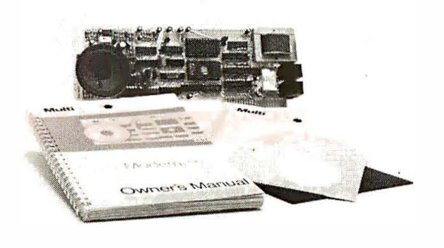
If anybody has completed these or other features, please write in to BYTE and let the rest of us in on it. This is a great project when it's working. I would like to thank John Bono for writing this article and for his patience with my questions. I wish also to thank other readers for their time on the phone and exchange of ideas, and BYTE for acting as the intermediary.

BYTE'S BUGS

Communication on Modem Gets Garbled

In the What's New section of the *Guide to the Apple Personal Computers*, a special supplement to the December 1984 BYTE, we inadvertently published the wrong picture and supplied some incorrect information.

The picture on page A136 does not depict Multi-Tech Systems' internal modem card for the Apple II, but rather it shows Multi-Tech Systems' MultiModem 1200/300-bps external modem.



The single-board MultiModem IIe, shown here, fits entirely inside Apple II series computers and does not require a serial card. It operates at 110/300 bps, features auto-answer and auto-dial, and comes with communications software. The list price is $229, which includes free-time and subscription discounts to a number of database networks, such as Dow Jones News/Retrieval Service and the Instant Yellow Page Service.

The MultiModem 1200/300 stores up to six 31-digit telephone numbers, detects dial and busy tones, and can continuously redial busy numbers. It lists for $549.

Both modems come with two-year warranties. Multi-Tech Systems Inc. is headquartered at 82 Second Ave. SE, New Brighton, MN 55112, (612) 631-3550.

Corrections from Commodore

The model number of Commodore's new 128K-byte computer was incorrectly stated in the February What's New section (page 40).

The computer is known as the Commodore C128. Also, it uses the 8502 microprocessor to run Commodore software and its Z80 coprocessor runs at 4 MHz.

The article also described a new high-speed disk drive that works with both the C128 and the C64. In its C64 mode, the drive transfers data at 300 cps. While in its C128 or CP/M modes, the data rate is 5200 cps. ■

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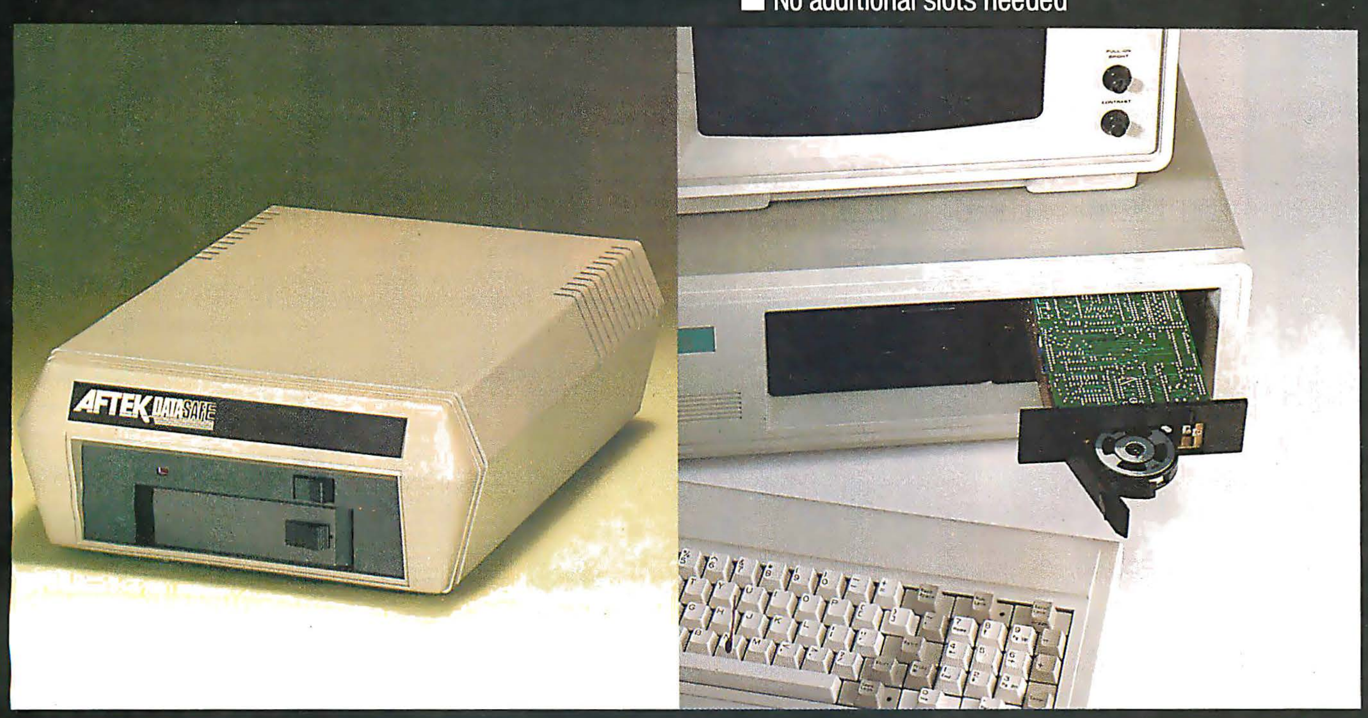
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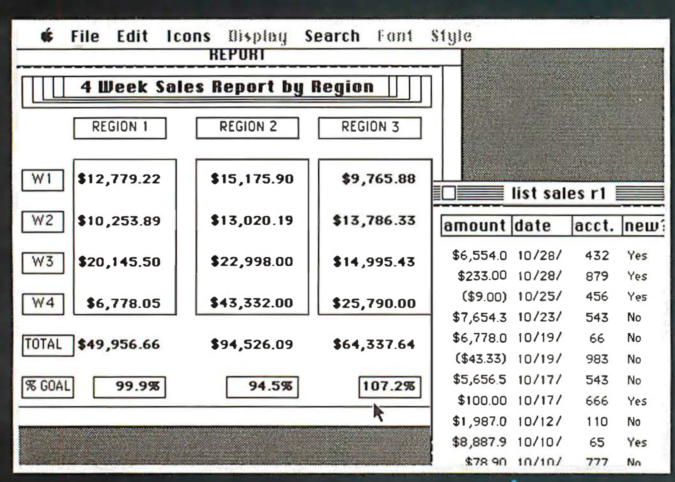
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14206
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Willowdale, Ontario
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Tel.: (416) 497-0531 or toll free
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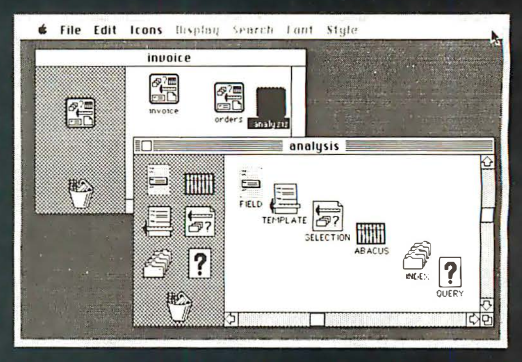
Inquiry 17

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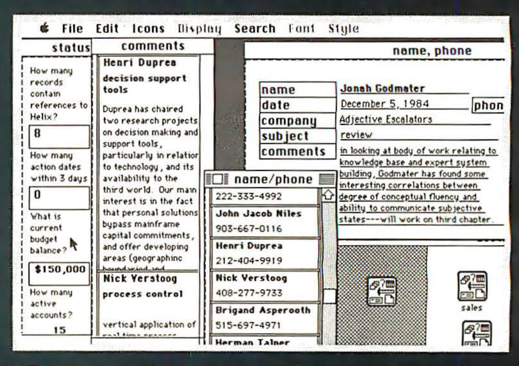


Helix is a data-based system, so that once you enter information you can use it for anything – reports, lists, analyses, mail merge printouts, or even relational look-ups to other data-bases within Helix.



The full functionality of Helix lies within its six basic icons. You can "learn by doing" with Helix, since it does not get in your way with imposed structure or restrictions. You don't have to worry about parameters, command codes, or "modes".

Requires: an external drive or hard disk
Runs on: 512K Macintosh ▪ Lisa with MacWorks
Supports: Hard disks ▪ Keypad ▪ 15″ Imagewriter
Includes: Helix Program disk ▪ Helix Guided Tour disk ▪ Helix Resource/Work disk ▪ User Manual ▪ 18-ring project binder ▪ Reference pad for custom documentation ▪ Registration card for support & updates
Offers: Modeless input, interactive query, editing, & report generation ▪ Text-formatting ▪ Calculations between fields & across records ▪ Object-oriented, icon-based design ▪ Relational Look-ups ▪ List management ▪ Mail merge ▪ Clipboard & ASCII file transfer ▪ Special Template tools for form design ▪ User defined, automatically updated Indexes ▪ Unrestricted length & number of fields ▪ Complete printing options ▪ Vertical and horizontal autoscroll ▪ Visual building blocks for arithmetic, date, text & Boolean operators, functions, & values.



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DAISY WHEEL	C. ITOH	A10-20S	29	$ 669
	QUME	LP20	20	799
	NEC	2010	20	950
	DIABLO	620	20	995
	C. ITOH	F10-55	58	1,449
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	QUME	1155	55	1,995
	NEC	7700	55	2,495

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Inquiry 55 for Dealers. Inquiry 56 for End Users.

Thermal Printer Has Full Graphics Ability

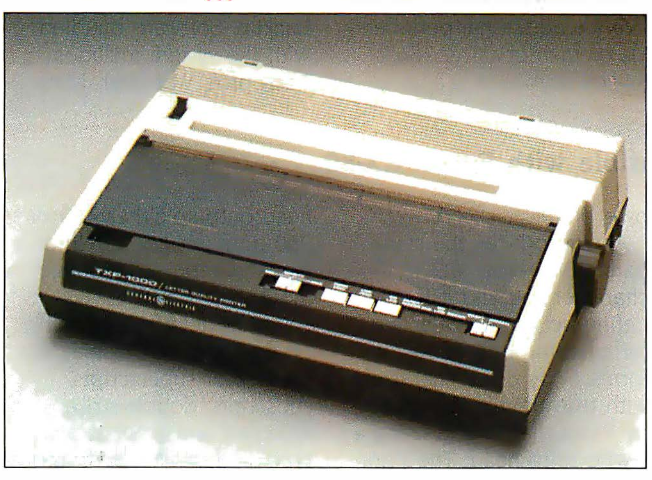
General Electric recently announced the Model 3-8100, a $300 thermal-transfer letter-quality printer with full graphics capability. Although the printer comes standard with a Centronics-type parallel connector, GE will also sell two compatibility modules for $89.95. One allows direct connection to the Atari 400/800 computers and Commodore's 64 and VIC-20; the other module permits direct connection to the IBM PCjr.

The Model 3-8100 prints at two speeds: 50 cps in draft mode and 25 cps in letter-quality mode. At both speeds, the printer is quiet. A 16-dot print head provides high-resolution dot-matrix output.

The Model 3-8100 can use single-sheet, roll, or 9½-inch-wide fanfold paper. It prints on thermal paper if you remove the cartridge. Each ribbon cartridge costs about $6 and provides about 100,000 characters.

The manufacturer's suggested retail price for the Model 3-8100 is $299.95. Contact General Electric Co., Consumer Electronics Business Operation, POB 4840, Electronics Park, Syracuse, NY 13221, (315) 456-3304.

Inquiry 600.



The General Electric 3-8100 dot-matrix printer.

Keyboard Enhancement Has Macros, Data Encryption

Borland International's SuperKey is a RAM-resident keyboard-enhancement program featuring macros and automatic data encryption. This program lets you define, edit, save, load, and recall macros on your IBM PC in real time.

SuperKey has a memory-resident full-screen macro editor that can be pulled down on top of a currently running program. The program supports single-key macros, user-definable macro titles, help menus, date/time information, alternate arrow-key definition, key-click switching, keyboard lock/unlock, sound effects, and color control.

With SuperKey, you can recall from a command stack the last 20 commands entered. These are displayed in a menu window that lets you select, edit, and reuse the commands at the DOS command level or in a program. SuperKey has a cut-and-paste capability that permits any data to be copied from the screen, stored within SuperKey under any key, and then moved into another application.

The SuperKey data-encryption function lets you encode files in two modes. In the first mode, no second file is created, thus saving disk space. In the second mode, you can encrypt binary files by transforming them into ASCII. This lets you transmit these files over telephone lines. The recipient of the files decrypts them using a special "key."

Also featured is a display burn-in protection capability that automatically switches off a monitor's video signal when no activity is detected for a reasonable length of time. The display is automatically reactivated when any key is pressed. The program is priced at $69.95. Contact Borland International, 4113 Scotts Valley Dr., Scotts Valley, CA 95066, (408) 438-8400.

Inquiry 601.

GE TVs Also Serve As Monitors; Modem Unveiled

Two new television sets from General Electric can also serve as your computer monitor. The Model 13BC5509 is a 13-inch color monitor, and the Model 12XR5204 is a 12-inch black-and-white monitor.

Both units handle 80-character-per-line displays and feature a display width-reduction capability that prevents character loss at the screen's edge. They accept composite-video input as well as standard antenna connectors and are compatible with most home computers from Apple, Atari, Commodore, IBM, and other manufacturers.

Suggested retail price is $489.95 for the color monitor and $129.95 for the black-and-white unit.

In a concurrent announcement, GE introduced the Model 3-8200 direct/acoustic modem. This 300-bps modem has a standard RS-232C cable, and optional cables are available for direct connection to Atari or Commodore computers.

The 3-8200 has automatically switchable answer/originate modes and once tied into a database, it automatically adjusts for full- and half-duplex operation.

The Model 3-8200 modem has a suggested retail price of $119.95. Contact General Electric Co., Consumer Electronics Business Operation, POB 4840, Electronics Park, Syracuse, NY 13221, (315) 456-3304.

Inquiry 602.

(continued)

Kaypro's 286i Is an IBM PC AT Compatible

Kaypro's 286i, scheduled for formal introduction last month, is compatible with IBM's Personal Computer AT. It features a 6-MHz 80286 processor, two parallel ports, one serial port, and two 1.2-megabyte 5¼-inch floppy-disk drives. The system's main board comes with 512K bytes of RAM, expandable to 640K bytes; expansion cards can supply an additional 15 megabytes of RAM to the system.

Three of the system's eight IBM-compatible expansion slots are occupied, leaving five for additional peripherals or memory. The 286i's 84-key keyboard is also functionally compatible with the PC AT's.

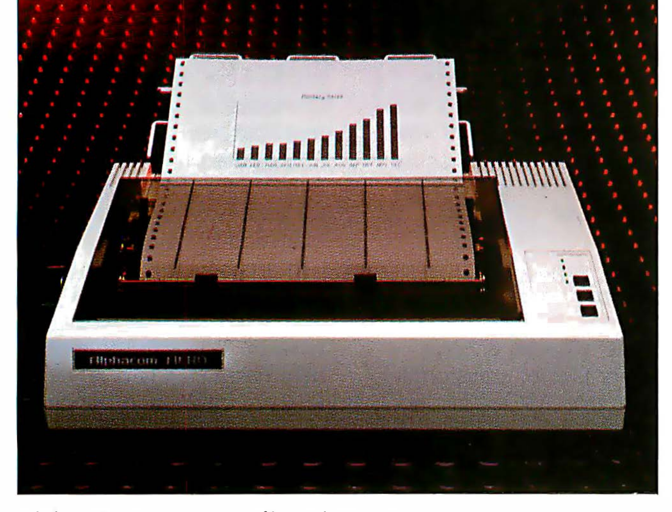
Standard with the system are color graphics (RGB and composite, both of which are compatible with the IBM graphics-display card) and a clock/calendar with battery backup. Software bundled with the system includes Micropro's WordStar, MailMerge, InfoStar, CalcStar, tutorials, and Microsoft's GW-BASIC interpreter.

The Kaypro 286i has a suggested list price of $4550. For more information, contact Kaypro Corp., 533 Stevens Ave., Solano Beach, CA 92075, (619) 481-4300.
Inquiry **603**.

130-cps Printer Is Compatible with Epson RX-80

The Aero from Alphacom is a 130-cps dot-matrix printer that's compatible with existing software and graphics supporting Epson's RX-80 series printing protocols. Alphacom has optimized the Aero's print speed with the inclusion of path-seeking logic and a 2K-byte buffer.

Aero produces the standard 96-member ASCII character set, and it lets you define up to 96 characters for custom applications. It forms 6- by 8-dot characters with true descenders in a 6- by 9-dot matrix grid using a 9-wire print head. The print head outputs either 480 or 960 dots per line in either alphanumeric or bit-image modes.



Alphacom's Aero is compatible with Epson's RX-80.

Manuscripts printed out on the Aero can display any mixture of superscripts, subscripts, double-strike, enlarged and emphasized type, underlining, text, and graphics on the same line. Aero will print out an original and three copies using perforated or regular-bond paper.

Indicators for power-on, on-line, paper-out, and ready are located on the top right side of the Aero along with its operator controls. Aero comes with a self-test feature, and it uses standard Epson ink cartridges.

RS-232C and Centronics-type parallel versions of Aero are available. The suggested retail is $249.95. Contact Alphacom Inc., 2323 South Bascom Ave., Campbell, CA 95008, (408) 559-8000.
Inquiry **604**.

Internal Hard Disk for PC AT

Control Data Corporation is now shipping a 30-megabyte hard-disk drive that fits inside IBM's PC AT. Called the StorageMaster 630, this drive has a typical access time of 30 milliseconds, which is reported to be approximately 25 percent faster than the native IBM drive.

The StorageMaster 630 uses the PC AT's resident disk controller and is shipped with adaptive software that lets you tweak it for operation with PC-DOS 3.0. The software gives you the ability to logically partition and format the disk, and includes diagnostic routines.

A pair of StorageMaster 630s can be tucked side-by-side within the PC AT's cabinet. Installing the StorageMaster 630 into the PC AT housing is said to require less than one hour.

Disk image or selected file-backup capabilities for the StorageMaster 630 are available through use of Control Data's 45-megabyte StorageMaster 745 ¼-inch cartridge streaming-tape backup system.

The suggested list price for the StorageMaster 630 is $2145. Contact Control Data Corp., 8100 34th Ave. S, POB 0, Minneapolis, MN 55440, (800) 328-3390.
Inquiry **613**.

ALL Card Allows 4 Megabytes RAM in IBM PC

ALL Computers' ALL Card AT1 features a custom CMOS memory-management unit (MMU) processor, in addition to other memory and interface enhancements, on a single IBM PC expansion card. The AT1 comes with a clock/calendar, a serial port, the MMU, and room for 1 megabyte of on-board memory using 256K-byte chips. You can add up to a total of 4 megabytes to the system.

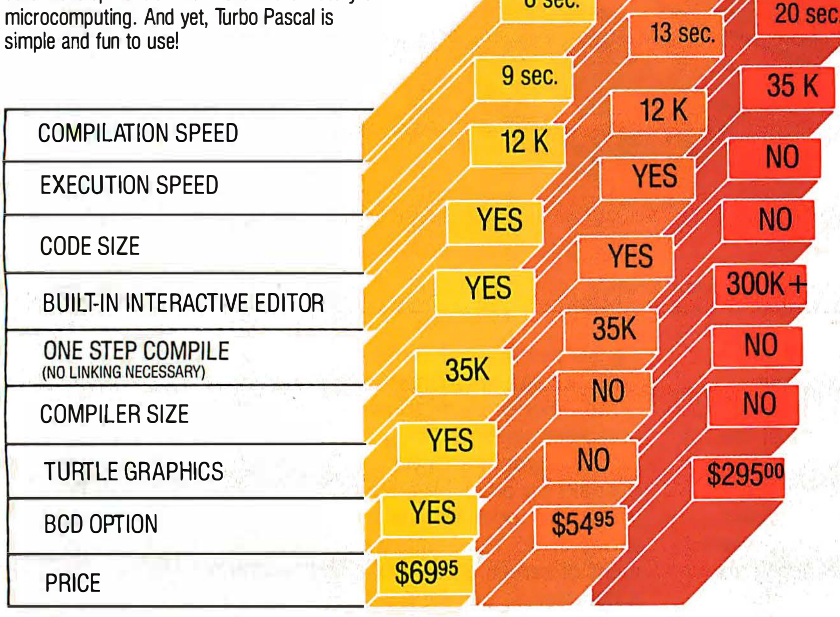
With 256K bytes of memory, the AT1 ALL Card is $1295. Without the MMU, it's $795. A version with neither memory nor the MMU is $395. Contact ALL Computers Inc., Suite 501, 110 Bloor St. W, Toronto, Ontario M5S 2W7, Canada, (416) 960-0111.
Inquiry **605**.

(continued)

They said it couldn't be done. Borland Did It. Turbo Pascal 3.0

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With more than 250,000 users worldwide Turbo Pascal is the industry's de facto standard. Turbo Pascal is praised by more engineers, hobbyists, students and professional programmers than any other development environment in the history of microcomputing. And yet, Turbo Pascal is simple and fun to use!



(*) **Benchmark** run on an IBM PC using MS Pascal version 3.2 and the DOS linker version 2.6. The 179 line program used is the "Gauss-Seidel" program out of Alan R. Miller's book: *Pascal programs for scientists and engineers* (Sybex, page 128) with a 3 dimensional non-singular matrix and a relaxation coefficient of 1.0.

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- And much much more.

The Critics' Choice.

Jeff Duntemann, PC Magazine: *"Language deal of the century . . . Turbo Pascal: It introduces a new programming environment and runs like magic."*

Dave Garland, Popular Computing: *"Most Pascal compilers barely fit on a disk, but Turbo Pascal packs an editor, compiler, linker, and run-time library into just 29K bytes of random-access memory."*

Jerry Pournelle, BYTE: *"What I think the computer industry is headed for: well documented, standard, plenty of good features, and a reasonable price."*

Portability

Turbo Pascal is available today for most computers running PC DOS, MS DOS, CP/M 80 or CP/M 86. A XENIX version of Turbo Pascal will soon be announced, and before the end of the year, Turbo Pascal will be running on most 68000 based microcomputers.

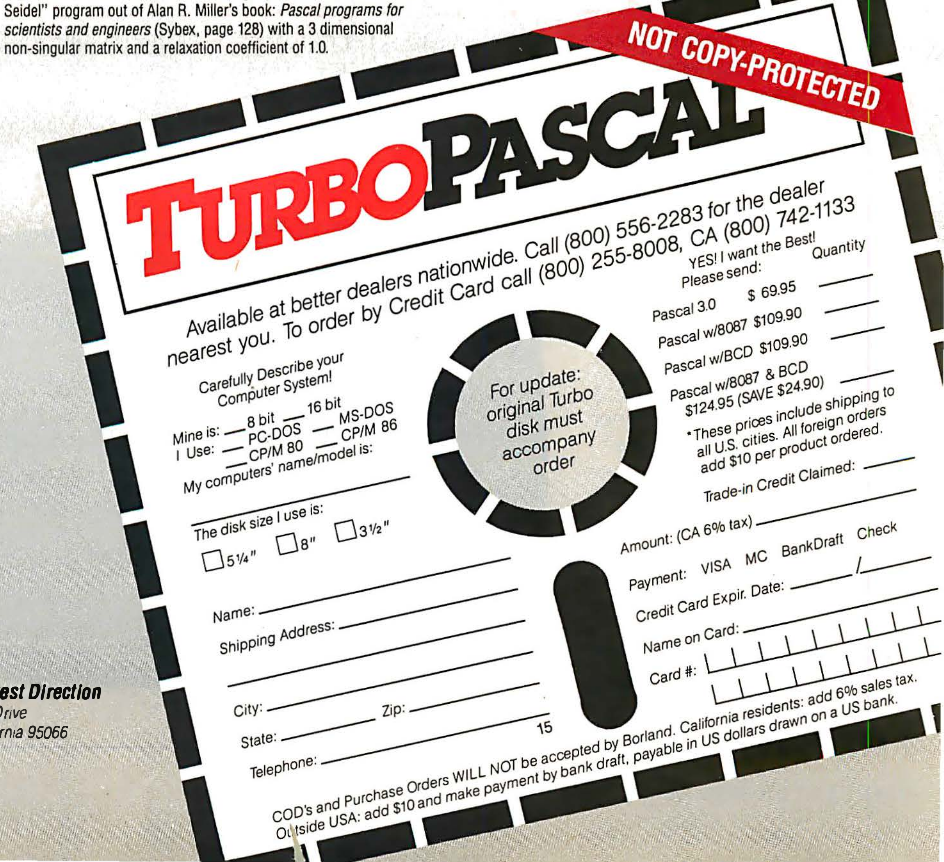
An Offer You Can't Refuse

Until June 1st, 1985, you can get Turbo Pascal 3.0 for only $69.95. Turbo Pascal 3.0, equipped with either the BCD or 8087 options, is available for an additional $39.95 or Turbo Pascal 3.0 with both options for only $124.95. As a matter of fact, if you own a 16 Bit computer and are serious about programming, you might as well get both options right away and save almost $25.

Update policy

As always, our first commitment is to our customers. You built Borland and we will always honor your support.

So, to make your upgrade to the exciting new version of Turbo Pascal 3.0 easy, we will accept your original Turbo Pascal *disk* (in a bend-proof container) for a trade-in credit of $39.95 and your Turbo87 original *disk* for $59.95. This trade-in credit may only be applied toward the purchase of Turbo Pascal 3.0 and its additional BCD and 8087 options (trade-in offer is only valid directly through Borland and until June 1st, 1985).



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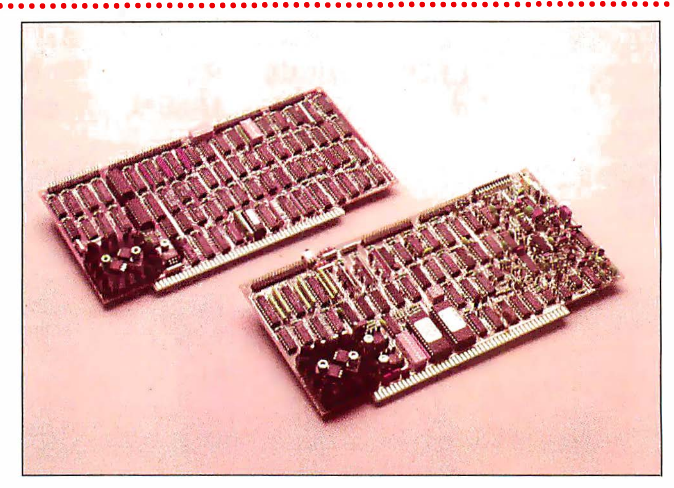
Inquiry 47

Turbo Pascal is a registered trademark of Borland International, Inc.

S-100 Graphics Cards Produce TV-Quality Images

The S-Series of color-graphics products lets you produce images to the maximum resolution of NTSC and PAL television standards on Cromemco's 68000-based S-100 computer systems. The S-Series comprises the previously announced SDD Color Digitizer Interface, plus four new S-100 (IEEE-696 standard) bus cards.

The SVID Color Video Generator Board works with the SDMA Video Memory Controller card to generate color images by panning over a virtual 1024- by 1024-pixel image. The NTSC version displays 756 by 484 pixels, while the PAL card set generates a 756- by 577-pixel image. Depending on graphics memory, up to 8 bits of data can be allocated per pixel to select up to 256 colors from a palette of 256,000.



S-Series color-graphics cards from Cromemco.

The 256KTP card comes with 256K bytes of two-ported memory; four 256KTP cards are required to take advantage of the full 1024- by 1024-pixel, 256-color capability of the S-Series. The SDCM Color Modulator Board converts red-green-blue signals to broadcast-type composite signals meeting either the NTSC or PAL standards.

The S-Series cards allow computer-generated or digitized graphics to be overlaid on other broadcast images. A zoom feature allows up to 4-to-1 enlargement of screen areas, while a pan feature can be used to move through the 1024 by 1024 image area either displaying edges or wrapping around to the opposite side of the image. Image input and output are possible using a wide range of devices: Any composite-video image can be digitized by the SDD card, while the other cards combine to provide output in RGB and NTSC and PAL composite-video formats.

The SVID video-generator board costs $795, while the SDCM modulator card is $995. Both are available in either NTSC or PAL versions. The SDMA controller board is $795, and each 256KTP memory card is $1995. The SDD digitizer card, for either NTSC or PAL versions, is priced at $995. Contact Cromemco Inc., 280 Bernardo Ave., POB 7400, Mountain View, CA 94039, (415) 964-7400.
Inquiry 606.

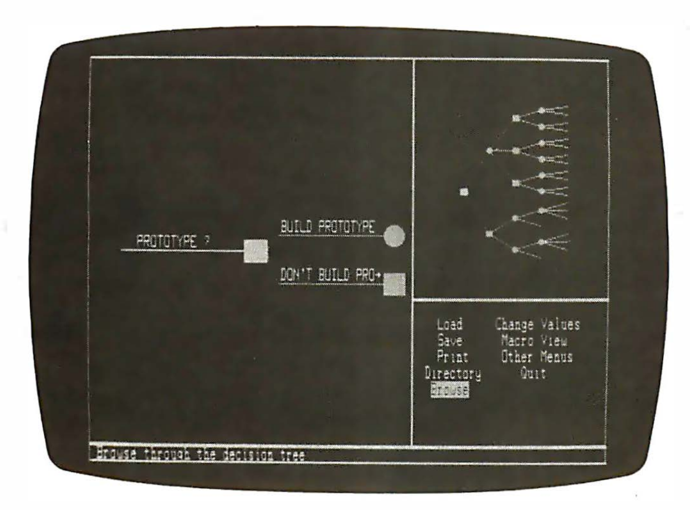
TI's Arborist, Decision-Tree Analysis Software, Supports IBM

Texas Instruments' Arborist, a decision-tree analysis software package, runs on both the TI Professional Computer and IBM's Personal Computer. Arborist brings quantitative decision-making techniques to planners using these desktop computers.

In decision-tree analysis, a series of multiple chance events and possible decisions is represented by a tree structure. If the planner can estimate the outcome and probability of each individual decision or event, Arborist can then determine the best choice at each decision point.

Arborist is intended primarily for people who have at least a basic understanding of decision-tree analysis. It uses a graphical display of decision-tree structures to aid in the decision-making process. The program accommodates color or monochrome displays and the 8087 numeric coprocessor.

Arborist sells for $595. For further details, contact Texas Instruments Inc., POB 80963, Dallas, TX 75380-9063, (800) 527-3500.
Inquiry 607.



A *decision tree created by* TI's *Arborist.*

XL/Serve for Macs

XL/Serve permits the Macintosh/XL (formerly the Lisa 2/10) to function as a disk and print server in an AppleTalk Personal Network. It lets distributed Macintoshes share disk storage and Imagewriter printers.

XL/Serve includes disk and printer software that runs concurrently on a host Macintosh/XL under MacWorks, driver software for individual Macintoshes, and a backup and restore utility.

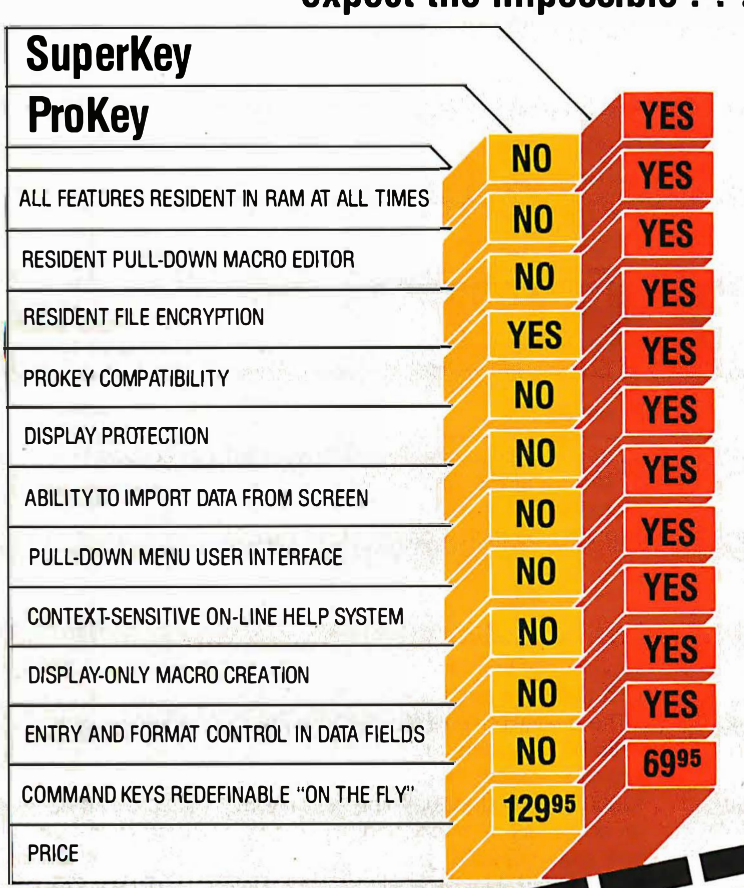
You can partition the host disk into individual volumes, and users can be granted read-only or read-write status.

XL/Serve is $200. Contact Infosphere Inc., 4730 Southwest Macadam Ave., Portland, OR 97201, (503) 226-3515.
Inquiry 608.

(continued)

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RESIDENT FILE ENCRYPTION	NO	YES
PROKEY COMPATIBILITY	YES	YES
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ABILITY TO IMPORT DATA FROM SCREEN	NO	YES
PULL-DOWN MENU USER INTERFACE	NO	YES
CONTEXT-SENSITIVE ON-LINE HELP SYSTEM	NO	YES
DISPLAY-ONLY MACRO CREATION	NO	YES
ENTRY AND FORMAT CONTROL IN DATA FIELDS	NO	YES
COMMAND KEYS REDEFINABLE "ON THE FLY"	NO	YES
PRICE	129.95	69.95

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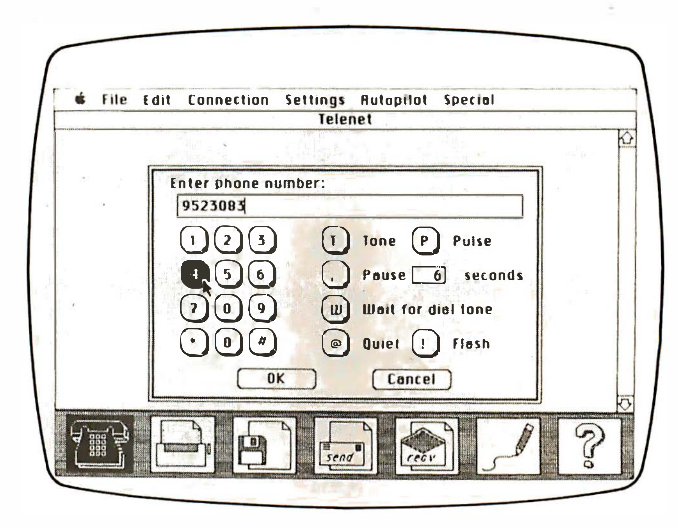
COD's and Purchase Orders WILL NOT be accepted by Borland. California residents: add 6% sales tax.
Outside USA: add $10 and make payment by bank draft, payable in US dollars drawn on a US bank.

Hayes Offers Smartcom II for the Macintosh

Hayes Microcomputer Products has announced Smartcom II for the Macintosh. The program, originally written for the IBM PC, has been redesigned to take advantage of the Macintosh graphical user interface.

Smartcom II is compatible with Hayes's existing standalone modems and with its recently introduced 2400-bps Smartmodem. Smartcom II can handle communications between computers in a hard-wired configuration at speeds of up to 19,200 bps.

Smartcom II has an "autopilot" feature that can be programmed to automatically perform such functions as logging onto remote systems, sending or receiving files, and performing database operations. It supports both the Hayes Verification Protocol and the XMODEM protocol for file transfers. It also lets you switch back and forth between voice and data during a communications session.



Smartcom II exploits the Mac's graphical user interface.

Hayes reports that the Smartcom II program will permit two Macintosh computers to exchange graphical images in real time using conventions similar to those in MacPaint. An image created on one screen is automatically reproduced on the remote screen. The second user can "take over" the drawing and make changes and additions.

The retail price for the Smartcom II software for the Macintosh is $149. For more information, contact Hayes Microcomputer Products Inc., 5923 Peachtree Industrial Blvd., Norcross, GA 30092, (404) 449-8791.
Inquiry 609.

Multiuser Board for IBM Based on 68000

The Multi-PC/68 from LinkData is a multiuser 68000 microprocessor board for the IBM Personal Computer. This two-board combination runs UNI-DOS, a DEC-like operating system that lets the PC run multiuser software written for the DEC PDP-11 family of minicomputers.

When equipped with Multi-PC/68, the IBM PC XT can support four terminals and run five concurrent programs written in the DIBOL or CADOL minicomputer languages. The IBM PC AT can support up to eight terminals and run nine programs. In addition, both the XT and AT can run MS-DOS applications concurrently with UNI-DOS applications.

The dealer price of the Multi-PC/68 system, including UNI-DOS, ranges from $2000 to $4000, depending on how much memory and how many RS-232C ports are included. LinkData will also make available to dealers a $200 DEC-like word processor, a series of accounting packages ($295 each), and a line of vertical-market applications packages with price tags spanning from $750 to $1000. For more information, contact LinkData, 2005 Route 22, Union, NJ 07083, (201) 964-6090.
Inquiry 610.

Harmony Comes to Mac

Harmony is a set of productivity tools that runs as a desk accessory on the 512K-byte Macintosh or as an application program on the 128K-byte Macintosh.

Harmony offers a full database in which each record can hold up to 18 information fields. Harmony has a time-manager module with a calendar, an appointment book with project-management features, a memo writer, and a print-spooler application that spools files from MacWrite and Microsoft Word.

Other features include a telecommunications application with auto-dial capabilities. Harmony can work in concert with Jazz from Lotus Development Corporation and other Macintosh programs. Intermatrix says that the program will be available in mid-April and that it will be priced at $195. Contact Intermatrix, 5547 Satsuma Ave., North Hollywood, CA 91601, (818) 509-0474.
Inquiry 611.

Harris Announces PC Network/File Server

The Harris 9300 network/file server can link up to 16 IBM PC-compatibles, 3270 terminals, Harris PCs, or printers with a high-capacity hard-disk drive and a local-area network.

Devices are linked by a coaxial cable with a data-flow rate of 1 megabit per second. The 9300 uses an 80286 chip for network processing and supports up to 80 megabytes of hard-disk storage and 2 megabytes of memory. An optional Z80B runs word-processor and office-automation programs developed by Lanier, a subsidiary of Harris.

The system with 1 megabyte of memory, 37 megabytes of hard-disk storage, and hardware for connection to the network is about $11,000. Adapter cards for personal computers are $1050 each. Deliveries are expected to begin in June. Contact Harris Corp., Melbourne, FL 32919, (305) 727-9100.
Inquiry 612.

(continued on page 440)

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Jeff Duntemann, PC Magazine: *"Language deal of the century . . . Turbo Pascal: It introduces a new programming environment and runs like magic."*

Dave Garland, Popular Computing: *"Most Pascal compilers barely fit on a disk, but Turbo Pascal packs an editor, compiler, linker, and run-time library into just 29K bytes of random-access memory."*

Jerry Pournelle, BYTE: *"What I think the computer industry is headed for: well documented, standard, plenty of good features, and a reasonable price."*

Portability. Turbo Pascal is available today for most computers running PC DOS, MS DOS, CP/M 80 or CP/M 86. A XENIX verison of Turbo Pascal will soon be announced, and before the end of the year, Turbo Pascal will be running on most 68000 based microcomputers.

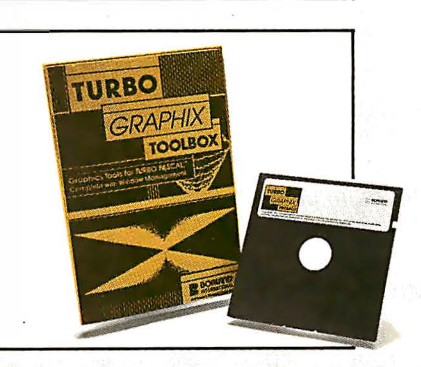
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Jerry Pournelle, BYTE: "The tools include a B+tree search and a sorting system; I've seen stuff like this, but not as well thought out, sell for hundreds of dollars."

Get started right away: free database! Included on every Toolbox disk is the source code to a working data base which demonstrates how powerful and easy to use the Turbo-Access system really is. Modify it to suit your individual needs or just compile it and run.

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Turbo Graphics	$ 54.95	____
Turbo Tutor	$ 34.95	____

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Carefully Describe your Computer System!

Mine is: — 8 bit — 16 bit
I Use: — PC-DOS — MS-DOS — CP/M 80 — CP/M 86

My computers' name/model is: ____

The disk size I use is: ☐ 5¼" ☐ 8" ☐ 3½"

Name: ____
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City: ____
State: ____ Zip: ____
Telephone: ____

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Inquiry 49



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With IBM's new Personal Decision Series, you start with *Data Edition*, adding others, like *Reports+* or *Plans*, as you like.

For even more help, you can add *Appoint-*

Conducted by Steve Ciarcia

Elementary Information

Dear Steve,

Can you tell me where I can get specific and in-depth answers to elementary questions about computers and electronics? I know that you answer questions, but I also know that you couldn't be expected to give very lengthy answers to my beginner's questions.

Charles F. Porter
Cedar Rapids, IA

The Ask BYTE column addresses hardware-related questions of general interest but is not meant for the beginner. BYTE's sister publication, Popular Computing, *caters to a less technical audience, and its Ask Popular column addresses questions related to computers in general. Both publications may answer your specific question, but the turnaround time is lengthy.*

If you need specific answers to specific questions in a reasonable amount of time, try a local computer club. There is usually an "expert" available on almost any topic. Failing that, the local bookstore will feature many books on computers and computer-related material.—Steve

S-100 Switching Supply

Dear Steve,

Will you be doing an article on a switching power supply for the S-100 bus?

I hear that switching supplies are less expensive to build than linear supplies; the selling prices I have seen are not less. Could Micromint offer a power-supply kit for this purpose?

Ernest A. Knipp
Houston, TX

A switching power supply for S-100–type computers is a good idea, and I will consider it for a future article.

The cost of switching-type power supplies is usually less than linear-regulated supplies of comparable power because smaller capacitors and inductors are used and can be packaged in a smaller volume. They also generate less heat and are easier to cool, resulting in a lower overall installed cost.

If you want to build your own switching supply, my article in the November 1981 BYTE provides the basics. "Switching Power Supplies: An Introduction" covers the fundamentals of design and describes a workable unit. This article isn't a do-it-yourself S-100 power-supply project, but it should give you most of the basics.

Several ±12-V, 5-V switching supplies are available commercially, including the MPX-10 (from Micromint, 561 Willow Ave., Cedarhurst, NY 11516), which powers the MPX-16 computer. Others are available from Kepco Inc., 131-38 Sanford Ave., Flushing, NY 11352; Lambda Electronics, 515 Broad Hollow Rd., Melville, NY 11747; and Sorensen, 676 Island Pond Rd., Manchester, NH 03103.—Steve

Graphic-Arts Computer

Dear Steve,

I would like to do graphic-arts work with a computer capable of producing a minimum of about 800 by 800 pixels and at least 100 simultaneously displayable colors. I have seen ads for various color boards or dedicated graphics computers, but they either don't match my specs or they are too expensive.

I'd like to build my own color add-on board for the Commodore 64 or a complete computer. I'd appreciate any suggestions.

Les Kohuth
Syosset, NY

High-resolution graphics systems are expensive and seem overpriced in comparison to the graphics systems available on microcomputers. To understand this high cost, let's look at the components of a high-resolution graphics system.

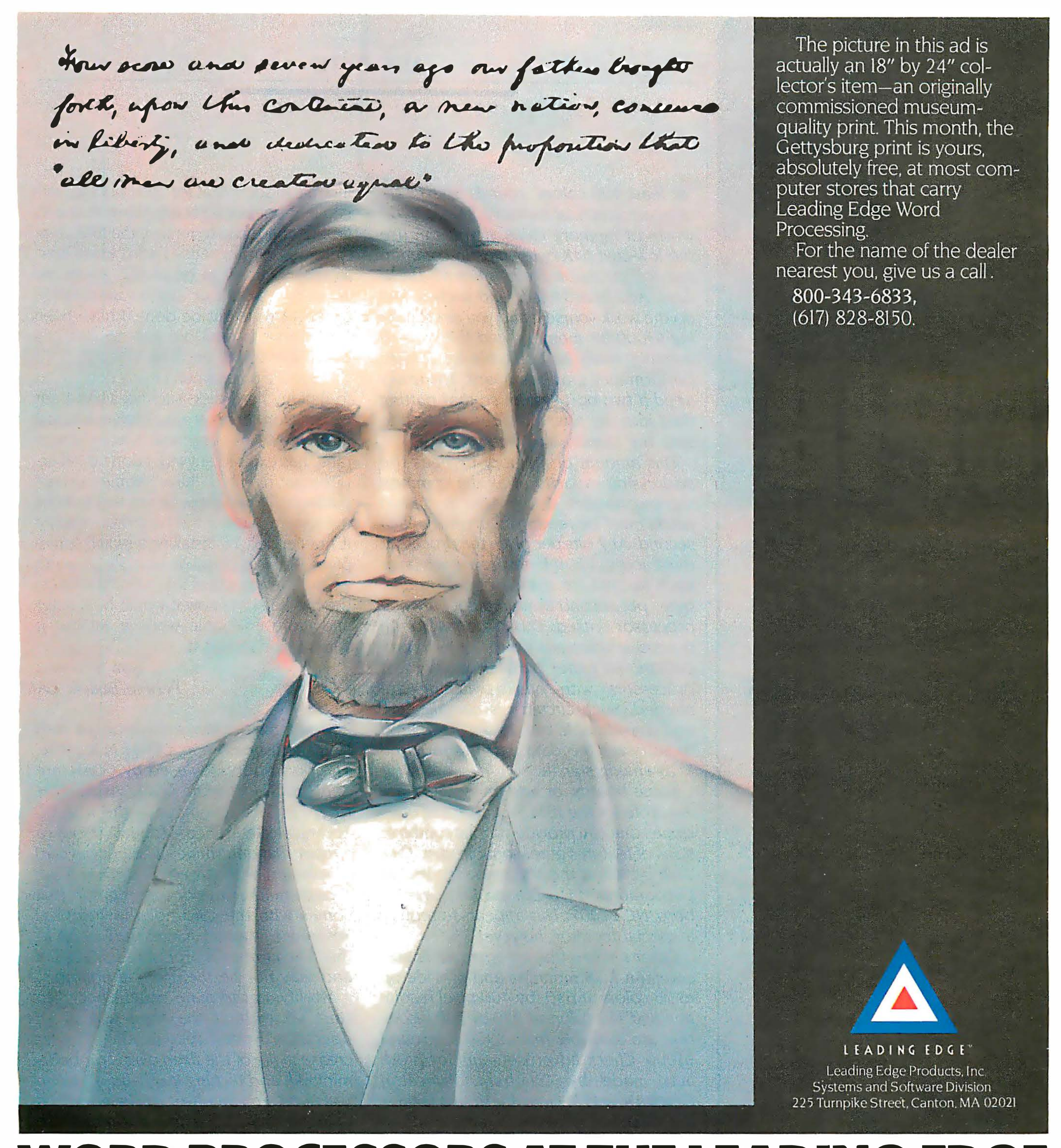
To display the resolution that you mentioned, a monitor with a video bandwidth of at least 18 to 20 MHz is needed to distinguish individual pixels, or dots. This requirement can be understood if we look at the makeup of one scan line of the picture.

The normal scan rate is 15,750 scans per second, and at 800 pixels of horizontal resolution, this is 12,600,000 pixels per second. However, the case where all the pixels are lit results in a zero-bandwidth requirement, and a DC voltage is all that is required. In the worst case, when every other pixel is lit, a clear display of 6 million pixels per second is needed. This appears to require only a 6-MHz bandwidth, but bandwidth is usually defined as the frequency where the signal (or gain) is reduced by 3 dB, or 50 percent of the normal level. Such a bandwidth would result in low brightness and contrast in picture areas where fine detail is shown. To display sharp images at this resolution, it is necessary to approximate a square wave at 6 MHz, and the first component of a square wave above the fundamental is the third harmonic, or 18 MHz. This is the minimum acceptable, and a noticeable improvement should be seen if the bandwidth is extended to the next component, which is the fifth harmonic (30 MHz).

The standard television sweep frequencies generate 525 horizontal lines per frame in two vertical scans (interlaced). A limit of about 400 lines within this region is required for good linearity. Most microcomputer graphics systems provide 200 or so lines by using the so-called noninterlace mode, displaying the same information on adjacent pairs of lines. This can be doubled by using twice as much memory and reprogramming the video controller. Getting to 800 lines requires twice as many horizontal sweeps per frame (and half the frame rate), which is not within the capabilities of the popular $500 RGB monitors. Monitors of this type are available, but the prices are in the several-thousand-dollar range.

800 by 800 pixels requires 640K bits, or about 80K bytes, of memory to give one color (we get black for free). If you want to be able to assign different colors to each pixel, rather than define characters within a block of 8 by 8 contiguous pixels, the memory is arranged in layers. One 80K-byte layer gives black and white, two layers doubles this to four colors (three colors plus black), another layer doubles again, etc., for as many colors as we want, or can afford. Your spec of

(continued)



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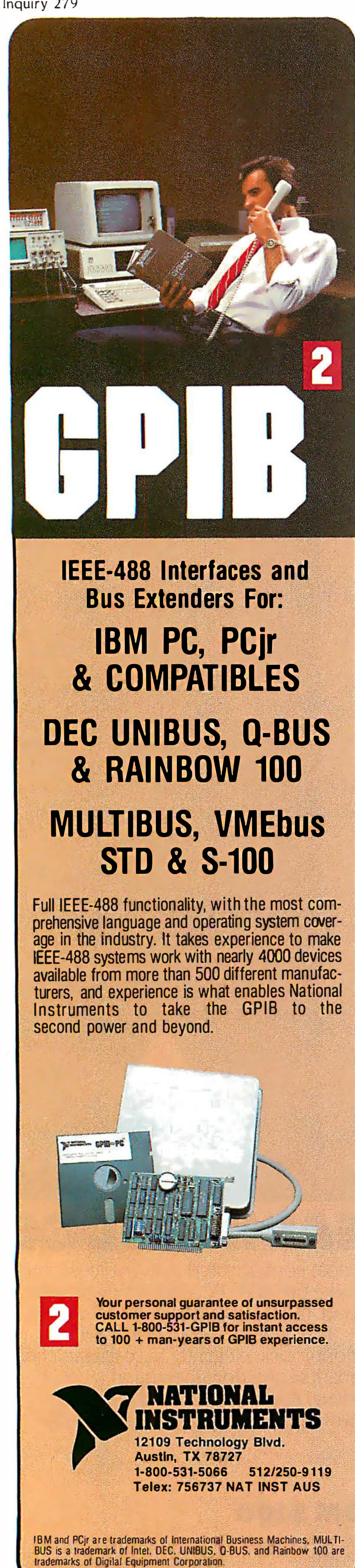
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Inquiry 279



"at least 100 colors" rounds up to 128, or seven layers of memory. This is $700 worth of memory chips, if you can use the low-cost 64K-byte chips in common use for microcomputer memory these days. Add board space and sockets and do the work yourself, and you're still talking $1000 for memory, and this type of memory really isn't suitable for a high-performance graphics board. You really need a two-port system so that putting data into the memory doesn't interfere with the display and vice versa.

This amount of memory exceeds the addressing capacity of all the common video-controller chips. Also, 6 million pixels must be read from memory each second. At 7 bits per pixel, the processor must access 750K bytes from each layer each second, or a total of 5.25 megabytes per second throughput if only one processor is used. This is too fast for inexpensive video processors, or microprocessors, so either parallel or very fast processors with bank switching are needed. Such circuitry is complicated, and considerable processing is required to separate the data into the required RGB analog signals.

Some boards, or add-on systems, are available for the IBM PC and some of its clones that can provide various combinations of features at reasonable cost. One such system is the VX, made by Vectrix Corporation, 1416 Boston Rd., Greensboro, NC 27407. This appears to require a special monitor, however.

Other systems that are compatible with common RGB monitors and provide up to 16 colors at 640- by 400-pixel resolution and 132 colors at 320 by 200 resolution are available from $300 to around $1000. Check advertisements for products made by Quadram, Princeton Graphics, and Tecmar Inc. in magazines like BYTE to find some that might represent a satisfactory compromise. Another good source for information on this subject is Electronic Imaging *magazine.* —Steve

Reconfiguring the PC XT

Dear Steve,

I have two questions that I would like to have answers for. They both relate to the IBM PC XT. After devouring your most interesting articles and answers in BYTE, I believe you can answer them.

The XT comes equipped with an asynchronous communications card configured as COM1. I have installed a Hayes internal modem that for compatibility with some important software I have to use as COM1. I have had to remove the IBM asynchronous card because I don't know how to reconfigure it to be COM2. There are no switches on it or any documentation on how this might be done. I have been told that it is possible, but no one has been able to tell me how to do it.

There are times when I really don't need to use my hard disk, such as when I am working for hours on a mainframe and just using my XT as a terminal. Since my warranty has expired anyway, I don't mind experimenting if I have some expert guidance. Would there be any way to boot my system without the hard disk, when it is not needed, by installing a switch someplace? If this is possible, would it be worth saving a few hours of idle running time on the hard disk? I know it would be quieter and more enjoyable working without it when I don't need it.

Bob Stephan
Pebble Beach, CA

Modifying the IBM asynchronous card to make it operate as COM2 is feasible. The port addresses used by COM1 are 3F8H to 3FFH, while COM2 uses 2F8H to 2FFH. The schematic in the IBM PC Technical Reference Manual *shows a jumper that determines whether the card is selected with A8 equal to 0 or 1, although neither the documentation that comes with the card nor the* Technical Reference Manual *makes reference to this. The jumper is probably soldered in and may not be there on all boards.*

Modifying the main system board to start up without the fixed disk is an operation I don't recommend. The increase in life of the fixed disk is probably minimal, and turning it on and off when you need it might offset any gain realized by not running it full time. I also suspect, based on my experience with IBM PCs, that the fan makes as much noise as the disk, so there is little to be gained.—Steve

Reading Latch Outputs

Dear Steve,

I have a Sinclair 1000 that I'm trying to use in a security system. In my system, octal latches monitor infrared beams. When a beam is broken, my program addresses a latch at an address above RAM and uses a POKE to put a 1 in the latch to ring the bell. This works fine. The problem is when I try to check the octal latches

(continued)

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Inquiry 356

ASK BYTE

with the PEEK command, instead of seeing the latch, it reads garbage. I have tried addresses just above RAM all the way up to address 65535, and I still read garbage.

It appears that when you check an address that is above RAM it mirrors back to a RAM or ROM address. Can you tell me how I can address and see my octal latches instead of mirroring back to RAM? Thanks for your help.

DAN GROGAN
San Pedro, CA

It appears that your Sinclair 1000 is not reflecting your PEEK commands back into low memory. As I interpret your letter, you have a set of latches that are supposed to put data on the bus to tell the computer that a detector has been tripped, and you are having trouble reading the latch outputs.

Are you sure that the address decoder on the latch board is set to the address to which you are writing? Is it properly timed to put the data on the bus at the right time or hold it there long enough to be recognized by the processor? The fact that you can write a bit into the bell latch seems to indicate that you are able to address the high memory, but the timing in writing data into the latch could be a lot less critical than reading data.

Have you looked at the signals at the latch outputs and on the data bus to be sure that they are putting out the correct voltage levels? How about signal quality? The level is fairly easy to get with TTL or CMOS chips if the power-supply voltage is at the required 5 volts, but if the wiring connecting the latches to the computer bus isn't properly dressed, you can do horrible things to the normally clean square waves put out by the latches. —Steve

A/D FOR Z-100

Dear Steve,

I have a Zenith Z-100 computer with two disk drives and with 192K bytes of memory. Now I am thinking of providing an A/D interface for the serial input so that I can feed in analog signals from various instruments, such as a spectrophotometer, pH meter, etc. Looking through the journals I located a few suppliers, though mostly of rather fancy multichannel data-acquisition units I do not need. At the most, I need four channels of input without any specialties attached. I would appreciate it if you could let me know of any

(continued)

such units on the market.

HERBERT JONAS
St. Paul, MN

Analog Devices (2 Technology Way, Norwood, MA 02062, (617) 329-4700) makes the μMAC-4000 series data-acquisition systems that provide up to 12 channels of 13-bit A/D input/output and serial communication, priced at $995 and up.

Two other units that interface through RS-232C are the 16-channel, 12-bit ADC-1 from Remote Measurement Systems Inc., POB 15544, Seattle, WA 98115, (206) 525-3369. It's advertised at $369. Also available is the BUSSter D16 8-bit, 16-channel unit from Connecticut microComputer. The address is 36 Del Mar Dr., Brookfield, CT 06804, (203) 775-4595.

All three of the above units accept digital inputs as well as analog.

Since your Z-100 uses the S-100 bus, you might also want to consider the plug-in AIM-12 S-100 board from Dual Systems Corp., 2530 San Pablo Ave., Berkeley, CA 94702, (415) 549-3854. This unit provides for 16 channels of input with 12-bit conversion, priced at $775. —Steve ■

Between Circuit Cellar Feedback, personal questions, and Ask BYTE, I receive hundreds of letters each month. As you might have noticed, at the end of Ask BYTE I have listed my own paid staff. We answer many more letters than you see published, and it often takes a lot of research.

If you would like to share the knowledge you have on microcomputer hardware with other BYTE readers, joining the Circuit Cellar/Ask BYTE staff would give you the opportunity. We're looking for additional researchers to answer letters and gather Circuit Cellar project material.

If you're interested, let us hear from you. Send a short letter describing your areas of interest and qualifications to Steve Ciarcia, POB 582, Glastonbury, CT 06033.

IN ASK BYTE, *Steve Ciarcia answers questions on any area of microcomputing. The most representative questions received each month will be answered and published. Do you have a nagging problem? Send your inquiry to*

Ask BYTE
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Due to the high volume of inquiries, personal replies cannot be given. All letters and photographs become the property of Steve Ciarcia and cannot be returned. Be sure to include "Ask BYTE" in the address.

The Ask BYTE staff includes manager Harv Weiner and researchers Bill Curlew, Larry Bregoli, Dick Sawyer, and Jeannette Dojan.

 Inquiry 151

Now Showing In Black And White

If you own an IBM-PC or PC work-alike, Roland's new MB-142 monitor lets you show off your text and graphics in today's hottest colors—black and white. That's right! The MB-142 gives you black characters on a paper-white background—just like people have been reading for centuries. You can also have white characters on a black background with just the touch of a button.

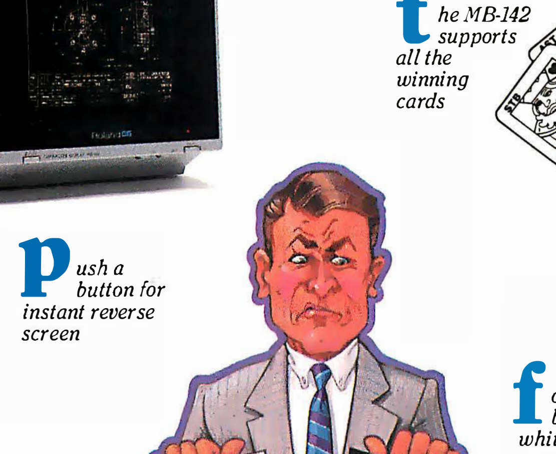
Both of these black and white display formats are easier on the eyes and less fatiguing than the green or amber phosphor used in standard monochrome monitors. The MB-142's large 14-inch screen, combined with its ultra-high 720 x 350 resolution, can display characters that are larger and more legible than what you can get with ordinary monochrome monitors. Another great plus is that the MB-142 plugs directly into the monochrome board of your IBM or compatible—just like your present monochrome monitor, with nothing more to buy.

Because of the MB-142's advanced electronic circuitry, you even have the ability to mix graphics and text on the same display when using graphics and text boards from leading manufacturers such as Persyst, STB, Paradise, Hercules, AST and many others. What makes it all possible? The same sophisticated technology used in color monitors.

Roland DG
CHARACTER DISPLAY MB-142

Actual screen image

MODEL
MB-142



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The MB-142 supports all the winning cards

For business, black and white makes more sense than green and black

The big difference is that the MB-142 monitor does the job for significantly less money. The MB-142 is designed to interface economically, too. Imagine seeing your favorite business graphics or CAD/CAM packages, such as Lotus 1-2-3, Energraphics, Chart-Master, AutoCAD, CADDraft and VersaCAD, in ultra-high resolution black and white. Also, take full advantage of your program's windowing capability using the large 14-inch screen.

Take a good look at the differences that set the MB-142 apart from the rest. No other monochrome monitor gives you the fatigue-free black and white viewing, text and graphics capabilities and easy interface.

Naturally enough, the MB-142 is from Roland DG—the new computer peripherals company that's pointing the way to the future. Look for this and other Roland products at fine computer dealers everywhere.

For more information, contact: Roland DG, 7200 Dominion Circle, Los Angeles, CA 90040. (213) 685-5141.

The software programs listed are trademarks of the following companies: AutoCAD, AUTODESK, Inc.; CADDraft, Personal CAD Systems, Inc.; Chart-Master, Decision Resources, Inc.; Energraphics, Enertronic Research, Inc.; Lotus 1-2-3, Lotus Development Corp.; VersaCAD, T&W Systems, Inc.

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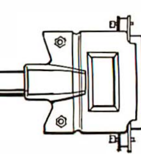
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Inquiry 146

● FUTURE INTELLIGENCE
A monthly newsletter devoted to tracking future computing technologies emphasizes research and business. Areas covered include artificial intelligence, supercomputers, parallel processing, expert systems, natural language, and voice/speech/pattern recognition and synthesis. An annual subscription is $295. Contact Ed Rosenfeld, *Intelligence*, POB 20008, New York, NY 10025.

● BASED IN THE BAY
A nonprofit users group for Sanyo computerists, the Bay Area Sanyo Enthusiast (BASE) welcomes anyone interested in computers. Regular meetings are held. Contact Lee Swearingen at (813) 788-7865 or Dave Robbins at (813) 886-7751 or write BASE, POB 260517, Tampa, FL 33685.

● CHUGGING ALONG
The Capitol Heath Users Group (CHUG) meets on the third Monday of every month at the Fairfax High School in Virginia. Members operate two 24-hour bulletin boards at (703) 759-2072 and (703) 360-3812. CHUG sponsors an annual conference, houses special-interest groups, and produces a monthly newsletter, *CHUG*, which is included in the annual $12 membership fee. Call John Roach in the evening at (703) 971-4930 or write CHUG, POB 10515, Alexandria, VA 22310.

● STANDARDS' BBS
The National Bureau of Standards' (NBS) Institute of Computer Sciences and Technology (ICST) has established a BBS at (301) 948-5718. Open to the public, its purpose is to exchange information that assists federal agencies in the efficient selection of software and hardware. Among topics discussed are security and interfacing. For details on the project, contact Ted Landberg at ICST, NBS, 225 Room #A266, Gaithersburg, MD 20899, (301) 921-3485.

● JOIN CP/M EFFORT
CP/M SIG assists members in the technical aspects of CP/M and related software through monthly meetings, a monthly newsletter, and a 24-hour RCP/M system at (303) 465-1313. Article submissions are welcome, public-domain software is available, and lectures educate members on areas of interest. Discounts on hardware and software and a subscription to the newsletter are provided with payment of $12 a year. Contact CP/M SIG Inc., POB 633, Broomfield, CO 80020-0633.

● GERMAN MAC RULES
At least once every two months, members of Clubmac (Europe) submit an article to the newsletter on anything about the Mac or their membership is not renewed. The result is a newsletter that keeps members up to date with latest developments, reviews new programs and hardware, and solves members' computing problems. The annual membership fee is £25 per annum. Contact K. Leslie, Clubmac, Triererstrasse 8, D-5511 Wincheringen, West Germany.

● BCS GOES REGIONAL
The Monadnock Region IBM PC Users Group, a subgroup of the IBM PC Users Group of the Boston Computer Society (BCS), gathers in Keene, New Hampshire, to see demonstrations and meet with other users. By joining, you benefit from a software exchange, group-purchase discounts, a monthly newsletter, and automatic BCS membership with access to the BCS BBS. Contact Susy Thielen, 45 Kelleher St., Keene, NH 03431, (603) 352-0971.

● CALL THE AMATEURS
The bulletin board of the New York Amateur Computer Club (NYACC) is up and running. The bimonthly newsletter contains NYC users group meetings and contacts, a NYACC directory, events, articles, letters, and news. Meeting times and locations of several users groups are announced on a hotline at (212) 864-4595. The membership is $15 annually; students pay $10. Write the NYACC, POB 106, Church Street Station, New York, NY 10008.

● DOWN UNDER THE TRS-80—Members of the Sydney TRS-80 Users Group (SYDTRUG) share knowledge about hardware, software, and education, business, and related applications for TRS-80 computers. Communication occurs through the monthly newsletter containing news and reviews, plus lectures, demonstrations, and the 24-hour BBS (CLUB-80) in Australia on (02) 332-2494. The BBS features messages, group news, and the exchange of public-domain software. Meetings are held on the second and third Saturdays of each month in Botany, New South Wales. Write SYDTRUG, POB 43, Erskineville 2043, New South Wales, Australia, tel: (02) 772-2009.

● ENGINEERS ANALYZE STRUCTURE—The Structural Analysis Programs Association (SAPA) upgrades the skills of engineers who use microcomputers to analyze and design buildings. Structural software and computer services that address this issue are discussed in the quarterly newsletter, *SAPA NEWS*, and in seminars held one full day in eight-month intervals. The annual membership fee is $100. Contact J. Jeff Davies, SAPA, Suite D2, 30 Southeast Seventh St., Boca Raton, FL 33432, (305) 392-6597.

● BBS IN FOX RIVER FORMS CLUB—Simplified Computer Solutions in Wisconsin has helped to form the Green Bay/Fox River Valley's bulletin-board service, SCS ABBS. The SCS Users Group evolved from the BBS and provides members with access to a library, group purchasing,

(continued)

CLUBS & NEWSLETTERS *is a forum for letting BYTE readers know what is happening in the microcomputing community. Emphasis is given to electronic bulletin-board services, club-sponsored classes, community-help projects, and other activities. We will continue to list new clubs and newsletters. Allow at least four months for your club's mention to appear. Send information to BYTE*, Clubs & Newsletters, POB 372, Hancock, NH 03449.

conferencing on the BBS, and a monthly newsletter. The annual dues are $10. Contact Don Sanderfoot, SCS, 2175 Wildwood Dr., Little Suamico, WI 54141.

● BUSINESS BBS

The Tulane University Business Bulletin Board (TUBBB) system combines business researchers, faculty, alumni, and students on line to share ideas, data, and programs. Contact John Page, A. B. Freeman School of Business, Tulane University, New Orleans, LA 70118.

● JOIN LONE STAR

The Lone Star Computer Club of Racine, Wisconsin, a group of users of all kinds of computers, meets at 7:30 p.m. on the second Thursday of each month at the Douglas Avenue Park Community House. The monthly newsletter, *President's Newsletter*, combines articles, software reviews, regular features, and library and system notes with applications. Contact H. S. Kanecki, Lone Star Computer Club, POB 93, Kenosha, WI 53140.

● VICTOR 9000 IN NW

The Victor 9000 Users Group serves users in Oregon and southern Washington state by meeting regularly to discuss the merits of the Victor 9000 business computer. A monthly newsletter, discount purchases, software demonstrations, and support for new users are group benefits. Contact Alan Bergen, 11765 Southwest Ebberts Court, Beaverton, OR 97005.

● KAYPRO IN BALTO

The Kaypro Users of Baltimore (KUB) meet at 7:30 p.m. on the first and third Wednesdays of every month at Loch Raven Middle School in Baltimore, Maryland. *The Bear Facts Newsletter* contains further information. The annual fee is $12 and requires a blank disk as an initial contribution. Newsletter subscriptions are an additional $6. Write KUB, POB 23510, Baltimore, MD 21203.

● ZORBA IN U.S.

The Zorba Equipment Users Society (ZEUS), a source of information and support for Zorba owners nationwide, maintains a public-domain library. The newsletter, *Oracle of Zeus*, is produced six times a year on disk and contains up to 30 files of relevant information. The $25 annual membership fee covers a subscription to the newsletter. Contact Randy Brook, ZEUS, POB 1112, Athens, OH 45701.

● EXPLORING THE STARS

Users of MicroPro's WordStar and InfoStar can subscribe to two Stargazer newsletters, *Exploring WordStar* and *Exploring InfoStar*. Designed to unlock the potential of the programs, they supply information for solving application questions and clarifying documentation through a practical, hands-on approach. Members are encouraged to submit articles and can benefit from group-purchase discounts. Subscriptions are $24 annually per newsletter or $40 for both. Contact HI-Tech, Department B, 4 Harwood Dr., Glen Cove, NY 11542.

● MAC GETS TECHNICAL

A Macintosh Programming Journal, *MacTech*, reviews software development and programming exclusively for the Mac. Each month articles written by a panel will build on previous columns, enhancing readers' understanding of how to best apply Macintosh software technology. The subscription rate is $24 a year. Contact *MacTech*, POB 846, Placentia, CA 92670, (714) 993-9939. ■

THE SIMPLE APPROACH IS THE SYMBOL APPROACH.

```
10 S=0
20 FOR I=1 TO 100
30 INPUT X
40 IF X = 0 GOTO 70
50 S=S+X
60 NEXT I
70 PRINT S/(I-1)
```

BASIC
A program to calculate averages...

```
      REAL X(100)
      READ*,N,(X(I),I=1,N)
      S=0
      DO 10 I=1,N
10    S=S+X(I)
      PRINT *,S/N
      END
```

FORTRAN
just shrunk from seven lines...

```
(+/X)÷ρX←⎕
```

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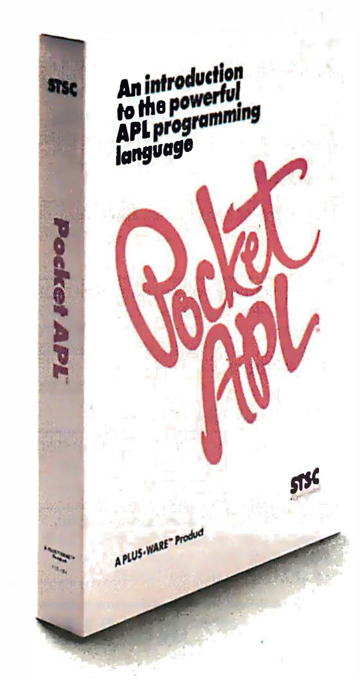
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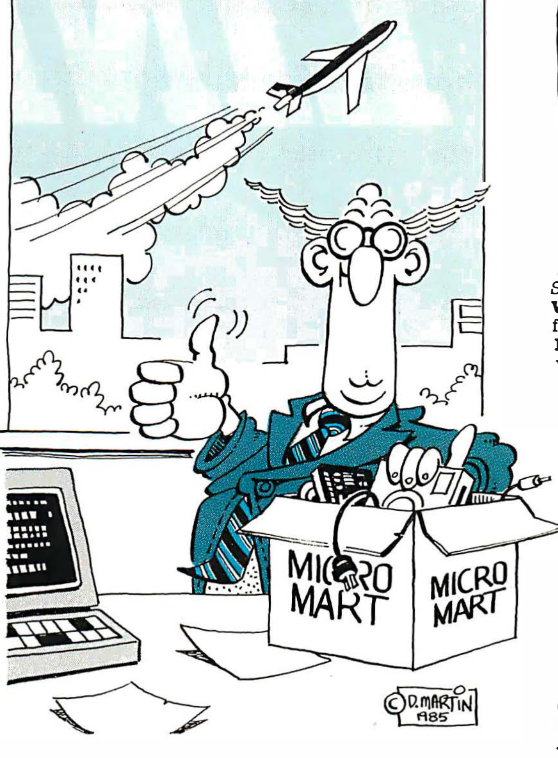
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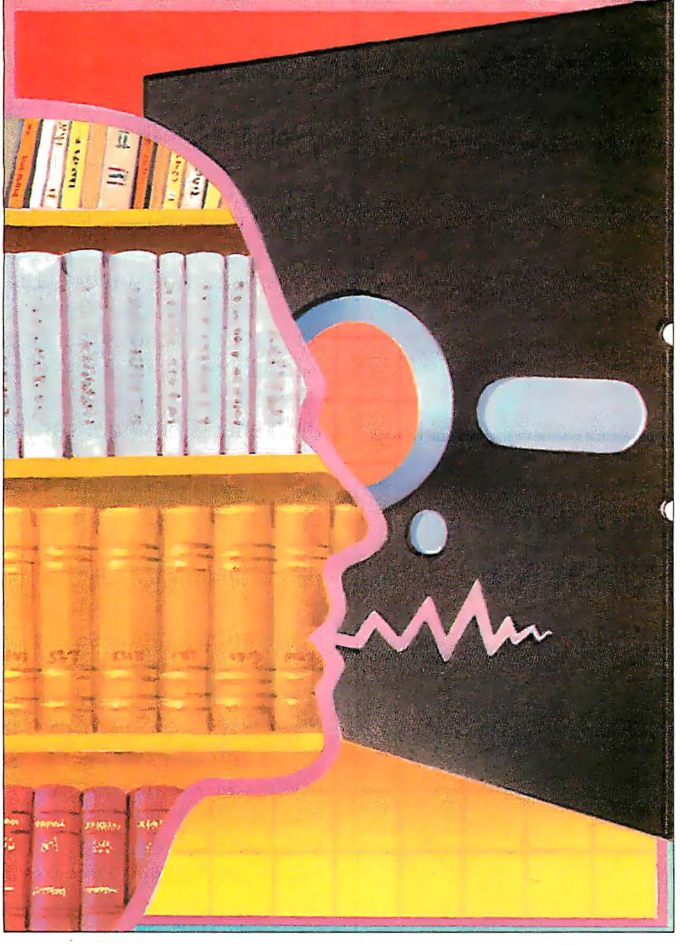
BUILD YOUR OWN EXPERT SYSTEM
Chris Naylor
John Wiley & Sons
New York: 1985
246 pages, $13.95

ARTIFICIAL INTELLIGENCE IN BASIC
Mike James
Focal Press
Stoneham, MA: 1984
122 pages, $14.95

THE COGNITIVE COMPUTER: ON LANGUAGE, LEARNING, AND ARTIFICIAL INTELLIGENCE
Roger C. Schank
with Peter G. Childers
Addison-Wesley
Reading, MA: 1984
282 pages, $17.95

BUILD YOUR OWN EXPERT SYSTEM

Reviewed by Ramachandran Bharath



An increasing number of comprehensive introductions to expert systems—computer programs that emulate the decision making of human experts—have been published recently. Two examples are *Building Expert Systems* by Frederick Hayes-Roth (Reading, MA: Addison-Wesley, 1983), and *A Practical Guide to Designing Expert Systems* by Sholom M. Weiss and Casimir A. Kulikowski (Totowa, NJ: Rowman and Allanheld, 1984).

But the object of Chris Naylor's book, *Build Your Own Expert System* (originally published in the United Kingdom in 1983), is to help home computer users write expert systems that learn.

John F. Sowa, author of *Conceptual Structures: Information Processing in Mind and Machine* (Reading, MA: Addison-Wesley, 1983), groups expert systems into three categories based on the kinds of problems they address: classification (such as diagnosis of disease), design (of chips, for example), and decision support. Naylor's book is aimed essentially at teaching readers about classification problems.

Naylor begins with a good discussion of the general advantages and limitations of current expert systems. He follows this with a chapter on statistical and probability theories; he provides the essentials of elementary probability theory and discusses revising initial estimates of probabilities in light of relevant additional information. (The technique for such revision of initial estimates is known as Bayes' theorem.) Naylor introduces these concepts extremely well by relating them to an expert system the reader might want to build: a program for forecasting weather using information on current conditions of fog, humidity, temperature, etc.

After providing this background, the author leads the reader through the process of developing a general BASIC program that can solve a broad range of classification problems. The process includes a BASIC program that asks the user questions regarding the variables relevant to the problem and the outcomes possible in the problem. The program then must be given examples of the different outcomes and of the values of the associated variables. The program can handle any problem that has these characteristics: a set of variables relevant to the problem; different outcomes distinguished by a different pattern of values for the variables; and the pattern of values of the variables indicates which outcome would result.

A concrete example of this abstract definition is medical diagnosis. Here, the pattern (symptoms) tells the doctor

(continued)

ILLUSTRATED BY TOM CENTOLA

BOOK REVIEWS

which outcome (disease) is indicated. The pattern is represented by a set of variables: a 1 in a particular variable means the symptom that variable represents is present; a 0 stored means it is not. Another example is a fault-diagnosis problem to test Naylor's expert program. In this problem, the possible variables are the faults you might observe in a cassette recorder: no lights; tape won't move; unit won't record; intermittent sound; distorted sound; erratic speed; and hum. Depending on which subset of these seven variables is operative, you can determine which outcome (or fault) you should diagnose, such as the switch is off, the tape jammed, the tape was inserted wrongly, the head is dirty, or there's a problem with the amplifier. (An optional extension of this is incorporated in a listing.) Using the diagnosis as the input, the extension offers as output a suggested remedial action—clean the head, switch on the recorder, etc.—that is, it is a two-node (or two-stage) classification problem.

The second stage classifies the faults to produce remedial action. Readers can come up with their own examples of situations that fit this general classification-problem format. By finding a suitable problem that relates different subsets of a set of variables to different outcomes, the general program can be used for diagnosis.

In the course of developing this general program, Naylor introduces the theoretical concepts underlying the general classification problem, referred to in texts on statistical theory as multiple discriminant analysis (the problem of discriminating or distinguishing between different outcomes on the basis of information regarding the discriminating variables). By the time readers work through the explanations of each line of the program and what it does, they will have learned useful statistical theory related to a problem that holds their interest.

The author explains the fundamental basis of all diagnostic or classification-type expert systems. He illustrates how they are essentially a set of IF (set of symptoms) THEN (corresponding outcome or diagnosis) statements. These are usually referred to as "production rules." He discusses major successful expert systems, like MYCIN, for medical diagnosis; Prospector, for geological prospecting; and DENDRAL, for chemical analysis. The book is worth reading just for this lucid explanation of the basis of current systems and for the discussion of making a program so specific to a particular problem area that it cannot be easily adapted to a different problem area. In contrast, the programs Naylor teaches readers to build are of the learning type; that is, on the basis of examples of different types of problems, they can learn to diagnose problems in different areas. He points out that the disadvantage of this is that such a general program would not be as efficient as one built for a specific purpose.

SUMMARY

I highly recommend this book for several reasons. It provides a simple yet insightful discussion of extant successful

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expert systems. It teaches the basic principles of statistical theory, production rules, learning algorithms, and so forth in a practical way and provides a technical summary at the end of the book for reference. The book contains a program for an expert system that is based on an application of Bayes' theorem.

Running the program in chapter 7 helped immensely in following Naylor's explanations. Also, verifying that the sample program produced the results indicated by the author confirmed that I was on the right track. The programs are given in Apple II and Spectrum versions of BASIC. The reader with access to a different system (I had to modify the learning program for the IBM Personal Computer) becomes painfully aware of the difficulty of understanding the logic of another person's BASIC program when it is written in a version that uses only single-letter names for variables. Naylor mentions the unsuitability of BASIC for these types of programs; his choice was based on the fact that it is the language most commonly available for home computers. Now that microcomputer versions of a more suitable language, Prolog, are becoming available, I hope Naylor's next edition of the book will provide micro-PROLOG listings as well.

Ramachandran Bharath is a professor in the Department of Management, Marketing, and Data Processing at Northern Michigan University (Marquette, MI 49855).

ARTIFICIAL INTELLIGENCE IN BASIC
Reviewed by Norman J. Chaplin

The artificial intelligence (AI) invasion that was once predicted has now arrived. In fact, this intelligence has established itself in the areas of intelligent games, decision analysis, and expert systems, in addition to programs that correct spelling and grammar.

Mike James, the author of *Artificial Intelligence in BASIC*, believes the best way to comprehend the scope of AI is to gain experience in it. He recommends using BASIC, which is both widely understood and easily read.

To illustrate different techniques, James uses a few simple problems that are repeated in various branches of AI. He provides practical programs that can be entered without prohibitive effort from a keyboard. His BASIC dialect is a standard Microsoft version without special features; it can be adapted readily to most home computers.

James uses a heuristic attack on the familiar nine-square problem (arrange 8 numbered tiles in numerical order within a 3 by 3 array). He defines a heuristic rule as one that, when applied, tends to make the result move closer to the solution. With a heuristic, as opposed to an algorithm, there is no guarantee that a solution will be found. The path of the heuristic may be diverted into a closed loop of repeating positions. The program prints the board position to the screen every two to four moves and prints out the total number of moves taken to reach

a solution. Although many of my attempts ended in continual cycling through a particular sequence of moves, I generally solved the problem in twenty to sixty moves, and sometimes in as few as seven or eight.

MAN AND MACHINE

The opening chapter discusses "Your Computer's IQ," "Computer-Aided Intelligence," and "What Is Intelligence?" In the sections on pattern recognition and speech production and recognition, James admits that these subjects are too much for BASIC and are best handled with dedicated hardware. A discussion of grammar leads to an example of English generated by a computer. "Thinking, Reasoning, and Problem Solving" deals with mathematical theorem proving, cybernetics, and human associative memory.

Man teaches machine in chapters 4, 5, and 6. Man instructs the program Aardvark to recognize animals. To accomplish this, Aardvark asks a series of questions to build up its inventory of identifiable animals until it becomes an expert in animal identification. Aardvark is rudimentary, but with some expansion it could become a practical program, useful in fields such as mineral identification. I used it for bird identification.

"Structure of Memory" discusses the problem of memory-recall and explains computer solutions such as relational stores and conceptual databases. James fully illustrates the conceptual database problem with the Tom the Cat program, which solves the recall problem using a number of corresponding matrices. If you enter TOM IS A CAT: CAT HAS FUR: and then inquire, Does Tom have fur? the program answers YES. (Tom wouldn't run until I eliminated its bugs.)

LANGUAGE AND PHILOSOPHY

Another chapter deals with language: syntax, parsing, and semantics. Several pages cover Eliza, the psychotherapy program. There is also a listing and description of a BASIC program, Chat, that generates English sentences.

The last chapter is about philosophy. Can a computer program be intelligent? Or merely very clever? What about awareness? Should the Turing test be modified to measure artificial intelligence? The theme of this book could be summarized in James's words: "There is nothing very different about intelligent programs and they can be understood without any difficult theory." Neurophysiology shows us how small groups of neurons work, functions that we can duplicate electronically. Psychology, however, is so general that it can provide little practical guidance. James emphasizes that the third-generation software beginning to appear is characterized by the assumption that any misunderstandings are the program's fault, and the program will attempt to correct its mistake by learning the meaning of the new input from the user. This could be interpreted as intelligent behavior. I loaded a Commodore 64 with the Chat program, made a few changes, and found

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the answers from such a short program to be thought-provoking. The program generates ideas, which is a form of creativity. But is it creativity from the machine that arranges the word symbols, or from the man who interprets those symbols? Or both? Is this machine-aided creation? The sentences generated by Chat are enigmatic, but that could be changed by programming some restrictions on word association. The meaningless sentences would be reduced by this and further suppressed by a supervisory censor. We could even program it to learn from human prose. But would we then be restricting creativity?

If you are already competent in AI, *Artificial Intelligence in BASIC* is not for you unless you would like to instruct others. It could be a useful text for a short laboratory course in which the existing programs could be extended as exercises, or it could serve as a practical supplement to more theoretical material. It is superb as an introductory text for study at home. The programs are short enough that you could enter most in less than half an hour.

The knowledge attained from these short BASIC programs is readily transportable to other, more efficient languages, where it can become a tool for construction of large, more practical AI programs.

Norman J. Chaplin (3155 South Dr., Allentown, PA 18103) is a retired designer in VLSI now acting as a writer and consultant.

THE COGNITIVE COMPUTER
Reviewed by Darrow Kirkpatrick

Roger Schank, director of Yale University's Artificial Intelligence Project, has succeeded in writing a clear, exciting report on the nature of human intelligence and the implications of machine intelligence. Explaining his research, Schank tells us how much we must know about computers, what we can learn about intelligence from the development of understanding computers, and how intelligent computers will affect our world.

SETTING THE RECORD STRAIGHT

Schank risks distilling his 20 years of research into one nontechnical book about artificial intelligence. This is his attempt to set the record straight. Along the way we can learn a little about how computers work and a great deal about how human beings think, learn, and understand. Schank thinks learning about AI research is more important for an understanding of computers than learning to program in BASIC (or any of the other computer-literacy skills in vogue). AI research has the potential to transform our lives through the creation of new machines that can do things never done before.

COGNITIVE UNDERSTANDING

If we want to build understanding computers, first we must understand ourselves; we must be familiar with human

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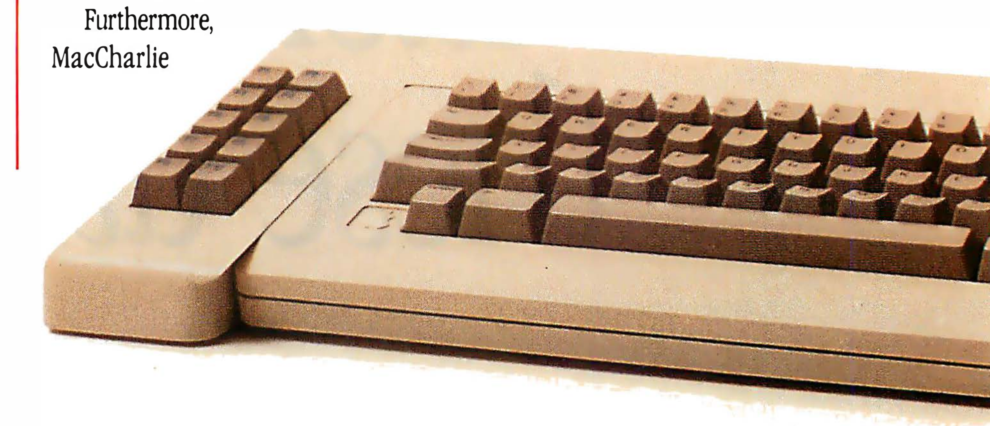
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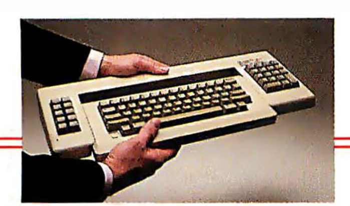
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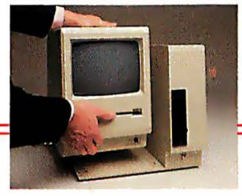
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thought processes before we can program an understanding computer. Schank defines three levels of understanding: making sense, cognitive understanding, and complete empathy. Current AI research is concerned mostly with cognitive understanding. Cognitive computers will be able to learn, relate the present to the past, formulate new information, and explain themselves.

People understand in terms of their own experiences. We can understand only if our memories are able to change to match a situation. In a sense, we are programmed by our experiences. But intelligent entities can, at best, "make sense" of experiences they haven't had. Computers will never understand us at the level of complete empathy because they are not like us.

Intelligence is the ability to react to something new in a nonprogrammed way. The fundamental difference between imitation and understanding in a system is self-knowledge. An intelligent system must be able to explain itself.

Because AI research is a new and different science, every major AI project is in some sense a failure at modeling human intelligence. Each success shows only what is missing. AI is a steady but plodding study of the impossible. As it asks questions about language, reading, and understanding, it can lead us to appreciate human qualities and abilities even more.

AI research has an uneasy relationship with computer science. Computer scientists are searching for ways to make computer hardware and software work more efficiently, but AI researchers are attempting to raise the level of understanding of computers. Ultimately, Schank feels, AI will be assimilated into other disciplines.

Schank defines product-directed AI as concerning the technology of getting computers to do intelligent things, and theory-directed AI as concerning the representation of knowledge, learning, and human thought processes. Expert systems are examples of product-directed AI.

Language and Knowledge Structures

Until recently, the representation of abstract ideas and concrete events has been possible only with natural languages. Computers also must be able to handle abstract concepts, but a system will not seem very intelligent without also having a clear grasp of the obvious. In a humorous progression of examples of conceptual errors in the development of an early AI program, Schank demonstrates just how obscure the obvious can be.

Our memories are tuned to ideas, not words. A major task in AI programs is making the computer forget the words and retain their meanings. An understanding system must rely on very basic conceptual representations of events. The Yale Artificial Intelligence Project utilizes only 11 primitive actions to represent real-world happenings.

An interesting thing about human knowledge is not how much we know, it's how effortlessly we recall what we know. One of the basic methods used to represent knowledge in AI programs is the "script." Scripts enable computers to deal with everyday, stereotypical situations by using a group of connected possibilities, or "slots," and rules for filling these slots.

But if computers are to understand more than stereotypical situations, they must have some knowledge of why and how people do what they do. Computers must have knowledge structures for goals and plans.

Early AI research concentrated on the outer form of language by building parsers to dissect language into its grammatical elements. Current research is occupied with understanding the *content* of communication. For Schank and others, language is a vehicle rather than an end; the aim is to write programs that concentrate on meaning rather than on grammatical structure.

In the early 1970s Schank and his students built software programs called the Inferencer and the Paraphraser. In order to process sentences and make conclusions, the Inferencer could parse, draw inferences, and generate natural language. The Paraphraser could understand a sentence well enough to restate it in different ways, from different perspectives. However, to understand large pieces of text, computers must draw inferences from many connected sentences.

A computer can use scripts to make up for the lack of logical connections between events, but researchers have to give the computer methods for dealing with the world when it does not have a script. More sophisticated AI programs use beliefs, inferences, plans, goals, scripts, and prior memories in order to understand. Researchers have seen the importance of a dynamic, flexible memory that changes every time it understands something.

In the long term, it is unrealistic for us to expect to build perfectly general knowledge structures into computers. Instead we must give them the ability to learn. This is the only way computers will be able to make connections across different fields of knowledge—thereby solving what Schank calls the "domain problem." Computers will have to know what they don't know as well as what they do know.

AI in Education

I suspect that first among Roger Schank's priorities is teaching. He has strong opinions about education. The issue is not how much we must learn *about* computers but what we can learn *from* them.

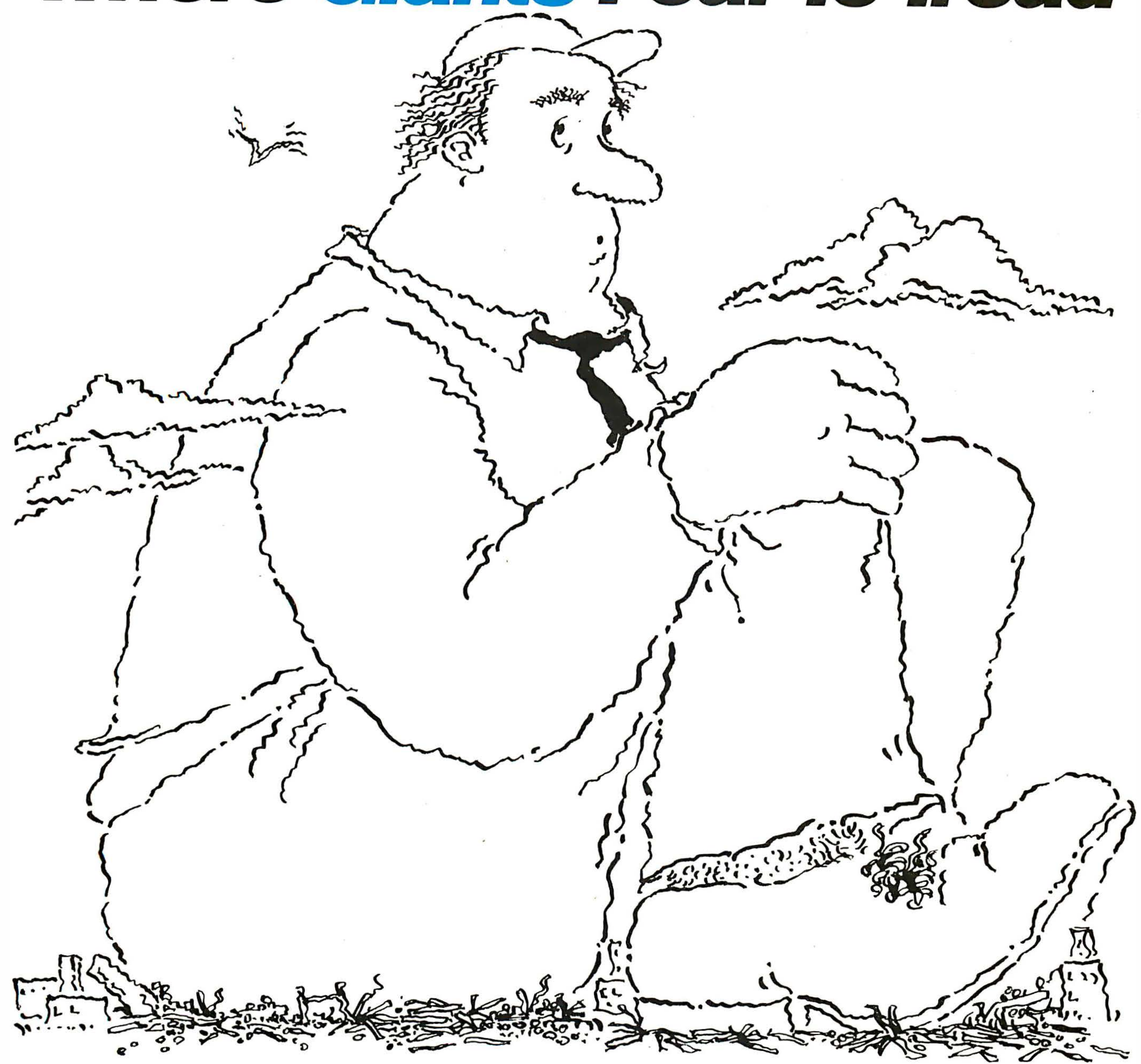
Schank thinks children should first learn to read and write. Public schools and teachers are not equipped to train children for programming careers. Schank concludes that children are better off with no programming skills rather than poorly taught computer skills.

Schank thinks that children must learn at an active, individualized pace. Children must actually learn, not just repeat, new principles. Experimentation with computers can provide this kind of learning.

For Schank, education is the most important and poten-

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CA3039H		1.25
CA3046N	14	.99
CA3059N	14	2.95
CA3060N	16	2.95
CA3065E	14	1.49
CA3080E	8	.99
CA3081N	16	1.15
CA3082N	16	1.15
CA3083N	16	1.15
CA3086N	14	.85
CA3089N	16	1.95
CA3096N	16	1.75
CA3130E	8	1.19
CA3140E	8	.85
CA3160H		1.79
CA3160E	8	1.49
CA3161E	16	1.79
CA3162E	16	6.95
CA3189E	16	2.79
CA3401N	14	.59

CD—CMOS

Part No.	Pins	Price
CD4001	14	.29
CD4002	14	.29
CD4006	14	.89
CD4007	14	.29
CD4008	16	.89
CD4009	16	.59
CD4010	16	.49
CD4011	14	.29
CD4012	14	.29
CD4013	14	.39
CD4014	16	.89
CD4015	16	.39
CD4016	14	.49
CD4017	16	.79
CD4018	16	.79
CD4019	16	.49
CD4020	16	.75
CD4021	16	.75
CD4022	16	.75
CD4023	14	.29
CD4024	14	.69
CD4025	14	.29
CD4026	16	1.59
CD4027	16	.45
CD4028	16	.69
CD4029	16	.79
CD4030	14	.39
CD4034	24	1.79
CD4035	16	.79
CD4040	16	.75

(More in Catalog)

Part No.	Pins	Price
CD4041	14	.69
CD4042	16	.69
CD4043	16	.79
CD4044	16	.79
CD4046	16	.89
CD4047	14	.89
CD4048	16	.59
CD4049	16	.39
CD4050	16	.39
CD4051	16	.79
CD4052	16	.89
CD4053	16	.79
CD4056	16	2.95
CD4059	24	3.95
CD4060	16	.89
CD4066	14	.45
CD4068	14	.39
CD4069	14	.35
CD4070	14	.29
CD4071	14	.29
CD4072	14	.29
CD4073	14	.29
CD4077	14	.35
CD4078	14	.49
CD4081	14	.29
CD4093	14	.49
CD4094	16	1.95
CD4098	16	1.95
CD4099	16	1.89

Part No.	Pins	Price
CD4503	16	.69
CD4506	16	1.29
CD4507	14	1.19
CD4508	24	1.95
CD4510	16	.85
CD4511	16	.85
CD4512	16	.85
CD4514	24	1.49
CD4515	24	1.49
CD4516	16	.89
CD4518	16	.89
CD4519	16	.59
CD4520	16	.89
CD4526	16	1.19
CD4528	16	1.19
CD4529	16	1.69
CD4531	16	.89
CD4538	16	1.49
CD4541	14	1.49
CD4543	16	1.19
CD4562	14	6.95
CD4566	16	2.95
CD4583	16	2.49
CD4584	14	.59
CD4723	16	1.19
CD4724	16	1.19
MC14410	16	8.95
MC14411	24	11.95
MC14412	16	7.95
MC14433	24	17.95
MC14572	16	1.19

74F00 NEW 74ALS00

Part No.	Pins	Function	Price
74F00	14	Quad 2-Input NAND Gate	.69
74F02	14	Quad 2-Input NOR Gate	.75
74F04	14	Hex Inverter	.89
74F08	14	Quad 2-Input AND Gate	.75
74F10	14	Triple 3-Input NAND Gate	.75
74F32	14	Quad 2-Input OR Gate	.79
74F74	14	Dual D Flip-Flop	.85
74F86	14	Quad Exclusive OR Gate	1.15
74F109	16	Dual JK Positive Edge Flip-Flop	.95
74F138	16	Expandable 3/8 Decoder	1.69
74F157	16	Quad 2-Input Multiplexer	1.69
74F158	16	Quad 2-Input Multiplexer (Inv.)	1.69
74F193	16	4-Bit Up/Down Binary Counter	5.29
74F240	20	Tri-State Octal Line Driver (Inverting)	3.75
74F244	20	Tri-State Octal Line Driver	3.49
74F257	16	Tri-State Quad 2-Input Multiplexer	1.79
74F373	20	Tri-State Octal Latch	4.89
74F374	20	Tri-State Octal D Flip-Flop	4.59

Part No.	Pins	Function	Price
74ALS00	14	Quad 2-Input NAND Gate	.59
74ALS02	14	Quad 2-Input NOR Gate	.59
74ALS04	14	Hex Inverter	.59
74ALS08	14	Quad 2-Input AND Gate	.59
74ALS10	14	Triple 3-Input NAND Gate	.59
74ALS30	14	8-Input NAND Gate	.59
74ALS32	14	Quad 2-Input OR Gate	.65
74ALS74	14	Dual D Flip-Flop	.79
74ALS109	16	Dual JK Pos. Edge Flip-Flop	.79
74ALS138	16	Expandable 3/8 Decoder	1.25
74ALS240	20	Tri-State Octal Line Driver (Inverting)	2.25
74ALS244	20	Tri-State Octal Line Driver	2.25
74ALS245	20	Octal Bus Transceiver (Non-Inv.)	2.59
74ALS373	20	Tri-State Octal Latch	2.59
74ALS374	20	Tri-State Octal D Flip-Flop	2.59

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MICROPROCESSOR CHIPS

Part No.	Pins	Function	Price
D765AC	40	Floppy Disk Controller	16.95 ~~19.95~~
D3242	28	Addr. Multiplexer & Refresh Counter	7.95
TMS5501	40	Synchronous Data Interface (SIRC)	14.95
Z80, Z80A, Z80B, Z8000 SERIES			
Z80	40	CPU (MK3880N)(780C)2.5MHz	2.75 ~~2.95~~
Z80-CTC	28	Counter Timer Circuit	3.49
Z80-DART	40	Dual Asynchronous Rec./Trans.	8.95
Z80-DMA	40	Direct Memory Access Circuit	12.49
Z80-PIO	40	Parallel I/O Interface Controller	2.95 ~~3.49~~
Z80-SIO/0	40	Serial I/O (TxCB and RxCB Bonded)	11.49
Z80-SIO/1	40	Serial I/O (Lacks DTRB)	11.49
Z80-SIO/2	40	Serial I/O (Lacks SYNCB)	11.49
Z80-SIO/9	40	Serial I/O	11.49
Z80A	40	CPU (MK3880N-4)(780C-1)4MHz	2.95 ~~3.49~~
Z80A-CTC	28	Counter Timer Circuit	3.95 ~~4.49~~
Z80A-DART	40	Dual Asynchronous Rec./Trans.	9.95
Z80A-DMA	40	Direct Memory Access Circuit	12.95
Z80A-PIO	40	Parallel I/O Interface Controller	3.95
Z80A-SIO/0	40	Serial I/O (TxCB and RxCB Bonded)	11.95
Z80A-SIO/1	40	Serial I/O (Lacks DTRB)	11.95
Z80A-SIO/2	40	Serial I/O (Lacks SYNCB)	11.95
Z80A-SIO/9	40	Serial I/O	11.95
Z80B	40	CPU (MK3880N-6) 6MHz	8.95
Z80B-CTC	28	Counter Timer Circuit	11.95
Z80B-DART	40	Dual Asynchronous Rec./Trans.	19.95
Z80B-PIO	40	Parallel I/O Interface Controller	10.95
Z6001 3	48	CPU Segmented (10MHz)	79.95
Z8002B	40	CPU Non-Segmented (10MHz)	59.95
6500/6800/68000 SERIES			
6502	40	MPU with Clock (1MHz)	4.95
6502A	40	MPU with Clock (2MHz)	6.49
6502B	40	MPU with Clock (3MHz)	8.95
6520	40	Peripheral Inter. Adapter	3.95
6522	40	Versatile Inter. Adapter	5.49
6551	28	Async Comm. Interface Adapt.	6.95 ~~10.95~~
6800	40	MPU	2.95
6802CP	40	MPU with Clock and RAM	5.95 ~~7.95~~
6809	40	CPU — 8-Bit (On-Chip Oscillator)	8.95
6809E	40	CPU — 8-Bit (External Clocking)	9.95
68B09E	40	CPU — 8-Bit (Ext. Clocking) 2MHz	14.95
68B10	24	128x8 Static RAM (2MHz)	5.95
6821	40	Peripheral Inter Adapt. (MC6820)	2.75 ~~2.95~~
68B21	40	Peripheral Interface Adapter (2MHz)	5.95
6845	40	CRT Controller (CRTC)	9.95 ~~14.95~~
68B45	40	CRT Controller (CRTC) 2MHz	14.95 ~~15.95~~
6850	24	Asynchronous Comm. Adapter	3.95
6860	24	0-600bps Digital MODEM	7.95
68000L8	64	MPU 16-Bit (8MHz)	39.95
68488P	40	General Purpose Inl. Adapter	9.95
8000/80000 SERIES			
8031	40	Control Oriented CPU w/RAM & I/O	12.95 ~~14.95~~
8035	40	MPU — 8-Bit	4.95 ~~6.95~~
8039	40	CPU — Sgl. Chip 8-Bit (128 bits RAM)	4.95 ~~5.95~~
8040N-6	40	CPU (256 bytes RAM)	9.95
8060	40	CPU — 8-Bit NMOS	12.95 ~~14.95~~
8073N	40	CPU w/Basic Micro Interpreter	29.95
8080A	40	CPU	3.95
8085A	40	CPU	4.95
8085A-2	40	CPU-8-Bit N-Channel (5MHz)	10.95 ~~11.95~~
8086-2	40	CPU 16-bit 8MHz	19.95 ~~24.95~~
8087	40	Arithmetic Processor	169.95 ~~189.95~~
8088	40	CPU 8/16-Bit	14.95 ~~19.95~~
8155	40	HMOS RAM I/O Port-Timer	4.95 ~~5.95~~
8156	40	RAM with I/O Port and Timer	6.95 ~~8.95~~
8205	16	Hi Speed 1 out of 8 Binary Decoder	3.95
8212	24	8-Bit Input/Output (74S412)	2.95
8224	16	Clock Generator/Driver	2.95
8228	28	Sys. Cont./Bus Driver (74S428)	3.95 ~~4.95~~
8237-5	40	High Perf. Prog. DMA Cont. (5MHz)	14.95 ~~19.95~~
8238	28	System Controller (74S438)	4.95
8243	24	I/O Expander for 48 Series	3.95 ~~4.95~~
8250N	40	Async. Comm. Element	10.95
8251	28	Prog. Comm. I/O (USART)	4.49 ~~4.95~~
8251A	28	Prog. Comm. Interface (USART)	4.95 ~~7.95~~
8253	24	Prog. Interval Timer	5.95 ~~6.95~~
8255	40	Prog. Peripheral I/O (PPI)	4.49 ~~4.95~~
8255A-5	40	Prog. Peripheral I/O (PPI) 5MHz	4.95 ~~7.95~~
8259	28	Prog. Interrupt Control	5.95
8272	40	Sgle/Dble Density Floppy Disk Cont.	16.95 ~~19.95~~
8274	40	Multi-Protocol Serial Cont. (7201)	14.95 ~~29.95~~
8279	40	Prog. Keyboard/Display Interface	6.95
8282	20	Octal Latch	6.49 ~~8.95~~
8284	18	Clock Generator/Driver	5.49 ~~5.95~~
8286	20	Octal Bus Transceiver	6.49 ~~7.95~~
8287	20	Octal Bus Transceiver (Inverted)	6.49 ~~7.95~~
8288	20	Bus Controller	14.95 ~~19.95~~
8303	20	8-Bit Tri-State Bi-Directional Trans.	3.49
8304	20	8-Bit Bi-Directional Receiver	3.49
8310	20	Octal Latched Peripheral Driver	3.95
8741	40	8-Bit Univ. Peripheral Interface	19.95 ~~29.95~~
8748	40	HMOS EPROM MPU	19.95 ~~39.95~~
8749	40	MPU 8-Bit EPROM Version of 8049	24.95 ~~39.95~~
8755	40	16K EPROM with I/O	39.95
80186-6	68	High Integration 16-Bit MPU	99.95
80188	68	High Integra. 16-Bit MPU (8-Bit Data Bus)	89.95
SPECIAL FUNCTION			
DS0026CN	8	Dual MOS Clock Driver (5MHz)	1.95
INS2651	28	Communication Chip	7.95
MC3470P	18	Floppy Disk Read Amp System	4.95
MM5321N	16	TV Camera Sync. Generator	9.95
MM54240N	24	Asynchronous Transmitter/Receiver	5.95
MM58167AN	24	Microprocessor Real Time Clock	8.95
MM58174AN	16	Micro Compatible Time Clock	8.95
*MM5369AA/N	8	Prog. Oscillator/Divider (60Hz)	1.79
MM5369EST	8	Prog. Oscillator/Divider (100Hz)	1.95

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DYNAMIC RAMS

Part No.	Pins	Function	Price
1103	18	1024x1 (300ns)	.99
4027	16	4096x1 (250ns)	1.49
4116N-15	16	16,384x1 (150ns)	1.39 — 8/10.95
4116N-20	16	16,384x1 (200ns)	.79-8/6.29 ~~1.15-8/8.95~~
4116N-25	16	16,384x1 (250ns)	.69-8/5.49 ~~[illegible]~~
4164N-150	16	65,536x1 (150ns)	3.95-8/31.49 ~~5.19-8/40.95~~
4164N-200	16	65,536x1 (200ns)	3.75-8/29.95 ~~4.95-8/38.95~~
MM5261	18	1024x1 (300ns)	.35 — 8/1.95
MM5262	22	2048x1 (365ns)	.35 — 8/1.95
MM5270	18	4096x1 (250ns) MK4096	4.95
MM5280	22	4096x1 (200ns) 2107	3.95
MM5298-3	16	8192x1 (200ns)	.59
41256-150	16	262,144x1 (150ns)	15.95 ~~24.95~~
41256-200	16	262,144x1 (200ns)	13.95 ~~31.95~~
48128	16	131,072x1 (250ns)	24.95
STATIC RAMS			
2101	22	256x4 (450ns) 8101	1.95
2102	16	1024x1 (350ns)	.89
2102-2L	16	1024x1 (250ns) L.P. (91L02)	1.49
2111	18	256x4 (450ns) 8111	2.49
2112	16	256x4 (450ns) MOS	2.49
2114N	18	1024x4 (450ns)	1.29 — 8/9.95
2114N-L	18	1024x4 (450ns) L.P.	1.65 — 8/12.95
2114N-2	18	1024x4 (200ns)	1.39 — 8/10.95
2114N-2L	18	1024x4 (200ns) L.P.	1.69 — 8/13.49
2147HN	18	4096x1 (70ns)	4.49
2148HN	18	1024x4 (70ns)	4.95
TMS4045	18	1024x4 (450ns)	3.95
TMS40L47-45	20	1024x4 (450ns)	1.95
5101	22	256x4 (450ns) CMOS	3.95
MM5257	18	4096x1 (450ns) 4044	4.95
HM6116P-2	24	2048x8 (120ns) CMOS	7.95
HM6116LP-2	24	2048x8 (120ns) L.P. CMOS	8.95
HM6116P-3	24	2048x8 (150ns) CMOS	3.95 ~~4.95~~
HM6116LP-3	24	2048x8 (150ns) L.P. CMOS	4.95 ~~5.49~~
HM6116P-4	24	2048x8 (200ns) CMOS	3.75 ~~4.75~~
HM6116LP-4	24	2048x8 (200ns) L.P. CMOS	4.75 ~~5.49~~
HM6264P-12	28	8192x8 (120ns) CMOS	19.95 ~~37.95~~
HM6264LP-12	28	8192x8 (120ns) L.P. CMOS	21.95 ~~39.95~~
HM6264P-15	28	8192x8 (150ns) CMOS	16.95 ~~34.55~~
HM6264LP-15	28	8192x8 (150ns) L.P. CMOS	17.95 ~~37.95~~
27LS00	16	256x1 (80ns) L.P.	3.95
7489	16	16x4 (50ns) 3101	2.25
74C921	18	256x4 (250ns) CMOS	5.95
74C930	18	1024x1 (250ns) CMOS (6518)	5.95
74S189	16	16x4 (35ns) 93405	2.95
74S289	16	16x4 (35ns) 3101	2.95
82S10	16	1024x1 (50ns) O.C. (93415)	3.95
82S25	16	16x4 (50ns) O.C. (74S289)	2.25
PROMS/EPROMS			
1702A	24	256x8 (1µs)	3.95
2708	24	1024x8 (450ns)	3.95
TMS2516	24	2048x8 (450ns) 2716	4.95
TMS2532	24	4096x8 (450ns) NMC2532	5.49
TMS2564	28	8192x8 (450ns)	10.95
TMS2716	24	2048x8 (450ns) 3 voltage	7.95
2716	24	2048x8 (450ns)	3.95
27C16	24	2048x8 CMOS	12.95 ~~14.95~~
2716-1	24	2048x8 (350ns)	5.49
27160-5	24	2048x8 (550ns)	3.75
2732	24	4096x8 (450ns)	4.95
2732A-20	24	4096x8 (200ns) 21V	11.49
2732A-25	24	4096x8 (250ns) 21V	7.19
2732A-45	24	4096x8 (450ns) 21V	4.95 ~~6.49~~
27C32	24	4096x8 CMOS	14.95 ~~19.95~~
27C32A-30	24	4096x8 (300ns) 21V (CMOS)	22.95
2764-20	28	8192x8 (200ns) 21V	9.95 ~~14.95~~
2764-25	28	8192x8 (250ns) 21V	7.19
2764-45	28	8192x8 (450ns) 21V	6.49
27C64	28	8192x8 CMOS 21V	14.95 ~~22.95~~
MCM68764	24	8192x8 (450ns) 21V	14.95 ~~24.95~~
27128-25	28	16,384x8 (250ns) 128K 21V	12.95 ~~21.95~~
27256-25	28	32768x8 (250ns) 256K (14V)	49.95 ~~99.95~~
74S188	16	32x8 PROM O.C. (6330-1)	1.75
74S287	16	256x4 PROM T.S. (6301-1)	1.79
74S288	16	32x8 PROM T.S. (6331-1)	1.79
74S387	16	256x4 PROM O.C. (6300-1)	1.95
74S471	20	256x8 PROM T.S. (6309-1)	4.95
74S472	20	512x8 PROM T.S. (6349-1)	4.95
74S473	20	512x8 PROM O.C. (6348)	4.95
74S474	24	512x8 PROM T.S. (DM87S296N)	4.95
74S475	24	512x8 PROM O.C. (6340)	4.95
74S476	18	1024x4 PROM T.S.	6.95
74S478	24	1024x8 PROM T.S.	9.95
74S570	16	512x4 PROM O.C. (6305)	2.95
74S571	16	512x4 PROM T.S. (6306)	2.95
74S572	18	1024x4 PROM O.C. (6352)	4.95
74S573	18	1024x4 PROM T.S. (82S137)	4.95
82S23	16	32x8 PROM O.C. (27S18)	2.95
82S115	24	512x8 PROM T.S. (27S15)	9.95
82S123	16	32x8 PROM T.S. (27S19)	2.95
82S126	16	256x4 PROM O.C. (27S20)	2.95
82S129	16	256x4 PROM T.S. (27S21)	2.95
82S130	16	512x4 PROM O.C. (27S12)	3.95
82S185	18	2048x4 PROM T.S. (TBP24S81)	9.95
82S191	24	2048x8 (80ns)	14.95
DM87S181N	24	1024x8 PROM T.S. (82S181)	9.95
DM87S184N	18	2048x4 PROM O.C. (82S184)	9.95
DM87S185N	18	2048x4 PROM T.S. (82S185)	9.95
DM87S191N	24	2048x8 PROM T.S. (82S191)	14.95
DATA ACQUISITION			
DC10		Mostek DC/DC Converter +5V to −9V	2.95
ADC0801	20	8-Bit A/D Converter (1/4LSB)	14.95
ADC0803	20	8-Bit A/D Converter (±1/2LSB)	4.95
ADC0804	20	8-Bit A/D Converter (1LSB)	3.49
ADC0808	28	8-Bit A/D Conv. w/8-Channel Analog	9.95
ADC0809	28	8-Bit A/D Converter (8-Ch. Multi.)	4.49
ADC0816	40	8-Bit A/D Conv. w/16-Channel Analog	14.95
ADC0817	40	8-Bit A/D Converter (16-Ch. Multi.)	9.49
DAC0806	16	8-Bit D/A Converter (0.78% Lin.)	1.95
DAC0807	16	8-Bit D/A Converter (MC1408-7)	1.49
DAC0808	16	8-Bit D/A Converter (MC1408-8)	2.25
DAC0830	20	8-Bit Up D/A Conv. (.05% Lin)	5.95
DAC0831	20	8-Bit Up D/A Conv. (.10% Lin)	4.49
DAC1000	24	10-Bit D/A Conv. Micro. Comp. (0.05%)	7.95
DAC1008	20	10-Bit D/A Conv. Micro. Comp. (0.20%)	6.95
DAC1020	16	10-Bit D/A Conv. (0.05% Lin.)	7.95
DAC1022	16	10-Bit D/A Conv. (0.20% Lin.)	5.95
DAC1222	18	12-Bit D/A Conv. (0.20% Lin.)	6.95
DAC1230	20	12-Bit Up D/A Conv. (.05% Lin.)	19.95
DAC1231	20	12-Bit Up D/A Conv. (.10% Lin.)	13.95
AY-5-1013A	40	30K Baud UART (TR1602)	3.95

Low Profile (Tin) Sockets

Part No.	1-9	10-99	100-up
8 pin LP	.16	.14	.13
14 pin LP	.17	.15	.11
16 pin LP	.19	.17	.16
18 pin LP	.26	.24	.23
20 pin LP	.30	.27	.25
22 pin LP	.31	.28	.26
24 pin LP	.33	.30	.28
28 pin LP	.40	.37	.35
40 pin LP	.49	.46	.43

Soldertail (Gold) Standard

Part No.	1-9	10-99	100-up
8 pin SG	.39	.35	.29
14 pin SG	.49	.45	.39
16 pin SG	.55	.49	.45
18 pin SG	.65	.59	.51
20 pin SG	.75	.65	.59
22 pin SG	.79	.69	.65
24 pin SG	.79	.69	.65
28 pin SG	.95	.85	.75
36 pin SG	1.25	1.15	.99
40 pin SG	1.39	1.25	1.15

Wire Wrap Sockets (Gold) Level #3

Part No.	1-9	10-99	100-up
8 pin WW	.55	.49	.45
10 pin WW	.69	.65	.59
14 pin WW	.75	.69	.65
16 pin WW	.79	.72	.65
18 pin WW	.95	.85	.75
20 pin WW	1.19	1.09	.95
22 pin WW	1.29	1.19	1.05
24 pin WW	1.35	1.19	1.09
28 pin WW	1.69	1.55	1.39
36 pin WW	1.89	1.79	1.69
40 pin WW	2.29	1.95	1.79

Header Plugs (Gold)

Part No.	1-9	10-99	100-up
14 pin HP	.65	.59	.55
16 pin HP	.69	.65	.59
24 pin HP	1.15	.99	.89

Header Covers

Part No.	1-9	10-99	100-up
14 pin HC	.15	.13	.12
16 pin HC	.19	.17	.15
24 pin HC	.29	.25	.22

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1355 SHOREWAY ROAD, BELMONT, CA 94002
4/85 ***PHONE ORDERS WELCOME — (415) 592-8097 — Telex: 176043***

DISK CONTROLLERS

Part No.	Pins	Function	Price
INS1771-1	40	Single Density	16.95
FD1791	40	Single/Dual Density (Inv.)	24.95
FD1793	40	Single/Double Density (True)	25.95
FD1795	40	Dual Density/Side Select (Inv.)	26.95
FD1797	40	Dual Density/Side Select (True)	29.95
WD2791	40	Single/Double Density (Inv.)	39.95
WD2793	40	Single/Double Density (True)	39.95
WD2797	40	Dual Density/Side Select (True)	39.95

Digitalker™

DT1050 — Applications: Teaching aids, appliances, clocks, automotive, telecommunications, language translations, etc. The DT1050 is a standard DIGITALKER kit encoded with 137 separate and useful words, 2 tones, and 5 different silence durations. The words and tones have been assigned discrete addresses, making it possible to output single words or words concatenated into phrases or even sentences. The "voice" output of the DT1050 is a highly intelligible male voice. The DT1050 consists of a Speech Processor Chip, MM54104 (40-pin) and two (2) Speech ROMs MM52164SSR1 and MM52164SSR2 (24-pin) along with a Master Word list and a recommended schematic diagram on the application sheet.

DT1050 Digitalker™ . . . . $34.95 ea.
MM54104 Processor Chip. . . . . $14.95 ea.

DT1057 — Expands the DT1050 vocabulary from 137 to over 260 words. Incl. 2 ROMs and specs.
Part No. DT1057. . . . . $24.95 ea.

INTERSIL

Part No.	Pins	Function	Price
7045IPI	28	CMOS Precision Timer	14.95
7045EV/Kit	28	Stopwatch Chip, XTL (Evaluation Kit)	19.95
7106CPL	40	3½ Digit A/D LCD Driver	10.49
FE0202D	40	4 Digit LCD Display for 7211IPL & 7211MIPL	14.95
FE0203D	40	3½ Digit LCD Display for 7106 & 7116	14.95
7106EV/Kit	40	IC, Circuit Board, Display (Evaluation Kit)	46.95
7107CPL	40	3½ Digit A/D LED Driver	10.95
7107EV/Kit	40	IC, Circuit Board, Display (Evaluation Kit)	46.95
7116CPL	40	3½ Digit A/D LCD Drs. HLD	10.95
7201IUS		Low Battery Volt. Indicator	2.25
7205IPG	24	CMOS LED Stopwatch/Timer	14.95
7205EV/Kit	24	Stopwatch Chip, XTL (Evaluation Kit)	16.95
7206CJPE	16	Tone Generator	4.95
7206CEV/Kit	16	Tone Generator Chip, XTL (Evaluation Kit)	7.95
7207AIPD	14	Oscillator Controller	5.95
7207AEV/Kit	14	Freq. Counter Chip, XTL (Evaluation Kit)	8.49
7211IPL	40	4 Digit LCD Display Decoder/Driver (TTL compatible)	7.95
7211MIPL	40	4 Digit LCD Display Decoder/Driver (Microproc. compat.)	8.95
7215IPG	24	4 Func. CMOS Stopwatch CKT	16.95
7215EV/Kit	24	4 Func. Stopwatch Chip, XTL (Evaluation Kit)	19.49
7216AIJI	28	8 Digit Univ. Counter C.A.	31.49
7216DIPI	28	8 Digit Freq. Counter C.C.	21.49
7217IJI	28	4 Digit LED Up/Down Counter C.A.	10.95
7217AIPI	28	4 Digit LED Up/Down Counter C.C.	9.95
7224IPL	40	LCD 4½ Digit Up Counter DRI.	10.95
7226AEV/Kit	40	5 Function Counter Chip, XTL (Evaluation Kit)	99.95

30009 1983 INTERSIL Data Book (1356p.) $9.95

74HC High Speed CMOS

Part No.	Pins	Price
74HC00	14	.59
74HC02	14	.59
74HC03	14	.89
74HC04	14	.59
74HCU04	14	.69
74HC08	14	.59
74HC10	14	.59
74HC11	14	.69
74HC14	14	.89
74HC20	14	.59
74HC27	14	.59
74HC30	14	.69
74HC32	14	.79
74HC42	16	1.09
74HC51	14	.89
74HC58	14	.89
74HC73	14	.79
74HC74	14	.79
74HC75	16	.99
74HC76	16	.79
74HC85	16	1.69
74HC86	14	.75
74HC107	14	.79
74HC109	16	.79
74HC112	16	.79
74HC123	16	2.29
74HC125	14	1.75
74HC132	14	1.29
74HC137	16	1.59
74HC138	16	1.19

Part No.	Pins	Price
74HC139	16	1.05
74HC147	16	1.29
74HC151	16	.99
74HC153	16	1.09
74HC154	24	2.65
74HC157	16	.99
74HC158	16	.99
74HC160	16	1.39
74HC161	16	1.39
74HC162	16	1.39
74HC163	16	1.39
74HC164	14	1.35
74HC165	16	2.15
74HC166	16	2.49
74HC173	16	1.29
74HC174	16	1.09
74HC175	16	1.09
74HC190	16	1.59
74HC191	16	1.59
74HC192	16	1.49
74HC193	16	1.49
74HC194	16	1.19
74HC195	16	1.19
74HC221	16	2.95
74HC237	16	1.49
74HC240	20	2.29
74HC241	20	2.29
74HC242	14	2.15
74HC243	14	2.15
74HC244	20	2.29

Part No.	Pins	Price
74HC245	20	2.59
74HC251	16	.99
74HC253	16	1.09
74HC257	16	.99
74HC259	16	1.69
74HC266	14	.89
74HC273	20	2.79
74HC280	14	4.59
74HC299	20	5.59
74HC366	16	2.59
74HC367	16	2.59
74HC373	20	2.69
74HC374	20	2.69
74HC390	16	1.59
74HC393	14	1.59
74HC533	20	2.69
74HC534	20	2.69
74HC595	16	3.19
74HC688	20	3.59
74HC4024	14	1.75
74HC4040	16	1.49
74HC4060	16	1.49
74HC4075	14	.59
74HC4078	14	.59
74HC4511	16	1.95
74HC4514	24	4.19
74HC4538	16	2.59
74HC4543	16	3.75

74HCU04 is unbuffered. All others are buffered.

74C—C/MOS

Part No.	Pins	Price
74C00	14	.29
74C02	14	.35
74C04	14	.35
74C08	14	.35
74C10	14	.35
74C14	14	.59
74C20	14	.35
74C30	14	.35
74C32	14	.39
74C42	16	1.19
74C48	16	1.79
74C73	14	.69
74C74	14	.59
74C85	16	1.39
74C86	14	.29
74C89	16	5.95
74C90	14	1.09
74C93	14	1.09
74C95	14	1.19

Part No.	Pins	Price
74C107	14	.79
74C151	16	2.19
74C154	24	3.25
74C157	16	1.75
74C160	16	1.19
74C161	16	1.19
74C162	16	1.19
74C163	16	1.19
74C164	14	1.29
74C165	16	1.29
74C173	16	.89
74C174	16	1.19
74C175	16	1.19
74C192	16	1.39
74C193	16	1.39
74C195	16	1.29
74C221	16	1.75

Part No.	Pins	Price
74C240	20	1.95
74C244	20	1.95
74C373	20	2.29
74C374	20	2.29
74C901	14	.59
74C902	14	.79
74C903	14	.59
74C906	14	.59
74C907	14	.69
74C911	28	8.95
74C912	28	8.95
74C915	18	1.19
74C917	28	8.95
74C922	18	4.49
74C923	20	4.95
74C925	15	5.95
74C926	18	5.95
80C95	16	.69
80C97	16	.69

LINEAR

Part No.	Pins	Price
TL071CP	8	.79
TL072CP	8	1.09
TL074CN	14	1.95
TL081CP	8	.59
TL082CP	8	1.19
TL084CN	14	1.95
LM109K		5.95
LM301CN	8	.39
LM302H		2.49
LM304H		1.95
LM305H		.99
LM307CN	8	.49
LM308CN	8	.69
LM309K		1.25
LM310CN	8	1.95
LM311CN	8	.59
LM312H		2.79
LM317T		1.19
LM317K		3.49
LM318CN	8	1.59
LM319N	14	1.49
LM320K-5		1.35
LM320K-12		1.35
LM320K-15		1.35
LM320K-24		1.35
LM320T-5		.85
LM320T-12		.85
LM320T-15		.85
LM320T-24		.85
LM322N	14	1.49
LM323K		4.95
LM324N	14	.59
LM329DZ		.65
LM331N	8	3.95
LM334Z		1.19
LM335Z		1.29
LM336Z		1.09
LM337MP		1.15
LM337T		1.89
LM338K		6.95
LM339N	14	.69
LM340K-5		1.35
LM340K-12		1.35
LM340K-15		1.35
LM340K-24		1.35
LM340T-5		.75
LM340T-12		.75
LM340T-15		.75
LM340T-24		.75
LF347N	14	1.49
LM348N	14	.89
LM350K		4.79
LF351N	8	.59
LF353N	8	.89

Part No.	Pins	Price
LF355N	8	1.09
LF356N	8	1.09
LM358N	8	.59
LM359N	14	1.79
LM370N	14	4.95
LM373N	14	4.95
LM377N	14	1.95
LM380CN	8	1.09
LM380N	14	.89
LM381N	14	1.79
LM382N	14	1.49
LM384N	14	1.95
LM386N-3	8	.89
LM387N	8	1.39
LM389N	18	1.19
LM391N-80	16	1.19
LM392N	8	.59
LM393N	8	.45
LF398N	8	3.95
LM399H		5.95
LF412CN	8	1.95
TL494CN	16	2.79
TL496CP	8	1.59
NE531V	8	1.79
NE544N	14	1.95
NE550A	14	1.95
NE555V	8	.35
XR-L555	8	.69
LM556N	14	.79
NE558N	16	1.59
NE564N	16	1.95
LM565N	14	.99
LM566CN	8	1.49
LM567V	8	.99
NE570N	16	2.95
NE571N	16	2.49
NE592N	14	1.19
LM703CN	8	1.49
LM710N	14	.69
LM711N	14	.79
LM723N	14	.49
LM733N	14	.89
LM739N	14	1.95
LM741CN	8	.39

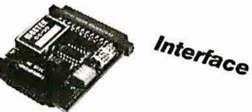
Part No.	Pins	Price
LM747N	14	.69
LM748N	8	.59
UA760HC		9.95
LM1456V	8	1.95
LM1458CN	8	.59
LM1488N	14	.69
LM1489N	14	.69
LM1496N	14	.99
LM1605CK		9.95
LM1800N	16	2.49
LM1871N	18	2.95
LM1872N	18	3.25
LM1877N-9	14	2.95
LM1889N	16	1.95
LM1896N	14	1.59
LM2002T		1.95
ULN2003A	16	1.49
XR2206	16	3.95
XR2207	14	2.49
XR2208	16	1.79
XR2211	14	2.95
LM2877P		1.95
LM2878P		2.95
LM2901N	14	.79
LM2902N	14	.89
LM2907N	14	2.49
LM2917N	8	1.95
LM3900N	14	.59
LM3905CN	8	1.19
LM3909N	8	.89
LM3914N	18	2.39
LM3915N	18	2.39
LM3916N	18	2.39
RC4136N	14	1.25
RC4151NB	8	1.95
RC4195TK		5.95
LM4250CN	8	1.49
LM4500A	16	2.95
NE5532	8	1.69
NE5534	8	1.39
79M05AH		1.29
ICL8038	14	3.95
LM13080N	8	1.19
LM13800N	16	1.19
76477	28	3.95

MORE AVAILABLE

30003 1982 Nat. Linear Data Book (1952pgs.) . $11.95

Commodore® Accessories

RS232 ADAPTER FOR VIC-20 AND COMMODORE 64

The JE232CM allows connection of standard serial RS232 printers, modems, etc. to your VIC-20 and C-64. A 4-pole switch allows the inversion of the 4 control lines. Complete installation and operation instructions included.

• Plugs into User Port • Provides Standard RS232 signal levels • Uses 6 signals (Transmit, Receive, Clear to Send, Request to Send, Data Terminal Ready, Data Set Ready).

JE232CM $39.95

VOICE SYNTHESIZER FOR APPLE AND COMMODORE



• Over 250 word vocabulary-affixes allow the formation of more than 500 words • Built-in amplifier, speaker, volume control, and audio jack • Recreates a clear, natural male voice • Plug-in user ready with documentation and sample software • Case size: 7¼"L x 3¼"W x 1-3/8"H

APPLICATIONS: • Security Warning • Telecommunication • Teaching • Handicap Aid • Instrumentation • Games

Part No.	Description	Price
JE520CM	For Commodore 64 & VIC-20	$114.95
JE520AP	For Apple II, II+, and //e	$149.95

Computer Memory Expansion Kits

All Major Manufacturers- Not Micron

IBM PC, PC XT and Compatibles

Most of the popular Memory Boards (e.g. Quadram™ Expansion Boards) allow you to add an additional 64K, 128K, 192K or 256K. The IBM64K Kit will populate these boards in 64K byte increments. The Kit is simple to install—just insert the 9 - 64K RAM chips in the provided sockets and set the 2 groups of switches. Complete conversion documentation included.

IBM64K (Nine 200ns 64K RAMs). $33.49

IBM PC AT

Each kit comes complete with nine 128K dynamic RAMs and documentation for conversion.

IBM128K (Nine 250ns 128K RAMs). $199.95

APPLE //e

Extended 80-Column/64K RAM Card. Expands memory by 64K to give 128K when used with programs like VisiCalc™. Fully assembled and tested.

JE864. . . . . $99.95

TRS-80 MODEL I, III

Each Kit comes complete with eight MM5290 (UPD416/4116) 16K Dynamic RAMs and documentation for conversion. Model 1: 16K equipped with Expansion Interface can be expanded to 48K with 2 Kits. Model III: Can be expanded from 16K to 48K using 2 Kits. Each Kit will expand computer by 16K increments.

TRS-16K3 200ns (Model III). $6.29
TRS-16K4 250ns (Model 1). $5.49

TRS-80 MODEL IV & 4P

Easy to install Kit comes complete with 8 ea. 4164N-20 (200ns) 64K Dynamic RAMs and conversion documentation. Converts TRS-80 Model IV computers from 16K to 64K. Also expands Model 4P from 64K to 128K.

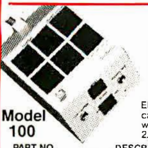
TRS-64K-2. . . . . $29.95
(Converts the Model IV from 16K to 64K or will expand the Model 4P from 64K to 128K)

TRS-64K2PAL (Model IV only). $49.95
(8 - 4164's with PAL Chip to expand from 64K to 128K)

TRS-80 COLOR AND COLOR II

Easy to install Kit comes complete with 8 each 4164N-20 (200ns) 64K Dynamic RAMs and documentation for conversion. Converts TRS-80 Color Computers with D, E, ET, F and NC circuit boards to 32K. Also converts TRS-80 Color Computer II to 64K. Flex DOS or OS-9 required to utilize full 64K RAM on all computers.

TRS-64K-2. . . . . $29.95



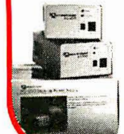
PTI INDUSTRIES

PROTECT YOURSELF...

DATASHIELD® Surge Protector

Eliminates voltage spikes and EMI-RFI noise before it can damage your equipment or cause data loss. 6-mo warranty. Power dissipation (100 microseconds): 2,000,000 watts

PART NO.	DESCRIPTION	PRICE
MODEL 75	4 Sockets, On/Off Switch.	$49.95
MODEL 85	6 Sock., Super Filters, On/Off Switch. . . .	$59.95
MODEL 100	6 Sock., Super Filters, Low Volt. Alarm. . .	$69.95
MODEL 110AMS	6 Sockets, Super Filters, Auto. Master Switch.	$99.95



DATASHIELD® Back-Up Power Source

Protect your computer from black-outs, brown-outs, power surges and line noise. PTI's PC200 is designed for PCs with floppy disk memory, the XT300 for hard disk memory and the AT800 for multi-user systems. A typical compatible PC for each of these standbys will be supported for 15 to 25 minutes after power is lost. Weight (PC200: 24 lbs.) — (XT300: 37.5 lbs.) — (AT500: 83 lbs.) — (AT800, 83 lbs.)

PC200	(200 Watt Rating).	$299.95
XT300	(300 Watt Rating).	$399.95
AT500	(500 Watt Rating).	$699.95
AT800	(800 Watt Rating).	$799.95

ProModem 1200 and Options



Intelligent 300/1200 Baud Telephone Modem with Real Time Clock/Calendar

The ProModem™ Is a Bell 212A (300/1200 baud) intelligent stand-alone modem • Full featured expandable modem • Standard features include Auto Answer and Auto Dial, Help Commands, Programmable Intelligent Dialing, Touch Tone™ and Pulse Dialing & More • Hayes command set compatible plus an additional extended command set • Shown w/alphanumeric display option.

Part No.	Description	Price
PM1200	RS-232 Stand Alone Unit.	$349.95
PM1200A	Apple II, II+ and //e Internal Unit.	$369.95
PM1200B	IBM PC and Compatible Internal Unit.	$269.95
PM1200BS	IBM PC & Comp. Int. Unit w/ProCom Software.	$319.95
MAC PAC	Macintosh Package. . . . . (Includes PM1200, Cable, & ProCom Software)	$399.95

OPTIONS FOR ProModem 1200

PM-COM	(ProCom Communication Software). . . . . Please specify Operating System.	$79.95
PM-OP	(Options Processor).	$79.95
PMO-16K	(Options Processor Memory – 16K).	$10.95
PMO-32K	(Options Processor Memory – 32K).	$20.95
PMO-64K	(Options Processor Memory – 64K).	$39.95
PM-ALP	(Alphanumeric Display).	$79.95
PM-Special	(Includes Options Processor, 64K Memory and Alphanumeric Display).	$189.95

KEYBOARDS



13⅛"L x 4¼"W x ¾"H

Mitsumi 54-Key Unencoded All-Purpose Keyboard

• SPST keyswitches • 20 pin ribbon cable connection • Low profile keys • Features: cursor controls, control, caps (lock), function, enter and shift keys • Color (keycaps): grey • Wt.: 1 lb. • Pinout included

KB54. . . . . $14.95

New!

82-Key ASCII Cherry Keyboard

• 7-bit parallel ASCII • 11-key numeric keypad • Cursor keypad • SPST mechanical keyswitches • 4 illuminated keys • 26-pin header connector Color: white • Size: 18"L x 6¾"W x 1¼"H • Spec included

KB8201. . . . (1700 avail.). . . . $29.95

Apple Owners!

SPECIAL FUNCTIONS!

Apple Keyboard and Case for Apple II and II+

Keyboard: • 68 keys • 15-key keypad • Direct connection with 16-pin ribbon connector • 26 special functions • Size: 14½"L x 5½"W x 1½"H

Case: Accommodates KB-A68 • Pop-up lid for easy access • Fits power supply and motherboard too • Size: 15½"W x 18"D x 4¼"H

Part No.	Description	Price
KB-EA1	Apple Keyboard and Case (pictured above).	$134.95
KB-A68	68-Key Apple Keyboard only.	$79.95
EAEC-1	Expanded Apple Enclosure Case only.	$59.95

POWER SUPPLIES



Power/Mate Corp. REGULATED POWER SUPPLY

• Input: 105-125/210-250 VAC at 47-63 Hz • Line regulation: ±0.05% • Three mounting surfaces • Overvoltage protection • UL recognized • CSA certified

Part No.	Output	Size	Weight	Price
EMA5/6B	5V@3A/6V@2.5A	4⅞"L x 4"W x 2⅛"H	2 lbs.	$29.95
EMA5/6C	5V@6A/6V@5A	5⅝"L x 4⅞"W x 2⅞"H	4 lbs.	$39.95

KEPCO/TDK 4-OUTPUT SWITCHING POWER SUPPLY

• **Ideal for disk drive needs of CRT terminals, microcomputers and video games** • Input: 115/230VAC, 50/60Hz • Output: +5V @ 5 Amp, +12V @ 1.8 Amp, +12V @ 2 Amp, -12V @ 0.5 Amp • UL recognized • CSA certified • Size: 7⅜"L x 6-3/16"W x 1⅝"H • Weight: 2 lbs. **$59.95 each or**

MRM 174KF. . . . . 2 for $99.95



Switching Power Supply for APPLE II, II+ & //e™

• Can drive four floppy disk drives and up to eight expansion cards • Short circuit and overload protection • Fits inside Apple computer • Fully regulated +5V @ 5A, +12V @ 1.5A, -5V @ .5A, -12V @ .5A • Direct plug-in power cord included • Size: 9⅞"L x 3½"W x 2¼"H • Weight: 2 lbs.

KHP4007 (SPS-109). $59.95



4-CHANNEL SWITCHING POWER SUPPLY

• Microprocessor mini-computer, terminal, medical equipment and process control applications • Input: 90-130VAC, 47-440Hz • Output: +5VDC @ 5A, -5VDC @ 1A, +12VDC @ 1A, -12VDC @ 1A • Line regulations: ±0.2% • Ripple: 30mV p-p • Load regulation: ±1% • Overcurrent protection • Adj: 5V main output ±10% • Size: 6⅜"L x 1⅞"W x 4-15/16"H • Weight: 1½ lbs.

FCS-604A. $69.95

New!

IBM PCXT EQUIVALENT 130 WATT POWER SUPPLY

UPGRADE YOUR PC!

• Input: 100V-130V/200V-260V selectable @ 47 to 63Hz • Output: +5VDC @ 15A, -5VDC @ 0.5A, +12VDC @ 4.2A, -12VDC @ 0.5A • Plug compatible connectors • Fits into IBM PC • Weight: 6 lbs.

IBM-PS. $169.95

$10.00 Minimum Order — U.S. Funds Only
California Residents Add 6½% Sales Tax
Shipping — Add 5% plus $1.50 Insurance
Send S.A.S.E. for Monthly Sales Flyer!

Spec Sheets — 30¢ each
Send $1.00 Postage for your
FREE 1985 JAMECO CATALOG
Prices Subject to Change





1355 SHOREWAY ROAD, BELMONT, CA 94002

4/85 ***PHONE ORDERS WELCOME — (415) 592-8097 Telex: 176043***

Apple® Accessories

5¼" APPLE™ Direct Plug-In Compatible Disk Drive and Controller Card

The ADD-514 Disk Drive uses Shugart SA390 mechanics—143K formatted storage • 35 tracks • Compatible with Apple Controller & ACC-1 Controller • The drive comes complete with connector and cable — just plug into your disk controller card • Size: 6"L x 3½"W x 8-9/16"D • Weight: 4½ lbs.

ADD-514 (Disk Drive). $169.95
ACC-1 (Controller Card). . . . . $ 49.95

More Apple Compatible Add-Ons...

APF-1	(Cooling Fan with surge protection). . . .	$39.95
KHP4007	(Switching Power Supply).	$59.95
JE614	(Numeric/Aux. Keypad for //e).	$59.95
KB-A68	(Keyboard w/Keypad for II & II+).	$79.95
MON-12G	(12" Green Monitor w/swivel stand). . . .	$99.95
JE864	(80 Col. +64K RAM for //e).	$99.95
ADD-12	(5¼" Half-Height Disk Drive).	$179.95



ADDITIONAL APPLE™ ADD-ONS AVAILABLE

ARC-16K	(16K RAM Card for Apple II & II+)	$39.95
AEB-2	(EPROM Burner for Apple II, II+ & //e) . . Allows copy of standard EPROMS 2708, 2716, 2732, 2764	$69.95
ASSC-P	(Super Serial Card for Apple II, II+ & //e) . .	$99.95
ADD-IIc	(5¼" Half-Ht. Disk Drive for Apple //c)	$189.95

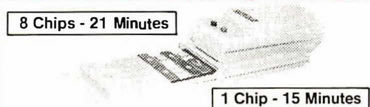
DISK DRIVES



MPI51S	(MPI 5¼" SS full-ht.).	$ 89.95
RFD480	(Remex 5¼" DS full-ht.).	$109.95
TM100-2	(Tandon 5¼" DS full-ht.). . . .	$159.95
FD55B	(Teac 5¼" DS half-ht.).	$149.95
SA455	(Shugart 5¼" DS half-ht.). . . .	$159.95
FDD100-8	(Siemens 8" SS full-ht.).	$119.95
PCK-5	(5¼" Power Cable Kit).	$2.95
PCK-8	(8" Power Cable Kit).	$3.95

UV-EPROM Eraser

8 Chips - 21 Minutes



1 Chip - 15 Minutes

Erases all EPROMs. Erases up to 8 chips within 21 minutes (1 chip in 15 minutes). Maintains constant exposure distance of one inch. Special conductive foam liner eliminates static build-up. Built-in safety lock to prevent UV exposure. Compact — only 9.00"L x 3.70"W x 2.60"H. Complete with holding tray for 8 chips.

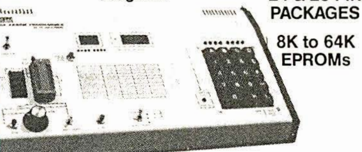
DE-4 UV-EPROM Eraser. $74.95
UVS-11EL Replacement Bulb. $16.95

JE664 EPROM PROGRAMMER

See Our New IBM Communications Program!

24 & 28 PIN PACKAGES

8K to 64K EPROMs



REQUIRES NO ADDITIONAL SYSTEMS FOR OPERATION

Programs and validates EPROMs • Checks for properly erased EPROMs • Emulates PROMs or EPROMs • Loads data in RAM by keyboard • Changes data in RAM by keyboard • Loads RAM from an EPROM • 664 RAMs can be used for external microprocessor development • Compares EPROMs for content differences • Copies EPROMs • Input: 115VAC @ 60Hz • Assembled and tested • Size: 15⅝"L x 8¾"D x 3½"H • Wt: 5¾ lbs • **2716 Module included**

JE664-A EPROM Programmer. $995.00

JE665-RS232C INTERFACE OPTION — This option implements computer access to the JE664's RAM, allowing computer to manipulate, store, and transfer EPROM data to and from the JE664. Sample program listing is supplied in MBASIC for CP/M computers • Documentation provided to adapt the software to other computers with an RS232 port • Specs: 9600 Baud, 8-bit word, odd parity with 2 stop bits • Assembled and tested • **2716 Module included**

JE664-ARS EPROM Programmer w/JE665 Option. $1195.00

JE664-ARS COMMUNICATION PROGRAM For IBM-PC or XT and Compatibles

• Fast compiled BASIC program • Easy to use, menu-driven • Print hard-copies of EPROM data • View data in HEX and ASCII **NEW!**

The JE664-ARS Communication Program was written for quick interfacing between the JE664-ARS EPROM Programmer and the IBM-PC computer and compatibles. Menu-driven program allows user to Load and Save EPROM data to and from the computer or floppy disk. Data entered by the computer can be viewed in Hex & ASCII formats. Printed hard-copies are also displayed in both formats. Program is ideal for keeping archives of master EPROMs on disk. The program is compatible for all EPROMs listed with the JE664. Computer requirements: IBM-PC, XT (or eq.) with at least 128K RAM and one serial port. Optional: One parallel port for printer

JE664-ARS-CP. $49.95
JE664-ARS Communications Program (5¼" Disk and User's Instructions)

JE664-CP CABLE. $29.95
Cable for IBM-PC to JE664-ARS Program (5' Shielded Cable & Connectors)

JUMPER (Personality) MODULES — Jumper (Personality) Modules for 8K, 16K, 32K, and 64K EPROMs. *Please specify EPROM and manufacturer.
JUMPER (Personality) MODULE *________________ . . . . $14.95 each

tially beneficial application of computers. Schools should be paying attention to computers not because they will take over our lives or because everyone has to be a programmer but because computers are part of the solution to education problems.

THE FUTURE

Computers will be really useful to the average person only when they can be used with no training at all. Schank sees advisory systems in areas such as finance, medicine, and law becoming available within the next few years. Sophisticated learning systems, with cognitive abilities, will be available within a decade, Schank says. And within 50 years, he predicts, there will be integrated world-knowledge systems capable of learning about new domains; their most effective role will be as librarians and consultants, figuring out what we need to know about a subject and the right way to explain it to us.

AI may change the way we look at ourselves. One of its by-products will be the opportunity for an informed public. People lack the information they need because they don't want to appear stupid, bother an expert, or pay lots of money for advice. In the future, people will be able to obtain expert advice of all kinds, easily, quickly, and inexpensively from computers. Of course, we should evaluate computer advice as carefully as we would that from any other advisor with a stake in our decision.

CRITICISM

Schank is best, and worst, when hypothesizing. He has made a career out of playing mind games, and most of those he presents are fascinating. However, he occasionally slips into an overly optimistic view of computers and the future. He says that machines will take over the most unpleasant human jobs and will provide people with the information they need to run their daily lives. I think this will be more a function of what people seek rather than simply what computers can provide.

AUDIENCE

The Cognitive Computer is not for those people who are interested in the engineering behind AI programs. Schank does not include details on how AI programs go together, what languages they are written in, and what kinds of hardware they run on. His contribution is to put thinking computers in perspective and show us where we can go with them.

It is a credit to his science of understanding how humans understand that Schank writes with such clarity. He demonstrates a genuine concern for how computers and their AI software will affect human lives. Schank has a healthy perspective on scientific progress: he doesn't believe that every aspect of human thought can or should be modeled on computers. ■

Darrow Kirkpatrick is an applications engineer at Development Associates Controls (POB 1049, *Carpinteria*, CA 93013).

You can buy a less expensive diskette and not save a thing.

One can understand the temptation to buy a less expensive diskette.

Rather than a Dysan® diskette.

After all, the less expensive diskette is probably almost as good. And should you run into a bad one, well, it didn't cost that much, anyway.

Right? Not quite.

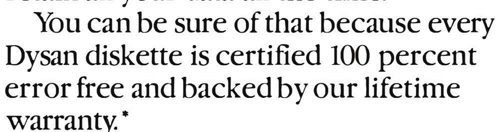
You see, a less expensive diskette is by definition less diskette. And the few pennies you save are worth a great deal less than what you have to lose.

Namely, your data.

That's why it makes more sense to spend a bit more for a Dysan diskette.

Every Dysan diskette you buy will record and retain all your data all the time.

You can be sure of that because every Dysan diskette is certified 100 percent error free and backed by our lifetime warranty.*



So next time you're tempted to buy a less expensive diskette, ask yourself this question.

Can you really afford it?

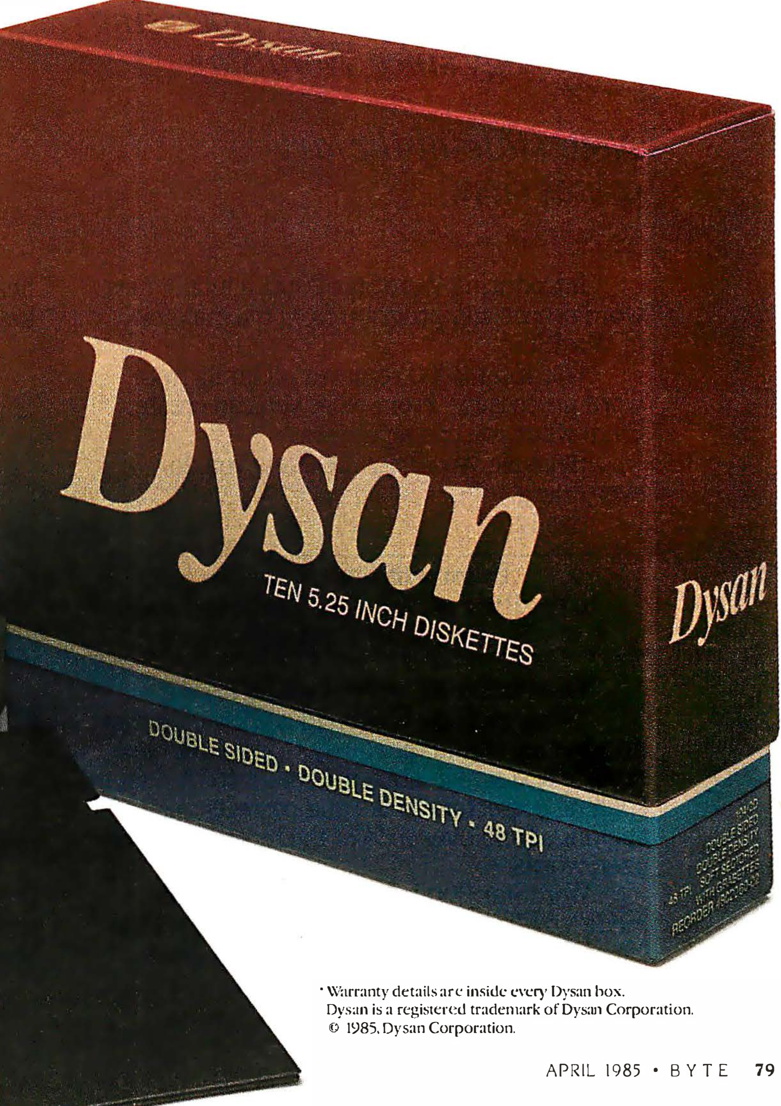
For the name of the Dysan dealer nearest you, call toll free (800) 551-9000.

Dysan Corporation, 5201 Patrick Henry Drive, P.O. Box 58053, Santa Clara, CA 95050.



Inquiry 131

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Announcing the first major breakthrough in word processing technology since WordStar.

Now, state-of-the-art comes easy.

Introducing WordStar 2000, a totally new word processing program from the makers of WordStar.

WordStar 2000 removes all limits from word processing. From what you can create. From what you can achieve.

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Easily.

From windows, to undo, to spelling correction, WordStar 2000 does it all. And more.

WordStar 2000 gives you the works.

"Windows" allows you to work on different documents—simultaneously. "Undo" lets you replace text you mistakenly removed. A built-in spelling corrector checks and corrects misspellings from over 97% of the most commonly used words.

WordStar 2000 also has a "typewriter mode" to fill in forms or envelopes easily. Plus "format sheets," which give you ready-made headings, tabs and margins at the touch of one key. It can even create and update footnotes.

Finally, a truly integrated word processing system.

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It comes with a built-in five function math. A built-in mail merge enables you to mass produce form letters. Get our special Plus package and you also get a built-in mail list data base that allows you to create, update and sort your own mailing lists. Also a built-in indexer. Not to mention built-in telecommunications capabilities.

All integrated together, so you never have to leave the program.

The only word processing program that interacts with you on your level, whatever your level.

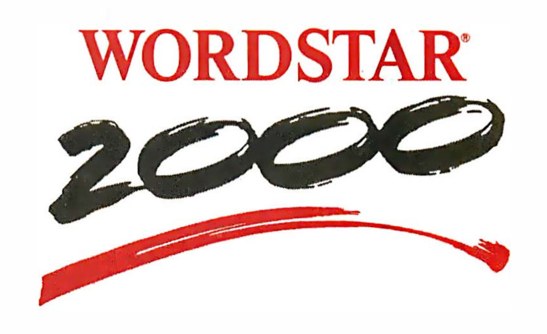
Before we created WordStar 2000, we studied the way people worked, and thought. We also drew from our experience with over 1,250,000 WordStar owners.

As a result, the keys you press are the keys you'd expect to press ("c" for copy, "p" for print, etc.). You may also use your computer's function keys. Menus have been uniquely designed for easy access to all functions. And MicroPro's exclusive "tutor-in-your-computer™" makes learning fast and fun.

WordStar 2000 is the easy word processing program you'll never outgrow. Of course, the original WordStar and WordStar for PCjr will continue to provide substantial and proven word processing capability for those with more modest budgets.

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Now available for IBM PC/AT*/XT* and compatibles with 256K RAM. Upgrade from WordStar to WordStar 2000 through your dealer, or call MicroPro Customer Update (800) 227-5609, 9am-3pm P.S.T.*

Now there are no limits.™



April 1985

● BUSINESS SHOW
Business-Expo, various sites throughout the U.S. This show features exhibits and services related to office technology. Contact International Business Expositions Inc., 200 East Northland Towers, 15565 Northland Dr., Southfield, MI 48075-5378, (313) 569-8280. *April–May*

● ROBOTICS, MATHEMATICS, COMPUTER LECTURES—Robotics Lecture Series and Colloquium Series, Room W-117, Mathematics & Science Building, Montclair State College, Upper Montclair, NJ. Monthly lecture series featuring experts in computer science, mathematics, and robotics. Contact Gideon Nettler, Department of Mathematics and Computer Science, Montclair State College, Upper Montclair, NJ 07043, (201) 893-4294 or (201) 893-5132. *April–May*

● INTELLIGENT MACHINES
Machine-Intelligence Classes, Turing Institute, Glasgow, Scotland. Among the classes offered are "Foundations of Artificial Intelligence" and "Cognitive Modeling as a Basis for Expert Systems." Contact The Turing Institute, George House, 36 North Hanover St., Glasgow G1 2AD, Scotland; tel: 041-552-6400. *April–June*

● MEMORY CARDS STUDIED—Memory-Card Technology, Columbus, OH. Business, industrial, and technological concerns will be addressed. Panel discussions and exhibits. The fee is $495. Contact Phil Wells, Battelle Memorial Institute, 505 King Ave., Columbus, OH 43201-2693, (614) 424-7249. *April* 10–11

● SYSTEMS DEVELOPMENT AND FOURTH GENERATION—Structured Techniques Using Fourth Generation Languages, Chicago, IL. This seminar explains how to use fourth-generation languages in a structured systems development environment. Contact Digital Consulting Associates Inc., 6 Windsor St., Andover, MA 01810, (617) 470-3870. *April* 10–12

● COMMUNICATIONS TECHNOLOGY FOR THE NONVERBAL—The Fourth Annual Conference on Communication Technology: Technology and Nonspeaking Children, Joseph Stokes Auditorium, Children's Hospital of Philadelphia, PA. Up-to-the-minute information on the use of technology with nonverbal children will be presented. Concurrent sessions will address ongoing research, computers, and treatment strategies. The registration fee is $95. Contact Joan Bruno, Children's Seashore House, 4100 Atlantic Ave., POB 4111, Atlantic City, NJ 08404, (609) 345-5191, ext. 278. *April* 12–13

● MAC IS FEATURED
MacFair, Creese Student Center, Drexel University, Philadelphia, PA. Seminars, demonstrations, and exhibits. Student-sponsored. Contact MacFair, The DUsers, Creese Student Center, Drexel University, Philadelphia, PA 19104, (215) 895-2573. *April* 13

● COMPUTERS AND PEOPLE—CHI '85: Human Factors in Computing Systems, Hyatt Regency at Embarcadero Center, San Francisco, CA. Contact ACM Conference Management, 11 West 42nd St., New York, NY 10036, (212) 869-7440. *April* 14–18

● OPTICAL STORAGE INVESTIGATED—The 1985 Materials Research Society: Symposium D, Golden Gateway Holiday Inn, San Francisco, CA. The mass-storage technologies symposium will investigate optical data storage. Areas to be addressed include write-once and erasable media, read-only technology, substrates, and lasers. Contact D. H. Davies, Symposium Co-Chair, 3M, 420 North Bernardo Ave., Mountain View, CA 94043. *April* 15–18

● SEMINAR CONSIDERS CAD—Computer-Aided Design, Ramada Inn, Rochelle Park, NJ. A seminar featuring PCAD and AutoCAD products. Contact Compu-Sales Corp., 1096 Goffle Rd., Hawthorne, NJ 07506, (201) 427-5949. *April* 16

● BUCKEYE SHOW
The Ninth Annual Computer Fair, University of Dayton Arena, OH. Terminals, microcomputers, and word processors to be displayed. Contact Dan Schumacher, University of Dayton, 300 College Park Ave., Dayton, OH 45469, (513) 229-3511. *April* 16–17

● DBM AND FOURTH GENERATION—Database Management Systems and Fourth Generation Languages for Personal Computers, Atlanta, GA. Topics include approaches for managing data, operational considerations, and management issues. The fee is $795. Contact Software Institute of America Inc., 8 Windsor St., Andover, MA 01810, (617) 470-3880. *April* 17–19

● OFFICE, DP EQUIPMENT
CeBIT '85, Hannover, West Germany. More than 1300 exhibitors from more than 25 countries will display office equipment and data-processing technology. Held in conjunction with the Hannover Fair. Contact Hannover Fairs Information Center, Route 22 East, POB 338, Whitehouse, NJ 08888, (800) 526-5978; in New Jersey, (201) 534-9044. *April* 17–24

● NETWORK CONTROL AND MANAGEMENT
Network Management/Technical Control, Marriott Copley Place, Boston, MA. Diagnostic and test instruments will be among the products displayed. Contact Louise Myerow, Registration Manager, CW/Conference Management Group, 375 Cochituate Rd., POB 880, Framingham, MA 01701, (800) 225-4698; in Massachusetts, (617) 879-0700. *April* 18–19

IF YOU WANT *your organization's public activities listed in* BYTE*'s* Event Queue, *we need to know about them at least four months in advance. Send information about computer conferences, seminars, workshops, and courses to* BYTE, Event Queue, POB 372, Hancock, NH 03449.

(continued)

EVENT QUEUE

● COMPUTER FESTIVAL
The Tenth Annual Trenton Computer Festival, Trenton State College, Trenton, NJ. Talks, tutorials, user-group activities, exhibits, computer-graphics theater, games, and a 50-acre outdoor electronics flea market are some of the highlights of this annual event. Contact Ms. Marilyn Hughes, Trenton State College, Hillwood Lakes CN 550, Trenton, NJ 08625, (609) 771-2487. *April 20–21*

● AIDS FOR EDUCATORS
AEDS/ECOO '85: The Twenty-Third Annual Convention of the Association for Educational Data Systems (AEDS), Hilton Harbour Castle, Toronto, Ontario, Canada. A forum for educators to exchange experiences and to keep up to date on developments in educational computing. The theme is "Computing Knows No Borders." Co-hosted by the Educational Computing Organization of Ontario (ECOO). Contact AEDS/ECOO '85, c/o OISE, 252 Bloor St. W, Toronto, Ontario M5S 1V6, Canada; in the U.S., AEDS/ECOO '85, 1201 16th St. NW, Washington, DC 20036. *April 21–27*

● CAD FOR ARCHITECTURE, ENGINEERING
CADDMania: Causes and Cure, Sheraton Twin Towers, Orlando, FL. Techniques for computer-aided design and drafting for architecture and engineering. The fee for the full three days is $175; the daily rate is $100. Contact Pat Johnson, CEPA Inc., 15713 Crabbs Branch Way, Rockville, MD 20855, (301) 926-7070. *April 22–24*

● SPEECH IN FOCUS
Speech Tech '85, Vista International Hotel, World Trade Center, New York City. Speakers and exhibitors will focus on voice synthesis and recognition. Registration is $195. Contact Media Dimensions Inc., POB 1121 Gracie Station, New York, NY 10028, (212) 772-7068 or (212) 680-6451. *April 22–24*

● DECISION-SUPPORT DISCUSSED—National Conference on Decision-Support Systems, Washington, DC. Examines the implementation and integration strategies of decision-support systems into management. Two days of workshops. The fee is $745. Contact Conference Manager, U.S. Professional Development Institute, 1620 Elton Rd., Silver Spring, MD 20903, (301) 445-4400. *April 22–25*

● PUBLIC NETWORK OPERATIONS—X.25 and Packet Switching Networks, Atlanta, GA. This course covers the internal operations of a packet-switching network and its implementation. International standards are also covered. The fee is $795. Contact Elaine Hadden Nicholas, Department of Continuing Education, Georgia Institute of Technology, Atlanta, GA 30332-0385, (404) 894-2547. *April 23–25*

● TRADE SHOW, CONFERENCE—Electro/85 and Mini/Micro Northeast-85, New York City. Areas to be covered include artificial intelligence, communications and networks, consumer electronics, high-density data storage, and personal computing. Contact Electronic Conventions Management, 8110 Airport Blvd., Los Angeles, CA 90045, (213) 772-2965. *April 23–25*

● COMPUTER APPLICATIONS EXPLORED
Perscomp '85, Sofia, Bulgaria. An international conference on the applications of personal computers and the problems encountered in using them. Contact Dr. Marcel Israel,

Bulgarian Academy of Sciences, Institute of Industrial Cybernetics and Robotics, 113 Sofia, Acad. G. Bonchev St., Bl. 12, Bulgaria; tel: 72-46-98; Telex: 22836 ITKR BG. *April 23–26*

● EXPERT SYSTEMS
Expert Systems and Knowledge Engineering, Gottlieb Duttweiler Institute, Ruschlikon/Zurich, Switzerland. The theme is "Essential Elements of Advanced Information Technology." Contact Dr. T. Bernold, Gottlieb Duttweiler Institute, CH-8803, Ruschlikon/Zurich, Switzerland. *April 25–26*

● MICROS IN EMPIRE STATE—The Fourth Annual New York Computer Show and Software Exposition, Nassau County Coliseum, Uniondale, NY. Contact Ann Katcef, CompuShows, POB 3315, Annapolis, MD 21403, (800) 368-2066; in Annapolis, (301) 263-8044; in Baltimore, (301) 269-7694; in the District of Columbia, (202) 261-1047. *April 25–28*

● VIRGINIA COMPUTING
The Fourth Annual Virginia Computer Show and Software Exposition, Pavilion, Virginia Beach, VA. Contact Ann Katcef, CompuShows, POB 3315, Annapolis, MD 21403, (800) 368-2066; in Annapolis, (301) 263-8044; in Baltimore, (301) 269-7694; in the District of Columbia, (202) 261-1047. *April 25–28*

● EQUIPMENT SALE
Produx 2000: Wholesale Expo '85, Civic Center, Philadelphia, PA. Six hundred booths of computers, communications devices, and business equipment for sale. Contact Vertical Marketing Corp., POB 557, Bala Cynwyd, PA 19004, (215) 457-2303. *April 26–28*

● SPRING WITH COMMONERS—COMMON's Spring '85 Conference, Louisville, KY. More than 250 presentations are planned. Contact COMMON, Spring '85 Conference, Suite 1717, 435 North Michigan Ave., Chicago, IL 60611, (312) 644-0828. *April 27–May 1*

● INTELLIGENT VISION
Intelligent Vision Systems, Holiday Inn, Monterey, CA. The technical and marketing aspects of intelligent vision will be covered. Contact Richard D. Murray, Institute for Graphic Communication Inc., 375 Commonwealth Ave., Boston, MA 02115, (617) 267-9425. *April 28–30*

● INTRO TO UNIX
Introduction to the UNIX System, Atlanta, GA. The pros and cons of UNIX will be covered. Contact Digital Consulting Associates Inc., 8 Windsor St., Andover, MA 01810, (617) 470-3870. *April 29–30*

● C FOR ENGINEERS
C Programming for Engineers, University of Michigan, Dearborn. A short course and workshop. Contact Professor R. E. Little, University of Michigan, 4901 Evergreen Rd., Dearborn, MI 48128, (313) 593-5241. *April 29–May 3*

● KNOWLEDGE ENGINEERING—Knowledge Engineering: A Short Course, University of Tennessee Space Institute, Tullahoma. Contact Professor Moonis Ali, University of Tennessee Space Institute, Tullahoma, TN 37388-8897, or call the Short Course Office at (615) 455-0631, ext. 278. *April 29–May 3*

● COMMERCIAL AI, HIGH-TECH CONFERENCE—AI 1985: Artificial Intelligence and Advanced Computer Technology Conference/Exhibition, Convention Center, Long Beach, CA. More than 20 technical sessions as well

(continued)

EVENT QUEUE

as panel discussions and product displays are planned. Contact Tower Conference Management Co., 331 West Wesley St., Wheaton, IL 60187, (312) 668-8100. *April 30–May 2*

● MEETING ON LINE
National Online Meeting, Sheraton Centre Hotel, New York City. On the docket are formal paper presentations, product review sessions, exhibits, and special workshops and seminars transmitted via satellite. Contact Thomas Hogan, National Online Meeting, Learned Information Inc., 143 Old Marlton Pike, Medford, NJ 08055, (609) 654-6266. *April 30–May 2*

May 1985

● SUMMER SEMINARS
Summer Seminar Series, Rochester Institute of Technology, NY. A series of one-week seminars. Titles include "Introduction to Linear Systems and Digital Signal Processing," "Basic 6800/6809," and "Advanced Digital Logic." Contact Yvonne Fish, School of Engineering Technology, Rochester Institute of Technology, One Lomb Memorial Dr., POB 9887, Rochester, NY 14623, (716) 475-2915. *May–June*

● MICROELECTRONIC ENGINEERING
Microelectronic Engineering Conference, Rochester Institute of Technology, NY. Technical papers and tours of microelectronic engineering facilities. Contact Dr. Lynn Fuller, Microelectronic Engineering Program, Rochester Institute of Technology, One Lomb Memorial Dr., POB 9887, Rochester, NY 14623, (716) 475-2035. *May 1*

● SCIENTIFIC COMPUTING AND AUTOMATION—The First Scientific Computing and Automation Conference and Exposition, Convention Center, Atlantic City, NJ. For practitioners and managers in analytic chemistry, biotechnology/biomedical research, clinical chemistry, and engineering. Product displays. Contact Expocon Management Associates Inc., 3695 Post Rd., Southport, CT 06490. *May 1–3*

● SPECIAL EDUCATION SOFTWARE—National Conference on Special Education Software, Radisson Mark Plaza, Alexandria, VA. The theme is "DISCover the Possibilities." Product displays and demonstrations. Registration: $50. Contact Elsa Glassman, The Council for Exceptional Children, Department of Professional Development, 1920 Association Dr., Reston, VA 22091, (703) 620-3660, ext. 261. *May 2–3*

● COMPUTERS AND WRITING—UCLA Conference on Computers and Writing: New Directions in Teaching and Research, University of California, Los Angeles. Contact Dr. Lisa Gerrard, UCLA Writing Programs, 371 Kinsey Hall, UCLA, Los Angeles, CA 90024, (213) 206-1145. *May 4–5*

● FAULT-TOLERANT DESIGN—Introduction to Fault-Tolerant Microcomputer Systems, Wisconsin Center, Madison. Presentations will emphasize practical applications. The fee is $650. Contact William C. Dries, University of Wisconsin-Extension, Dept. of Engineering and Applied Science, 432 North Lake St., Madison, WI 53706, (800) 262-6243; in Wisconsin, (608) 262-2061. *May 6–8*

● INTEGRATED OPTICS
ECIO '85: The Third Euro-

(continued)

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Lotus 1-2-3	Lotus Symphony	dBase III	FrameWork	MultiMate	WordStar 2000+
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Word Processing Editors
- EASYWRITER II SYSTEM $219
- FANCY FONT $139
- FINAL WORD $189
- MICROSOFT WORD $239
- MICROSOFT WORD W/MOUSE $289
- MULTIMATE $259
- PFS: WRITE $ 95
- SAMNA WORD III $Call
- VOLKSWRITER DELUXE $159
- VOLKSWRITER SCIENTIFIC $309
- THE WORD PLUS (OASIS) $105
- WORD PERFECT $249
- WORDPLUS W/BOSS $319
- WORDSTAR $199
- WORDSTAR 2000 $269
- WORDSTAR 2000+ $319
- WORDSTAR PROFESSIONAL $259
- XYWRITE II+ $229

Spreadsheets/Integrated Packages
- ELECTRIC DESK $209
- ENABLE $459
- FRAMEWORK $339
- LOTUS 1-2-3 $299
- MULTIPLAN $135
- OPEN ACCESS $299
- SMART SYSTEM $559
- SPREADSHEET AUDITOR $ 79
- SUPERCALC 3 $199
- SYMPHONY $419
- TK! SOLVER $269

Desktop Environments
- DESK ORGANIZER $129
- GET ORGANIZED $159
- SIDEKICK $ 45
- SPOTLIGHT $109

Communications/Productivity Tools
- CROSSTALK $105
- PROKEY $ 89
- RELAY $ 99
- SMARTCOM II $109

Database Systems
- ALPHA DATA BASE MANAGER II $179
- CLOUT V 2.0 $139
- CONDOR III $299
- DBASE II $269
- DBASE III $339
- INFOSTAR+ $319
- KNOWLEDGEMAN $269
- PFS: FILE/PFS: REPORT $169
- POWERBASE $219
- QUICKCODE III $169
- R BASE 4000 $259

Languages/Utilities
- CONCURRENT DOS $189
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- DIGITAL RESEARCH C COMPILER $219
- DR FORTRAN 77 $219
- LATTICE C COMPILER $Call
- MICROSOFT C COMPILER $309
- MS BASIC COMPILER $249
- MS FORTRAN $239
- NORTON UTILITIES—NEW $Call
- TURBO PASCAL $45

Project Management
- HARVARD PROJECT MANAGER $219
- HARVARD TOTAL PROJECT MANAGER $299
- MICROSOFT PROJECT $159
- SCITOR PROJECT 5000 W/GRAPHICS $289

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- DOLLARS AND SENSE $119
- FINANCIER II $119
- HOWARD TAX PREPARER 85 $195
- MICROTAX $Call
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- AUTOCAD $Call
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- CHARTMASTER $239
- CHARTSTAR $209
- DR DRAW $199
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- EXECUVISION $259
- GRAPHWRITER COMBO $389
- MS CHART $159
- OVERHEAD EXPRESS $139
- PC DRAW $259
- PC PAINTBRUSH $ 89
- PFS: GRAPH $ 95
- SIGNMASTER $179
- STATPRO $Call
- STATPAK-NWA $329
- STATPAC-WALONICK $299

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- MBA $369
- OPEN SYSTEMS $399
- PEACHTREE $299
- REAL WORLD $469
- STATE OF THE ART $389
- STAR ACCOUNTING PARTNER $249
- STAR ACCOUNTING PARTNER II $599

Hardware *

Multifunction Boards
- AST ADVANTAGE $Call
- AST 6 PAK PLUS (64K) $249
- AST 6 PAK PLUS (384K) $449
- AST MEGAPLUS II (64K) $269
- AST MEGAPAK (256K) $349
- QUADBOARD (64K) $269
- QUADBOARD (256K) $399
- QUADBOARD EXP. (64K) $269
- QUADBOARD EXP. (384K) $469
- QUAD 512 + (64K) $269
- ORCHID BLOSSOM $Call
- PERSYST $Call
- TECMAR CAPTAIN(64K) $279
- TECMAR WAVE (64K) $209

Display Boards
- AST MONOGRAPH PLUS $Call
- EVEREX GRAPHICS EDGE $419
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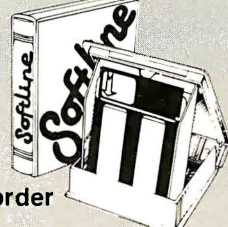
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pean Conference on Integrated Optics, Berlin, Federal Republic of Germany. More than 250 engineers and scientists from Europe, Japan, and the United States will discuss the potential of optics for communication, signal processing, and instrumentation. Contact ECIO '85 Conference Secretariat, Frau I. Weber-Zuckarelli, Heinrich-Hertz-Institut Berlin GmbH, Einsteinufer 37, D-1000 Berlin 10, Federal Republic of Germany. *May 6–8*

● SPRING COMDEX
COMDEX Spring, Atlanta, GA. More than 750 companies will exhibit. Contact The Interface Group Inc., 300 First Ave., Needham, MA 02194, (800) 325-3330; in Massachusetts, (617) 449-6600. *May 6–9*

● MAPLE LEAF COMPUTING—The 1985 Canadian High Technology Show, Civic Centre, Ottawa, Ontario, Canada. Product displays, speakers, and tutorials. Contact Canadian High Technology Show, Suite 214, 2487 Kaladar Ave., Ottawa, Ontario K1V 8B9, Canada, (613) 731-9850. *May 7–8*

● MEMORY CARDS STUDIED—Memory-Card Technology, Crowne Plaza, San Francisco, CA. See April 10–11 for details. *May 8–9*

● PC DISPLAYS
PC Expo, Convention Centre, Montreal, Quebec, Canada. Contact PC Expo, 20 Butterick Rd., Toronto, Ontario M8W 3Z8, Canada, (416) 252-7791. *May 8–10*

● TOPICS IN COMPUTER LAW—The Sixth Annual Computer Law Institute, Los Angeles, CA. Topics on the docket include proprietary rights issues in the design of compatible products, product distribution, and antitrust and copyright issues. Contact Cheryl Litrenta, University of Southern California Law Center, University Park, Los Angles, CA 90007, (213) 743-2582. *May 9–10*

● C CONVOCATION
C85: The First International Conference on the C Programming Language, Ramada Renaissance Hotel, San Francisco, CA. A forum for programmers and developers using or considering the use of the C language. Sessions on ANSI X3J11 standard, portability, programming tools, and applications. Contact Lifeboat Associates, 1651 Third Ave., New York, NY 10128, (800) 847-7078; in New York, (212) 860-0300. *May 13–15*

● GRAPHICS FOR ENGINEERING, DRAFTING
Computer Graphics for Engineering/Drafting Practice and Computer Graphics Workshop, University of Texas, Austin. These short courses stress learning the principles of computer graphics and seek to develop the ability to prescribe computer graphics equipment for engineering applications. Contact College of Engineering, University of Texas, Austin, TX 78712, (512) 471-3506. *May 13–17*

● PROFESSIONAL TUTORIALS—Tutorials for Professional Development, Hyatt Hotel, Los Angeles, CA. A series of all-day seminars on software, logic programming, and communications. Contact Gerry Segal, Association for Computing Machinery, 11 West 42nd St., New York, NY 10036, (212) 869-7440. *May 13–17*

● TEST, MEASUREMENT EXPO—The 1985 Test and Measurement World Expo, Convention Center, San Jose, CA. Conferences and technology exhibits. Contact Meg Bowen, Test and Measurement World Expo, 215 Brighton Ave., Boston, MA 02134, (617) 254-1445. *May 14–16*

● MODULA-2 ENGINEERING—Software Engineering with Modula-2, Atlanta, GA. A course emphasizing methods for building large-scale software systems in Modula-2. Prerequisite: knowledge of Ada or Pascal. The fee is $495. Contact Elaine Hadden Nicholas, Department of Continuing Education, Georgia Institute of Technology, Atlanta, GA 30332-0385, (404) 894-2547. *May 15–17*

● OK SHOW
The Eighth Annual Show & Tell Microcomputer Conference, University of Oklahoma, Norman. Microcomputer fans of all ages and levels of expertise come together to share ideas and demonstrate applications and hardware. Contact Richard V. Andree, Show & Tell Computer Conference, Mathematics Department, University of Oklahoma, 601 Elm St., Norman, OK 73019. *May 18*

● MANAGEMENT CONGRESS—Update '85, Sheraton Hotel, Brussels, Belgium. A briefing covering technological developments for those in the information management and micrographic industries. Contact Update '85, International Information Management Congress, POB 34404, Bethesda, MD 20817, (301) 983-0604. *May 20–22*

● CAD TECHNOLOGY
CAD 2001: The Countdown, Dallas, TX. Presentations on the future of computer-aided design. The fee is $900. Contact CAD Seminars Inc., Suite 400, 150 East Riverside, Austin, TX 78704, (512) 445-7342. *May 22–24*

● SOFTWARE AND HUMAN DEVELOPMENT
Computer Software and Human Development Conference, Royal York Hotel, Toronto, Ontario, Canada. Held in conjunction with the Third Annual Software Panorama, this conference will examine the impact of software development on business, education, health, and agriculture. Contact Reuben Lando, The Software Developers Association, Suite 500, 185 Bloor St. E, Toronto, Ontario M4W 1C8, Canada, (416) 922-1153. *May 22–24*

● DISK STORAGE EXPO
The 1985 International Videodisc, Optical Disk, and CD-ROM Conference and Exposition, London West Hotel, London, England. Workshops, presentations, and exhibitions. Contact Angela Suter, Meckler Communications, 11 Ferry Lane W, Westport, CT 06880, (203) 226-6967; in England, Alice Taylor, Meckler Communications, c/o Eurospan, 3 Henrietta St., London WC2E 8LU, England; tel: 01 240-0856. *May 29–31*

● MANAGE PROGRAMS
Configuration Management of Software Programs, Washington, DC. Methods for controlling the costs of development, maintenance, and operation of software. Contact Stod Cortelyou, Continuing Engineering Education, George Washington University, Washington, DC 20052, (800) 424-9773; in the District of Columbia, (202) 676-8520. *May 29–31*

● COMPUTER INTERFACING—Personal Computer and STD Computer Interfacing for Scientific Automation, Virginia Polytechnic Institute and State University, Blacksburg. A hands-on workshop with participants wiring and testing interfaces. The fee is $450. Contact Dr.

Linda Leffel, C.E.C., Virginia Polytechnic Institute and State University, Blacksburg, VA 24061, (703) 961-4848. *May 30–June 1*

June 1985

● LEARN TO BUILD PROGRAMS—First North American Summer School on Program Construction, Newport, RI. Methods for the effective construction of software will be taught. Contact Teleprocessing Inc., 60 State St., Boston, MA 02109, (617) 367-6227. *June 3–12*

● INTERFACES FOR SCHOOL LABS—Interfacing for School Laboratories, Miami University, Oxford, OH. A workshop for secondary-school and college teachers on the construction and use of interfaces for laboratory instrumentation. Contact Bill Rouse, 301 McGuffey Hall, Miami University, Oxford, OH 45056, (513) 529-2141. *June 3–14*

● COMPUTER MAINTENANCE Independent Computer Maintenance, Halloran House, New York, NY. Contact Carol Every, Frost & Sullivan Inc., 106 Fulton St., New York, NY 10038, (212) 233-1080. *June 5–6*

● OPTICAL-STORAGE CONFERENCE—First Annual Conference on Optical Storage for Small Systems, Biltmore Hotel, Los Angeles, CA. Contact Technology Opportunity Conference, POB 14817, San Francisco, CA 94114-0817, (415) 626-1133. *June 5–7*

● COMPUTERS FOR SALE Computer Supermarket, San Mateo County Fairgrounds, San Mateo, CA. Retailers, manufacturers, and distributors will be selling hardware and software. Admission is $7; children $3. Contact Microshows, Suite 203, 1209 Donnelly Ave., Burlingame, CA 94010, (415) 340-9113. *June 8–9*

● COMPUTER VISION CONFERENCE—Computer Vision and Pattern Recognition Conference, Cathedral Hill Hotel, San Francisco, CA. Submitted and invited technical papers. Contact Computer Vision and Pattern Recognition, POB 639, Silver Spring, MD 20901, (301) 589-8142. *June 9–13*

● MUMPS MEETING The Fourteenth Annual Meeting of the MUMPS Users' Group, McCormick Center Hotel, Chicago, IL. Tutorials, workshops, site visits, discussions, and exhibits. Contact MUMPS Users' Group, Suite 510, 4321 Hartwick Rd., College Park, MD 20740, (301) 779-6555. *June 10–14*

● ROBOTIC STRATEGIES Robot Manipulators, Computer Vision, and Intelligent Robot Systems, University of Stirling, Stirling, Scotland. A short course for professionals emphasizing the development of strategies for the solution of robotic-sensing, spatial-reasoning, and manipulation problems. Contact Director of the Summer Session, Massachusetts Institute of Technology, Room E19-356, Cambridge, MA 02139. *June 10–14*

● NETWORK CONTROL AND MANAGEMENT—Network Management/Technical Control, Santa Clara Marriott, Santa Clara, CA. See April 18–19 for details. *June 12–13*

● CLINICAL COMPUTING Computing in Clinical Laboratories: The Fifth International Conference, Stuttgart, Federal Republic of

(continued)

Germany. Topics on the agenda include databases, data presentation, and expected developments. Demonstrations and exhibits. Contact PD Dr. Chr. Trendelenburg, Katharinenhospital KCI, Kriegsbergstrasse 60, D-7000 Stuttgart 1, Federal Republic of Germany; tel: (07 11) 20 34-4 82. *June* 12–14

● COMPUTERS IN CLINICAL LABS—Clinical Laboratory Computers, Symposium 1985, The Towsley Center, University of Michigan, Ann Arbor. Contact Dove Margenau, Office of Continuing Medical Education, The Towsley Center, Box 057, The University of Michigan Medical School, Ann Arbor, MI 48109-0010, (313) 763-1400. *June* 12–14

● INFO MANAGEMENT EXPO, CONFERENCE Info/West: The Western Information Management Exposition and Conference, Convention Center, Anaheim, CA. Trade show for executives and data-processing and management-information system managers. Contact Info/West, 999 Summer St., Stamford, CT 06905, (203) 964-8287. *June* 12–14

● FORTH CONFERENCE The 1985 Rochester FORTH Conference, University of Rochester, Rochester, NY. The focus will be on software engineering and management. Contact Ms. Maria Gress, Institute for Applied FORTH Research, 70 Elmwood Ave., Rochester, NY 14611, (716) 235-0168. *June* 12–15

● LOGICAL MACHINES CONFERENCE—The Second Annual Conference on Logic, Logic Machines, and Public Education, University of Houston-Clear Lake, Houston, TX. Formal and informal sessions, symposia, and workshops. Contact the Institute for Logic and Cognitive Studies, University of Houston-Clear Lake, Box 269, Houston, TX 77058, (713) 488-9274. *June* 13–15

● INTERNATIONAL SHOW The International Computer Show, Trade Fair Center, Cologne, West Germany. More than 350 manufacturers from more than 18 countries are expected to display their wares. Contact Messe- und Ausstellungs-Ges.m.b.H. Köln, Messeplatz, Postfach 210760, D-5000 Köln 21, West Germany; tel: (0221) 821-1; Telex: 8 873426 mua d. *June* 13–16

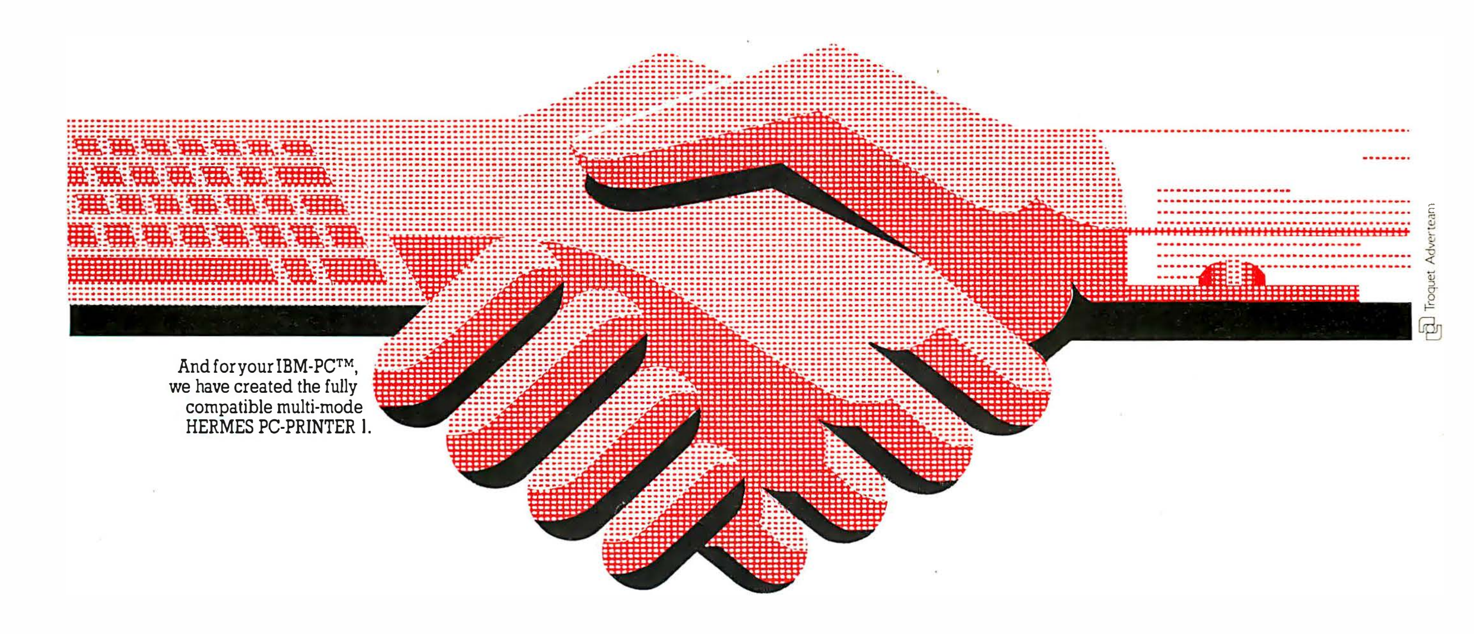
● PC IN BIG APPLE PC Expo, Coliseum, New York, NY. Seminars and product displays. Contact PC Expo, 333 Sylvan Ave., Englewood Cliffs, NJ 07632, (800) 922-0324; in New Jersey, (201) 569-8542. *June* 17–19

● SOFTWARE FOR ENGINEERING—Engineering Software: Engsoft 85, The Fourth International Conference and Exhibition, Kensington Exhibition Centre, London, England. Exhibits and sessions of software for engineering. Contact Elaine Taylor, Computational Mechanics Centre, Ashurst Lodge, Ashurst, Southampton SO4 2AA, England; tel: (042 129) 3223; Telex: 47388 Attn. COMPMECH. *June* 18–20

● GRAPHICS IN SUNSHINE Computer Graphics '85 West, Los Angeles, CA. Contact National Computer Graphics Association, 8401 Arlington Blvd., Fairfax, VA 22031, (703) 698-9600. *June* 25–27

● CAD TECHNOLOGY CAD 2001: The Countdown, Boston, MA. See May 22–24 for details. *June* 26–28 ■

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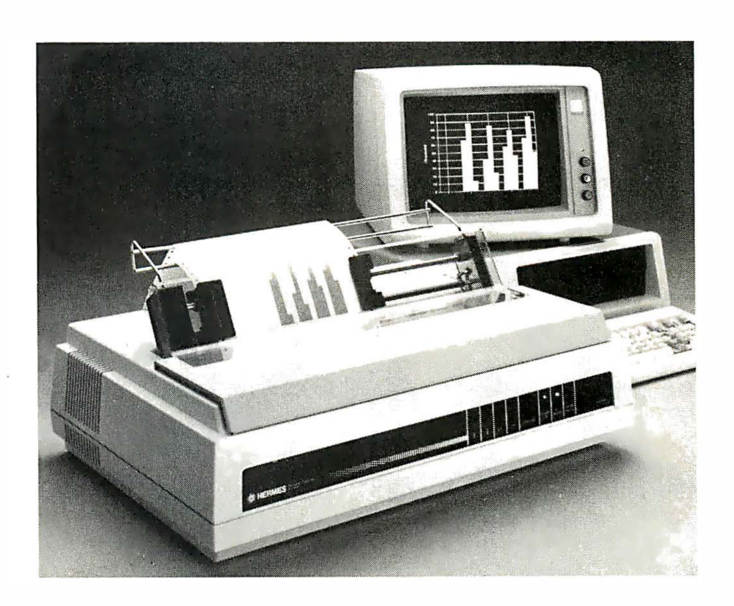
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XEROX

From day one, Xerox and Diablo have been known as the two best names in daisywheel printers. And now there are three more in the Xerox line to choose from.

The Xerox Advantage D-25 Diablo printer turns out letter quality documents quickly and quietly. And it does all that for the price of a dot matrix printer.

At 80 c.p.s., the D-80IF is the fastest daisywheel printer ever made by Xerox. It has a built-in double bin sheet feeder. As well as the capacity to handle up to 16 computers at once.

Team Xerox

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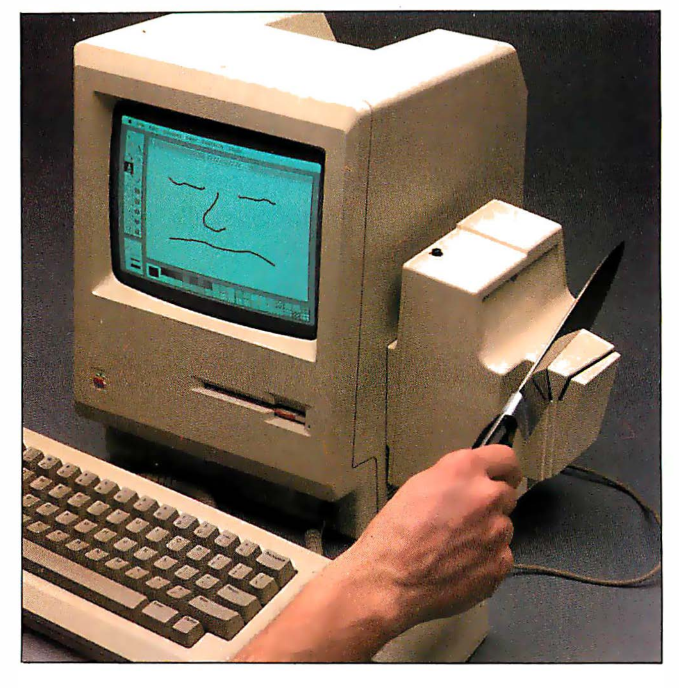
But Xerox didn't stop there. Each of these new machines is compatible with most computers on the market, including the IBM-PC. And they're all easy to use.

They're also a part of Team Xerox, so they can be serviced by the national Xerox service force and authorized service locations across the country.

So if you're looking for the latest in daisywheel printing technology, go with the people who've been in the business the longest. Call 1-800-833-2323, ext. 25, your local Xerox office, an authorized Diablo or Xerox dealer or send your business card to Xerox Corporation, Dept. 25192, P.O. Box 24; Rochester, NY 14692.

For more information from Xerox, circle 405 on the Reader Service card.

Xerox Advantage
D-25 Diablo Printer



Knife the Mac

Ennui Associates has announced MacKnifer, a hardware attachment that mounts on the side of your Macintosh and sharpens knives, scissors, lawn-mower blades—anything in your home that needs sharpening. With MacKnifer's patented double-action grinding wheel, you can easily sharpen any utensil in less time than it takes the Mac to open a file. According to the manufacturer, MacKnifer is so easy to use that you can operate it within 30 minutes of taking it out of the box. Turn your spare computing time into extra cash with a knife-sharpening business on the side . . . of your Macintosh.

For more information on MacKnifer, contact Ennui Associates, 52502 Marginal Ave., Somnolencia, CA 90541.

One for the Road

Honda Corporation has announced the Transporter, the first truly transportable computer. With a few simple twists, you can transform the Transporter from a portable computer (with full keyboard, 24-line by 80-column display, and two microfloppy-disk drives) into a single-passenger automobile.

The Transporter runs on 32 D-cell batteries (not included) with additional one-year battery backup for the ignition, which is in ROM (ride-only memory). Thus, if the Transporter won't start on a chilly winter morning, you can simply give it a cold boot to jog its memory.

Although the Transporter is somewhat heavier than other portable computers, you can easily drive it through airport terminals. Service will be available through AAA (American ASCII Association), which provides pickup and delivery with no tote-charges.

Options include the TP-100 Printer Trailer, the 300-BeePS Modem, and a genuine Naugahyde keyboard cover. Honda has also announced plans to release the SemiPortable, a 20-megabyte hard-disk system that transforms into an 18-wheel tractor/trailer (assembly required).

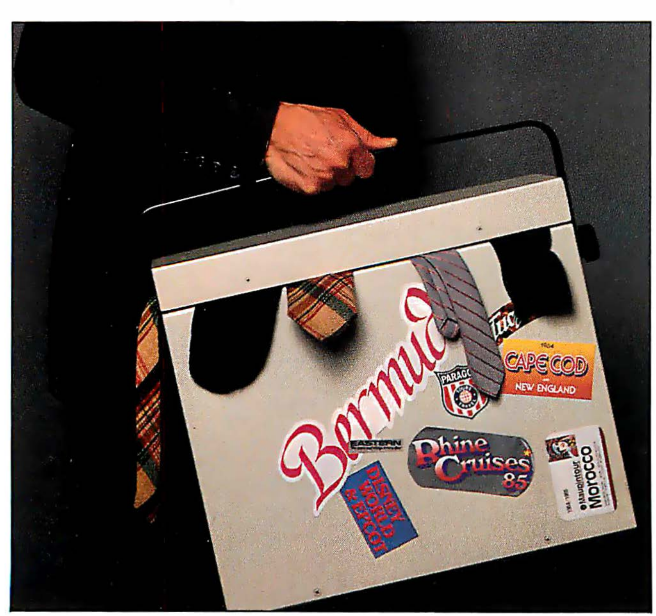
The Transporter is 100 percent compatible with the popular Toyota Corolla and runs on most operating roads. The cost is $5995. For more information, contact Honda Corporation Ltd., 2 Duryea Drive, Minikin, MI 48101.

Nouveau-Chic Luggage

The Spike Untermeyer Luggage Company manufactures hollow replicas of the most popular lap-size and transportable personal computers for use as travel bags by status-conscious travelers. For example, the Untermeyer Executive Portfolio resembles a Tandy Model 100, complete with movable (nonfunctional) keys. The Executive Portfolio flips open to reveal enough space for a pad, appointment calendar, several pens and pencils, or a couple of peanut butter and jelly sandwiches for that quick executive snack. The Untermeyer Overnighter, easily confused with a Compaq, TI, or IBM portable computer, is perfect for that sudden business trip.

Untermeyer luggage is painfully authentic. The Overnighter is exactly half an inch too large to fit under the average coach airline seat, and the bottom of the case is heavily weighted to ensure that nasty crack on the shins when you maneuver past the flight attendant.

For more information, contact the Spike Untermeyer Luggage Company Inc., 442 Glenwood Ave., Prosaic, NJ 22104.



New Arrival

Celebrity Software, maker of the Howard Cosell Word Processor and the Michael Jackson Spreadsheet, has announced the Princess Di Database. If your data is a royal mess, this hierarchical database will arrange things in a neat succession for you. You can obtain output from the system every nine months, with three levels of security: Mum's the Word, Rumor City, and Tell the World.

Available at supermarket checkout counters, the Princess Di Database is priced at $49.95 from Celebrity Software, 135 Pachelbel Canyon, San Regales, CA 90342.

New Mag

High Press Technologies (HipTech) has announced a new publication, *Personal Photocopying*. Designed to make photocopiers less threatening for the average person, the magazine will be written in nontechnical language that explains PRINT, PAUSE, and CANCEL in language that a layperson can understand.

Articles in the first issue of PPC will include "1001 Ways to Make Money with Your Photocopier," "Paper Jam—Deadly Threat to Your Business," and "Big Gray: The Xerox Story."

Based on research done in its own offices, HipTech has also announced *Constant Coffeemaking*. For a one-year subscription to either magazine, send $25 to POB 123123, South Banausic, WI 03458.

Home on the Database

ThinkFast Software has introduced a revolutionary natural-language database designed for home management. MOM, the Model Management program, is a matriarchal database of home-related subjects that responds to plain-English queries. After entering information about your home, age, eating habits, and shoe size, you enter search phrases in the format "Where is the screwdriver?" After a quick pass through its files, MOM responds, "Right where you left it—behind the TV set." Enter the search phrase, "Where are my sneakers?" and MOM responds with lightning speed, "I don't know where your sneakers are; I don't wear your sneakers."

ThinkFast has also announced a product for integration with MOM, one that provides personal advice and guidance. Decisions and Declarations (DAD) responds to the traumas of everyday living with such plain-English messages as, "You want to cry? I'll give you something to cry about!" and "Ask MOM."

MOM and DAD are priced at $99 each from ThinkFast Software, Duitmy Way, Homeville, NC 28210.

A Taste of Security



If merely erasing sensitive data is not enough for you, Soycure Systems of Tokyo has developed the ultimate in disk security. Made entirely of processed soybeans, Parasoya Disks are writable, readable, and edible. Parasoya disks contain 84 percent more protein than average floppy disks and are available in 5¼-inch (regular) and 3½-inch (crunchy) formats.

Available at computer and health stores everywhere, Parasoya Disks are priced at $50 per 10-pack from Soycure Systems, 1 Tufchuying, Tokyo, Japan.

Keeping Time to Yourself

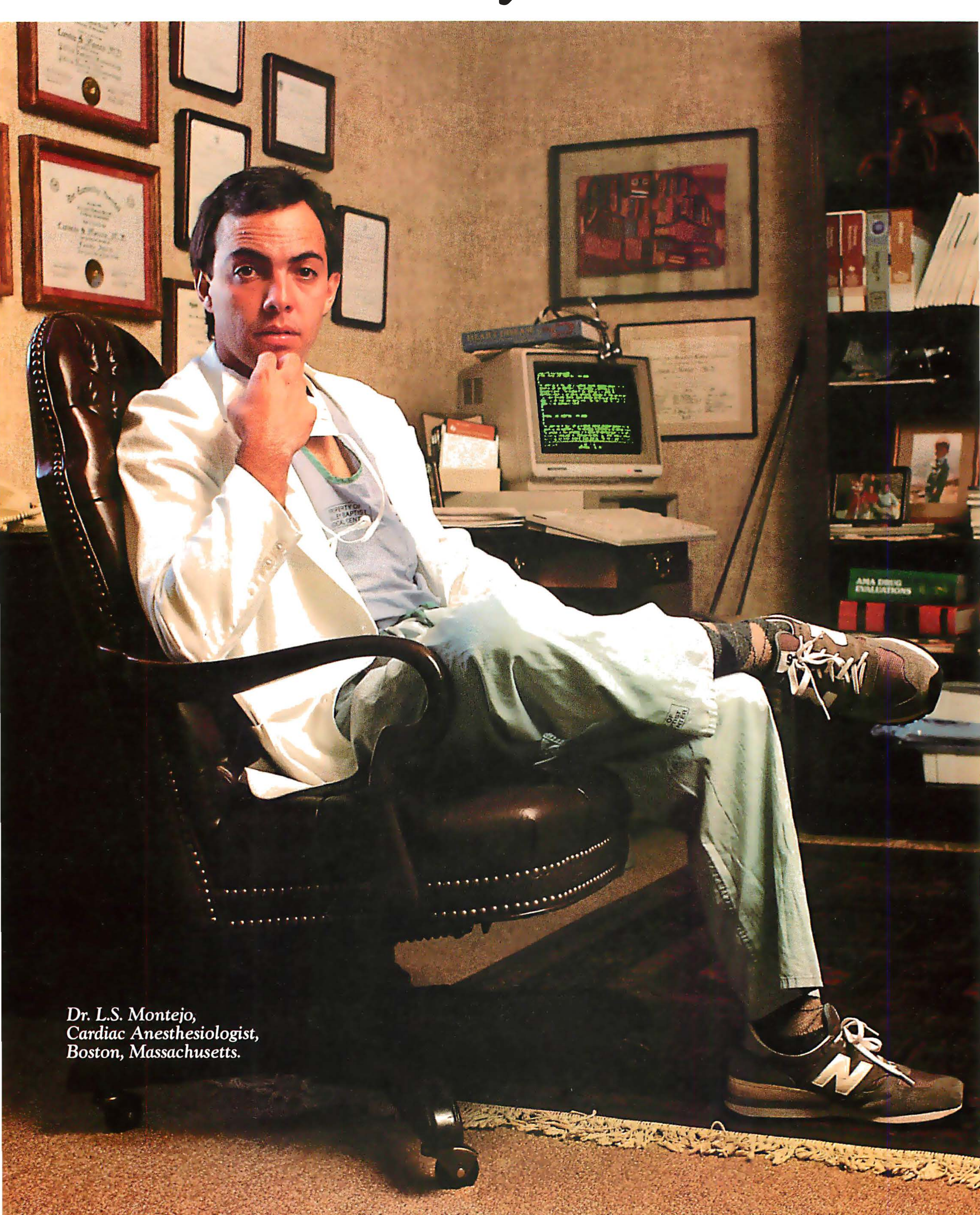
Incognito, a low-profile time-management program for MS-DOS computers, combines an appointment calendar with 200 stock excuses for breaking or avoiding social engagements.

The Incognito calendar's avoidance categories include: My Mate and I; The Car; Kids, Pets, and Relatives; Let Me Check With My . . . (accountant, boss, etc.); I'm Coming Down With . . . ; and Previous Engagement.

Incognito's Fib-Jogger utility reminds you what you said to whom and tells you when you've ducked someone more than a set number of times. The program also generates fake itineraries, resumes, and credit references.

For your copy of Incognito, send $395 to ApresHeures Computing, 70 Main St., Paulsboro, NH 03458, (800) 123-4567. Call after 6 p.m. Please allow 10, maybe 12 weeks for delivery.

Texas Instruments announces Dr. L.S. Montejo Professional



Dr. L.S. Montejo,
Cardiac Anesthesiologist,
Boston, Massachusetts.

the Computing System.



No two individuals work alike. TI had unique answers to help Dr. L. S. Montejo keep his patients and his business healthy.

"I used to walk out of the operating room with a clipboard and a chart," says Dr. L. S. Montejo. "Now I walk out with a floppy disk."

Dr. Montejo is a prominent anesthesiologist who is pioneering the use of personal computers in heart surgery. His unique idea for making quicker, more informed decisions led to a unique solution from TI: a portable PC he could talk to. Configured to his exact needs from the wide range of TI options.

"Using TI's Speech Command," he says, "I can respond to drug reactions faster, with the PC making calculations as I speak to it. And my hands are free to do other things.

"The information just flies by.

But the computer organizes it, and by calling up color charts, I can make better decisions at a glance. It lets me provide better medical care."

In his office, Dr. Montejo uses a desktop TI Professional Computer to keep the business side of his practice operating smoothly. "Having to wait on a computer is a waste of valuable time," he says. "TI runs software fast. And the TI screen has a lot better resolution than other monitors."

His TI 855 printer also speeds up the paperwork. "We can use it to go from draft to letter quality immediately, and change typefaces very quickly by using the control panel instead of software commands."

TI had what the doctor ordered to put together a complete PC system for his specific needs. Including a solution for a budding computer genius in his family. "My daughter," he says, "loves her Speak & Spell."

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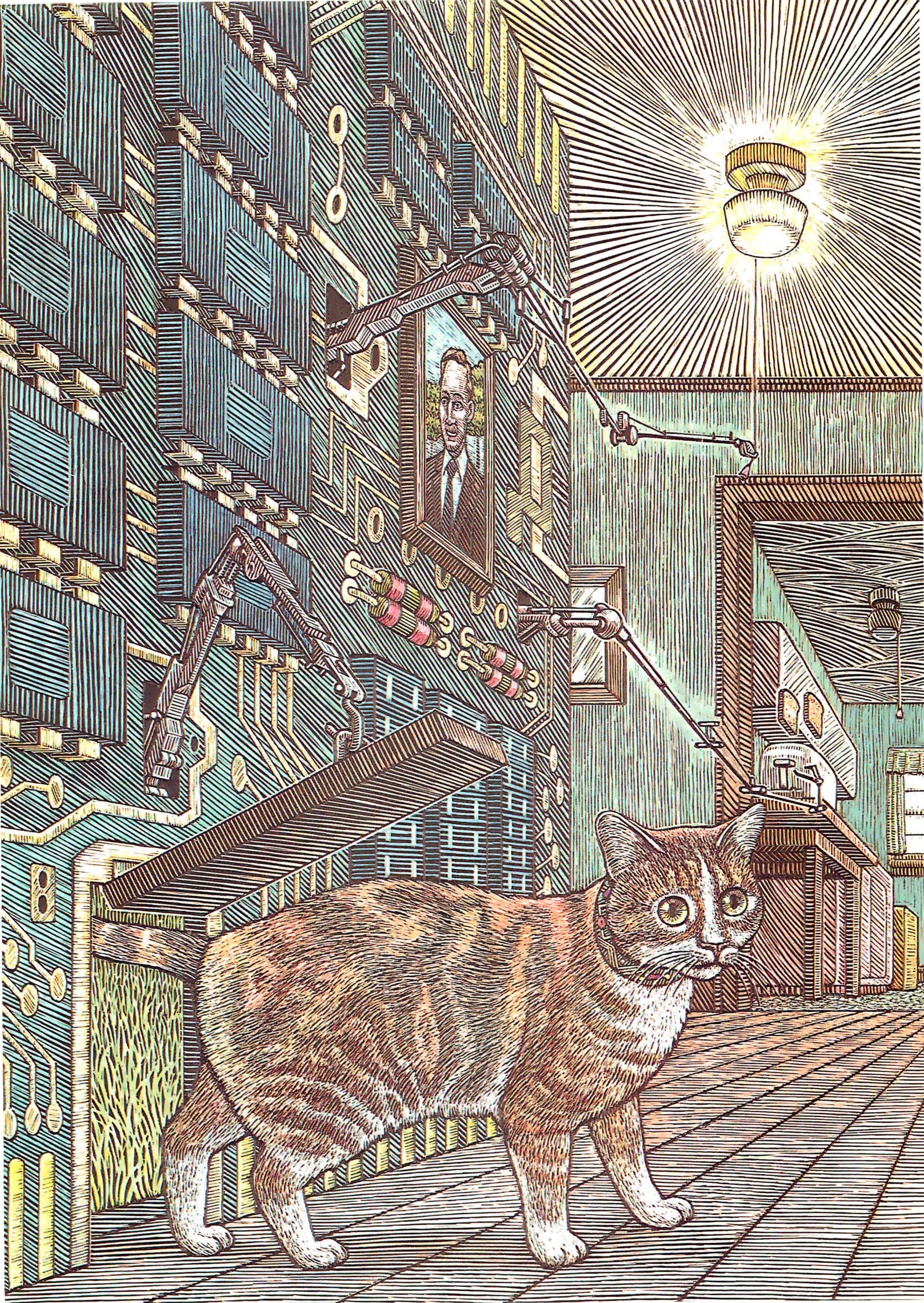


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2775-06



Features

IN JANUARY WE PRESENTED a real feast in the Features department; because we had no theme section, we were able to publish 11 articles on a wide variety of topics. This month, the significance of our theme on artificial intelligence and the depth of coverage it required limited the space we had available for features. Next month we'll return with our usual number.

As we hinted in the March Features introduction, this month Steve Ciarcia begins a three-part project that he's wanted to build for some time. The Circuit Cellar Home Run Control System takes up where Steve's first project of this type left off some years ago (see "Build a Touch Tone Decoder for Remote Control," December 1981, page 42). Imagine full programmable control over just about any outlet in your home. Lights can turn on and off automatically as you enter and leave a room. You can design a complex surveillance and security system that includes automatic emergency dialing. And you can phone home, check system status, and make modifications to the control system to suit your schedule. All in all, Steve was pretty happy with his original 1981 design, but with recent technological advances and his eye for improvement, he developed the Home Run Control System to be a lot friendlier and deliver a lot more.

In August 1984 the BYTE theme was Modula-2. Heralded by many as the language of the future, it also has detractors, some of whom point out that Modula-2 is only an upgrade of its Pascal ancestor with problems of its own. Colleen Roe Wilson's "Coprocessing in Modula-2" describes Modula-2's facility for the development of concurrent programs, one of its significant differences with Pascal.

If you have a Zenith Z-100 and are interested in exploiting its graphics capabilities, you might want to build "A Million-Point Graphics Tablet" based on Koala Technologies' KoalaPad. James Hawley shows you how to add the appropriate components and interface it to the Z-100's S-100 bus. With his graphics tablet, you can use a stylus instead of a light pen for pinpoint control over your drawings.

—Gene Smarte, Managing Editor







BUILD THE HOME RUN CONTROL SYSTEM

PART 1: INTRODUCTION

BY STEVE CIARCIA

Energy management, convenience, and security in one package



Six years ago I presented an article on building a computer-controlled security system using an SDK-85 experimenters board. To this day, I still get letters asking for software and material sources. Since home/industrial energy and security management have been and still are a major interest (and little has been published since then), that article remains a popular reference for students and experimenters.

As I look back on it now, I realize that my first home-control computer was engineered properly but was about as user-friendly as ENIAC. It's time to readdress the subject, bring the design up to date, and make this home-control system a real friend.

I conceive of this project as a simple computer control system equally applicable in the home or factory. The choice of input sensors and output controls designates its primary application.

Whether for industrial or home use, control systems function similarly. Specific input data is analyzed and compared to a predetermined set of action parameters. If a favorable comparison exists, the designated task is performed. For example, if a light is to be turned on at 2:00 p.m., the control system sees a negative request-affirmation comparison until that time. At that instant, the output of the control system turns on the light and then continues with the next request. In a control system configured as an alarm, the inputs would be from contact closures, and the outputs would be to bells, automatic dialers, and other such items.

Whatever the application, control systems are designed to be either open loop or closed loop in function. An open-loop controller simply outputs its decision and forgets about it. Industrial control systems, on the other hand, require more assurance that the action has been performed. They close the loop by analyzing feedback signals from the operation being controlled. If

(continued)

Steve Ciarcia (pronounced "see-ARE-see-ah") is an electronics engineer and computer consultant with experience in process control, digital design, nuclear instrumentation, and product development. He is the author of several books about electronics. You can write to him at POB 582, Glastonbury, CT 06033.

PHOTOGRAPHED BY PAUL AVIS, STYLED BY JANE SUTTON

a heating element is turned on, a current sensor in series with the element's power source or a temperature sensor next to the element indicates positively that the action has been performed.

It is this open-loop versus closed-loop configuration that, for most applications, defines whether a controller is consumer or industrial quality. I beg to differ with the trend, however, and feel that it is about time a system successfully bridged the gap. The Circuit Cellar Home Run Control System (HCS) is the result.

My intention is not to directly address the industrial market with my HCS. Rather, I will apply some of my industrial process-control experience to produce a design that offers flexibility and reliability as a home-control and energy-management system. If you are in the process-control business, you will soon realize that its sophistication and cost-effectiveness make it ideal for dedicated industrial-control applications where you might ordinarily use an expensive programmable controller.

HOME RUN CONTROL SYSTEM

Practically all commercial home-control systems use BSR X-10 remote-control power modules. They are sold under a variety of trademarks: Plug-N-Power, Sears Home Control, BSR X-10, and GE HomeMinder. These remotely controlled power switches turn the power on or off to lights and appliances that are plugged into them. A separate controller activates the individual switches by transmitting a coded command sequence through the power lines. Command controllers are available that perform timed or telephone-designated activations.

The Plug-N-Power or Sears Home Control system is quite adequate for most open-loop applications. An attic fan that needs to run two hours a day to keep the attic cool could use a timer-activated BSR module. Simply set the command unit to turn the fan on from 1:00 to 3:00 every afternoon, for example. Of course, on really hot days the attic fan will need to run longer, and on rainy days you'll be wasting power. If you compensate (close the loop) by changing the run time each day, it is hardly a home-control system. Instead, it is merely a more convenient manual power switch.

The solution is to use a true closed-loop control. By adding a 120- to 135-degree thermostatic switch in the attic, the control system can know when the attic is hot and has to be exhausted. A 90-degree thermostatic

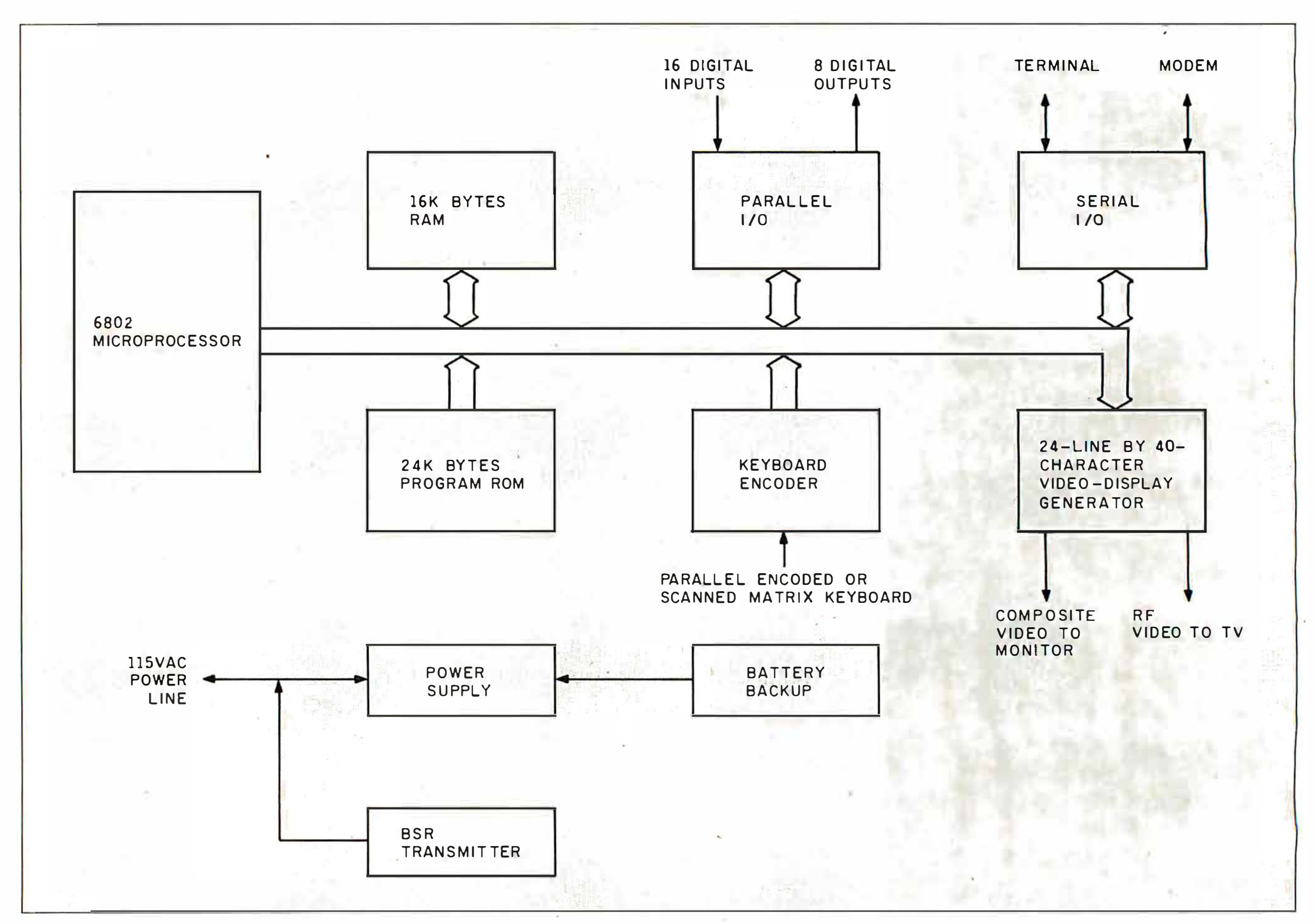


Figure 1: A *block diagram of the Circuit Cellar Home Run Control System.*

switch is also wired in. When the attic temperature reaches 135 degrees, the fan turns on. It turns off when it gets to 90 degrees. The BSR control modules could still provide the on/off power to the fan, but the control decision is more adequately defined by directly monitoring the temperature with heat sensors than by simple timed activation. This way, the fan will stay on as long and often as needed. On cloudy or rainy days, the fan might not come on at all. (I am aware that special thermostatically controlled attic-fan switches can accomplish this specific task without a computer. I am not trying to find a specific solution but rather to demonstrate the two control approaches as they apply to general-purpose control systems.)

The immediate answer to open-loop BSR control is to add more intelligence in the form of a computer. Presently, many control systems on the market use personal computers. Using the parallel I/O (input/output) and display capabilities of the personal computer with a specialized BSR transmitter card installed, many companies have successfully designed just the kind of home-control system I'd want. However, such a seemingly economical approach uses the entire function of the computer. You can have a $2500 Apple II home controller or suffer when the entire system grinds to a halt because you've loaded a word-processing program. Besides, it can cost $10 a month just to run an IBM PC 24 hours a day—and don't forget the cost of the uninterruptible power supply.

Ultimately, successful computer-based energy-management and home-control systems must have completely dedicated functions. Trying to time-share tasks among games, word processing, and environmental control is simply more complicated than it's worth. The age of specialized computers is at hand.

The Circuit Cellar HCS is designed specifically for that task. It is a single-board microprocessor-based controller that uses a combination of both open- and closed-loop control design. It takes advantage of the cost-effective BSR control modules and fully duplicates any of the manual, automatic, or timed functions presently supported in the BSR product line.

The Circuit Cellar HCS closes the control loop with 16 hard-wired digital input and 8 TTL (transistor-transistor logic)-compatible hard-wired output lines. Relays, contact closures, motion detectors, and thermostatic switches can be connected to these I/O lines for direct "sense and respond" activities. It can also accommodate 48 BSR modules. Figure 1 is a block diagram of the HCS.

The 6802-based HCS is a stand-alone control unit (see photo 1) complete with battery backup. Photo 2 shows the prototype circuit board that mounts inside the control unit. The HCS communicates with the user through either a serial terminal or video monitor and keyboard. In the terminal mode, RS-232C communication is at 75 to 4800 bits per second (bps).

The HCS optionally supports an integral video-display generator to provide a 24-line by 40-character display either directly to a composite video monitor or to a television set. A keyboard encoder allows connection of either an Apple II-compatible parallel-encoded keyboard or an unencoded scanned-matrix keyboard. Finally, the HCS can communicate with other systems. An additional con-

(continued)

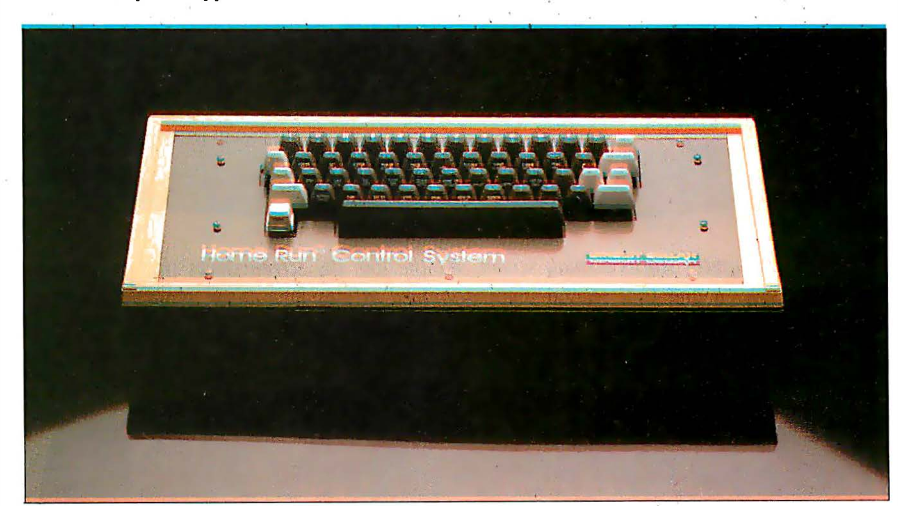


Photo 1: *Home Run Control System stand-alone control unit.*

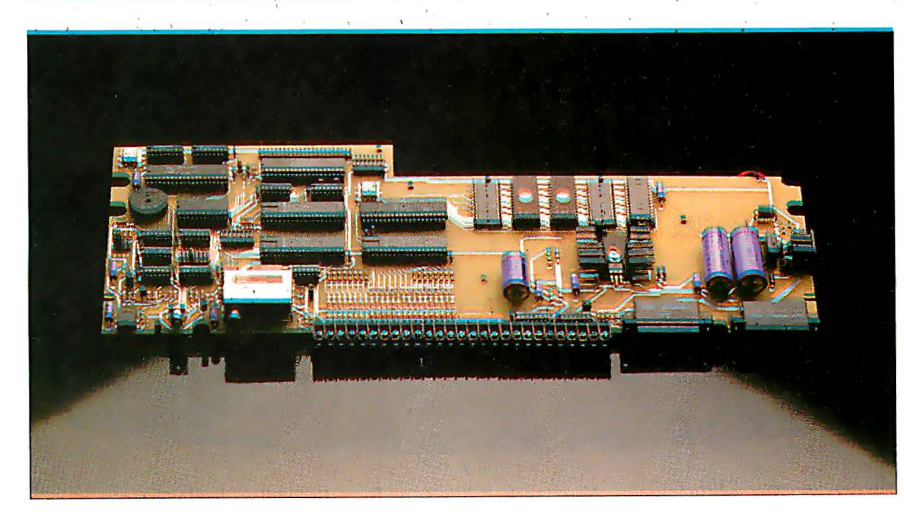


Photo 2: HCS *prototype circuit board.*

nector has been provided to which an auto-answer modem can be attached (such as the Hayes 300 or 1200). When the modem answers and the CTS line is activated, the HCS switches its display to the modem data rate and allows the remote calling terminal to access and control the HCS. Unlike auto-answer BSR units that allow command input only, this option lets you view the complete status of all I/O and make program changes as well.

```
FRI APR  5  8:04 PM

ALARM SYSTEM ON
MOTION DETECTED IN STOCK ROOM
LIGHTS TURNED ON
SILENT ALARM
SECURITY NOTIFIED

                        1111111
                     1234567890123456
1 BSR ON/OFF A 1111·······0····
2 BSR DIMMER A ················
3 BSR CYCLER A ················
4 BSR ON/OFF B ················
5 BSR ON/OFF C ················
6 DIRECT OUT   ········
7 MESSAGES     1···············
8 SUPERKEY     0···············
```

Photo 3: *A typical status-display screen. At the top, the screen shows that an alarm has been triggered and that several preprogrammed actions have taken place. The bottom half of the screen indicates the status of all the output drivers.*

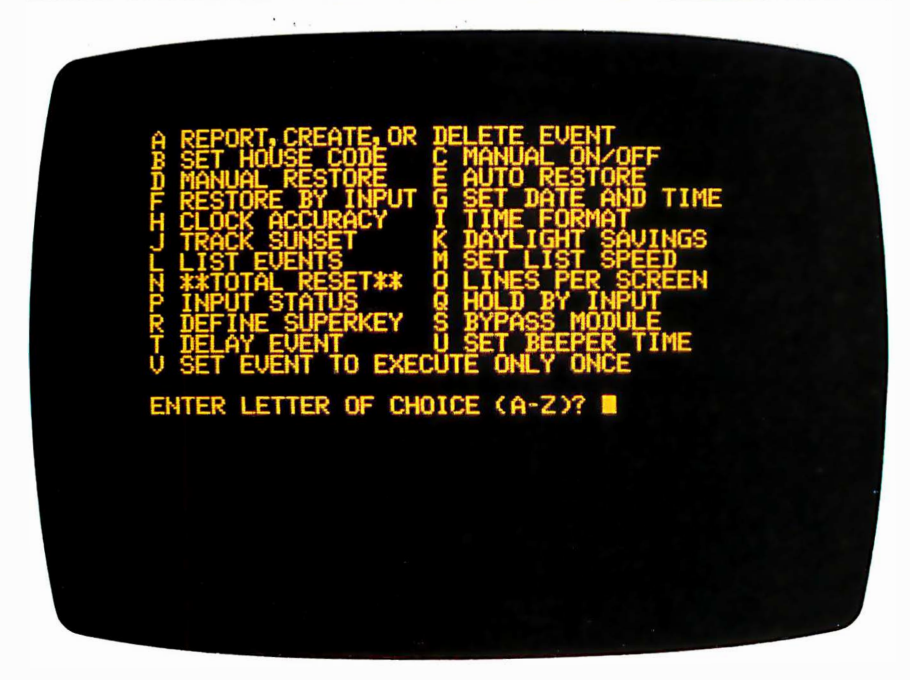


Photo 4: *The editing menu. You reach this screen from the status-display screen by pressing the space bar. All the functions will be explained in subsequent articles.*

The HCS can schedule to turn outputs on or off based on combinations of the following conditions:

a. time of the week (e.g., Tuesday at 4:32)
b. time of the month (e.g., 22nd at 11:20)
c. input line going high
d. input line going low
e. turn off after time delay (e.g., remain on for 15 minutes)
f. one-time action triggered by specific input or time

When you want to create an event, various combinations of inputs and time can be specified. They are

1. ON at specified time
   OFF at specified time
2. ON at specified time
   OFF when specified input occurs
3. ON when specified input occurs
   OFF at specified time
4. ON when specified input occurs
   OFF when specified input occurs
   or
   ON while specified input occurs
5. ON when specified input occurs
   OFF after period of time

Lights can be dimmed to one of 16 levels. This allows mood control, night light, or power conservation operation. Text messages of variable size can be scheduled as announcements or reminders. And the HCS uses less than 5 watts (W).

The processor and clock continue to operate during a power failure; scheduled events are noted in memory. When AC power is restored, the HCS restores all modules to the state they would be in if power weren't interrupted.

The on-time of desired modules, usually lights, tracks the sunset. This alleviates having to adjust the schedule many times per year as the sunset changes. Included is a com-

mand to compensate sunset times for daylight saving.

The HCS can optionally restore the status of all modules every four minutes. This is useful in commercial applications where a module may be turned off by a transient or non-HCS-generated command. Restore can also be triggered by an input line.

Modules can be bypassed for a selected interval (up to 44 days). This can be used for vacations or holidays. It also allows an input occurrence to lock out specified modules. Clock accuracy can be adjusted by software to within one second per day. And, finally, the entire event schedule can be listed to the serial port. The speed of the listing can be controlled to allow for printing of the schedule.

The HCS is designed to communicate in English and not in a programming language. All control sequences are prompted through menus, and any input errors simply cause the system to revert back to the status display or the option menu.

The HCS is designed around the concept of an "event." An event has four elements: the type of event, the device on which the event will operate, the trigger that starts the event, and the trigger that ends the event. The type of event is defined in terms of its "driver." These include Message Driver, BSR On/Off Driver, BSR Cycle Driver, BSR Dimmer Driver, Direct Output Driver, and Superkeys.

The Message Driver displays a message on the terminal. The BSR On/Off Driver turns a BSR control module on or off. The BSR Cycle Driver causes a specified BSR module to cycle on and off periodically at a rate determined by the user. The BSR Dimmer Driver changes the brightness of a BSR lamp module. The Direct Output Driver sets the output level on the eight direct output lines. Superkeys are 16 function keys that, when selected by a three-button sequence, trigger a predefined event sequence (such as turning on specific BSR modules, displaying particular messages, or setting specific outputs). The quantity of events is limited only by

(continued)

Figure 2: *Programming the HCS to turn the attic fan on.*

```
FRI APR  5 10:09 PM


                        1111111
               1234567890123456
1 BSR ON/OFF A  ----------------
2 BSR DIMMER A  ----------------
3 BSR CYCLER A  ----------------
4 BSR ON/OFF B  ----------------   (When using a terminal, the raised-
5 BSR ON/OFF C  ----------------   dot graphics character is printed
6 DIRECT OUT    --------           as a " – " instead)
7 MESSAGES      ----------------
8 SUPERKEY      ----------------

(a space entered on the keyboard brings up the editing menu)

A REPORT,CREATE,OR DELETE EVENT
B SET HOUSE CODE      C MANUAL ON/OFF
D MANUAL RESTORE      E AUTO RESTORE
F RESTORE BY INPUT    G SET DATE AND TIME
H CLOCK ACCURACY      I TIME FORMAT
J TRACK SUNSET        K DAYLIGHT SAVINGS
L LIST EVENTS         M SET LIST SPEED
N **TOTAL RESET**     O LINES PER SCREEN
P INPUT STATUS        Q HOLD BY INPUT
R DEFINE SUPERKEY     S BYPASS MODULE
T DELAY EVENT
U SET EVENT TO EXECUTE ONLY ONCE

ENTER LETTER OF CHOICE (A-Z)? A

* MEANS EVENTS ARE SCHEDULED

                        1111111
               1234567890123456
1 BSR ON/OFF A  ----------------
2 BSR DIMMER A  ----------------
3 BSR CYCLER A  ----------------
4 BSR ON/OFF B  ----------------   (No events are
5 BSR ON/OFF C  ----------------   presently scheduled)
6 DIRECT OUT    --------
7 MESSAGES      ----------------
8 SUPERKEY      ----------------

ENTER DRIVER NUMBER (1-8)? 1

ENTER MODULE NUMBER (1-16)? 1

THIS DRIVER/MODULE NOT IN USE

CREATE OR DELETE EVENT (C/D)? C
374 CHARACTERS AVAILABLE

ENTER NAME OF MODULE

ONE RETURN STARTS NEW LINE
AND TWO RETURNS ENDS
?ATTIC FAN

1  ON AT SPECIFIED TIME
   OFF AT SPECIFIED TIME

2  ON AT SPECIFIED TIME
   OFF WHEN SPECIFIED INPUT OCCURS

3  ON WHEN SPECIFIED INPUT OCCURS
   OFF AT SPECIFIED TIME
```

(continued)

By selecting different options you can program the HCS to perform specific tasks.

the available RAM (random-access read/write memory). (Even though the Superkeys, messages, and outputs are not BSR devices, I refer to each of their separate events as modules to be consistent with BSR terminology.)

The HCS has two display modes: status and editing. The status display, shown in photo 3, is the normal operating display of the HCS. At the top is the current date and time. Below that is an area where any messages will be displayed when activated. At the bottom is the actual real-time status of all output drivers presented as an 8-driver by 16-module display matrix. If no action has been defined for a particular module, a raised dot is displayed. If an event has been programmed for a particular module, a "0" indicates that it is currently off; a "1" indicates that it is currently on. The display updates in real time as the modules change state or the clock updates.

Pressing the space bar displays the editing menu (see photo 4). By selecting the different options presented in the menu, you can program the HCS to perform the specific tasks you wish. Controlling the attic fan with two thermostatic switches attached to input lines 1 and 2 respectively is a relatively simple procedure. Figure 2 shows what appears on the display screen as we program that event.

The fan will start when input line 1 goes low (it can be redefined for reverse polarity) and will go off when line 2 goes low. Perhaps you want to know when the fan is on (besides remembering that driver 1/module 1 is the fan and looking at the status display), so we'll add a message defined

```
4  ON WHEN SPECIFIED INPUT OCCURS        (Entering the same input # for
   OFF WHEN SPECIFIED INPUT OCCURS        both the ON and OFF trigger
                                          in Item 4 results in "ON WHILE
                                          SPECIFIED INPUT OCCURS")
5  ON WHEN SPECIFIED INPUT OCCURS
   OFF AFTER PERIOD OF TIME

ENTER NUMBER OF ON/OFF
COMBINATION (1-5)? 4

ENTER INPUT # FOR ON (1-16)? 1

ENTER INPUT # FOR OFF (1-16)? 2

ATTIC FAN
  1     INPUT#  1       INPUT#  2

ENTER INPUT # FOR ON (1-16)?    (More inputs can be added to specify
                                 the same BSR module function; to exit,
                                 simply enter a return and the status
                                 display will resume)

FRI APR 5   10:11 PM

                          1111111
                 1234567890123456
1 BSR ON/OFF A   0---------------
2 BSR DIMMER A   ----------------     (Status display now
3 BSR CYCLER A   ----------------      shows driver 1 module
4 BSR ON/OFF B   ----------------      1 programmed but
5 BSR ON/OFF C   ----------------      inactive)
6 DIRECT OUT     --------
7 MESSAGES       ----------------
8 SUPERKEY       ----------------
```

Figure 3: *Programming the HCS to print a message when the fan is on.*

```
* MEANS EVENTS ARE SCHEDULED

                          1111111
                 1234567890123456
1 BSR ON/OFF A   *---------------
2 BSR DIMMER A   ----------------
3 BSR CYCLER A   ----------------
4 BSR ON/OFF B   ----------------
5 BSR ON/OFF C   ----------------
6 DIRECT OUT     --------
7 MESSAGES       ----------------
8 SUPERKEY       ----------------

ENTER DRIVER NUMBER (1-8)? 7

ENTER MODULE NUMBER (1-16)? 1

THIS DRIVER/MODULE NOT IN USE

CREATE OR DELETE EVENT (C/D)? C

1  ON AT SPECIFIED TIME
   OFF AT SPECIFIED TIME
```

(continued)

```
2  ON AT SPECIFIED TIME
   OFF WHEN SPECIFIED INPUT OCCURS
3  ON WHEN SPECIFIED INPUT OCCURS
   OFF AT SPECIFIED TIME
4  ON WHEN SPECIFIED INPUT OCCURS
   OFF WHEN SPECIFIED INPUT OCCURS
5  ON WHEN SPECIFIED INPUT OCCURS
   OFF AFTER PERIOD OF TIME
ENTER NUMBER OF ON/OFF
COMBINATION (1-5)? 4
ENTER INPUT # FOR ON (1-16)? 1
ENTER INPUT # FOR OFF (1-16)? 2
502 CHARACTERS AVAILABLE
ENTER MESSAGE
ONE RETURN STARTS NEW LINE
AND TWO RETURNS ENDS
?
  THE ATTIC FAN IS ON
  1    INPUT#  1        INPUT#  2
THE ATTIC FAN IS ON
ENTER INPUT # FOR ON (1-16)? (just return to exit)
FRI APR 5 10:12 PM

                           1111111
                  1234567890123456
1 BSR ON/OFF A    0---------------
2 BSR DIMMER A    ----------------
3 BSR CYCLER A    ----------------
4 BSR ON/OFF B    ----------------      (The two zeros indicate that the
5 BSR ON/OFF C    ----------------      modules are defined but OFF)
6 DIRECT OUT      ----------
7 MESSAGES        0---------------
8 SUPERKEY        ----------------

(If we close the contact on input line #1, the following happens:)
FRI APR 5 10:15 PM
THE ATTIC FAN IS ON

                                        (This listing is spaced to show
                                        the full 24-line display)

                           1111111
                  1234567890123456
1 BSR ON/OFF A    1---------------
2 BSR DIMMER A    ----------------
3 BSR CYCLER A    ----------------
4 BSR ON/OFF B    ----------------
5 BSR ON/OFF C    ----------------
6 DIRECT OUT      ----------
7 MESSAGES        1---------------
8 SUPERKEY        ----------------
```

As I use the HCS and find certain functions or displays I want revised, some of them may change.

to trigger from the same events to say "the fan is on."

We can create an event at this point by simply typing "A." The display that results is shown in figure 3.

There is a lot more to this control system than the simple example in figure 3 illustrates. You probably noticed functions such as Restore, Sunset Adjust, Delay, Bypass, and Hold in the editing menu. Eventually, I'll get to explaining them all and illustrating their use.

One Parting Comment

The HCS is an evolving design. This is a three-month project that is being written over the course of three months. While the hardware design is fixed and printed-circuit boards are checked out, software is constantly evolving and more features are being added. Photos of the menus, status displays, and other items are taken at a specific time in the evolution of the software. As I use the HCS and find certain functions or displays that I want revised, some of them may change.

User-friendliness is one area. In reviewing some of the higher-volume but lower-functioning control systems such as GE's HomeMinder, the emphasis is on graphics and simple user interfacing. If you want to control a lamp on the HomeMinder, you look for the picture of a lamp and manipulate it on the screen.

I configured HCS to be a high-level controller with much less emphasis on pretty graphics. However, many of the professional software people who have seen HCS believe it would have

(continued)

a much wider audience if it had some "paint-by-numbers" appearance. Consequently, they plan to support it independently. A HomeMinder-like graphics package is presently being written for the IBM PC by third parties. It will connect to the HCS through the terminal I/O port. Hopefully, I'll have a picture of it in operation by the third month.

While I'll live without Alice-in-Wonderland control software, I was bitten by the large-system interface bug and decided to take advantage of big-system functions. The HCS optionally includes an upload/download capability to the IBM PC (eventually for other computers). The complete command and control sequence resident in the HCS can be uploaded serially to the PC for storage on disk. A download provision reprograms the HCS with that control sequence.

This storage capability allows the user to run the HCS with various control sequences loaded from disk. A "training" session debugs the sequence and then it is stored on disk for later retrieval. Industrial users who change program sequences frequently are the prime beneficiaries, but new tools often produce new applications. This function is also accessible via the HCS's modem port, and Home Run can be completely reprogrammed by telephone. (Perhaps you have a vacation home. Simply call ahead and let the HCS make it a warm and cozy arrival.)

EXPERIMENTERS AND OEM USERS

As always, I try to support the computer experimenter by providing sources for many of the components. The Circuit Cellar Home Run Control System is a single-board design suitable for OEM applications as well. It is available in various configurations that are all ultimately upgradable to the same potential.

If you plan on building the unit from scratch, good luck and take heart. Send me a picture of your board, and I'll send you a free hexadecimal dump (16K bytes) of the control software, provided it is for noncommercial private use. I'll supply the code on two 2764 EPROMs (erasable programmable read-only memories) and a manual for $32 (postpaid in the U.S.). Add $7 for overseas.

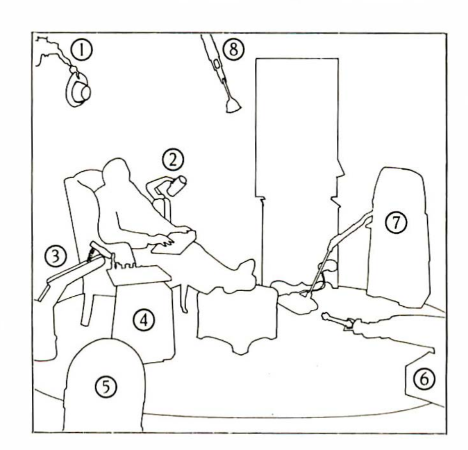
CIRCUIT CELLAR FEEDBACK

This month's feedback begins on page 408.

NEXT MONTH

This is a three-part article. Next month, I'll describe the hardware in detail, hopefully to the extent that you can build your own HCS. The third part will emphasize the software and demonstrate a typical control application. ■

ROBOTIC PROPS (counterclockwise from upper left): 1. CYBOT INC., 12510 128th Ave. NE, Kirkland, WA 98034. 2. MICROBOT INC., 453 Ravendale Dr., Mountain View, CA 94043. 3. HAIKATO ROBOTICS LTD., 1580 Lincoln St., Suite 950, Denver, CO 80203. 4. HEATH CO., Hilltop Rd., St. Joseph, MI 49085. 5. RB ROBOT CORP., 14618 West 6th Ave., Golden, CO 80401. 6. RSI INC. (Robotics Systems International Ltd.), 9865 West Saanich Rd., RR2, Sydney, British Columbia V8L 3S1, Canada. 7. HUBOTICS INC., 6352-D Corte Del Abeto, Carlsbad, CA 92008. 8. RHINO ROBOTS INC., POB 4010, Champaign, IL 61820.



SET PROPS: STURBRIDGE YANKEE WORKSHOP INC., Kettleford Korner, Bedford, NH 03102. BRITCHES OF CONCORD INC., 1 Eagle Square, Concord, NH 03301. GENIE VACUUM CLEANER CO., 93 South Maple St., Manchester, NH 03103.

Special thanks to Bill Summers and Leo Taylor for their software expertise.

The following items are available from

The Micromint Inc.
25 Terrace Dr.
Vernon, CT 06066
(800) 635-3355 for orders
(203) 871-6170 for information

1. Home Run HCS—Complete assembled system with enclosure and Apple-compatible keyboard HCS01, $589
2. Home Run HCS—Populated PC board. Assembled and tested PC board. No enclosure or keyboard HCS02, $429
3. Home Run HCS—Video-based kit. Includes PC board and all components except enclosure, keyboard, and serial-interface components (IC16, IC17, IC20, and two DB-25 connectors) HCSV05, $329
4. Home Run HCS—Terminal-based kit. Includes PC board and all components except video-display processor (IC22, IC25, and IC26). No keyboard, enclosure, or RF modulator HCST06, $289
5. 8K-byte static-RAM upgrade. Increases RAM to 16K bytes. HCS20, $35
6. Apple II-compatible ASCII-encoded keyboard HCS21, $79
7. Wall transformer/transmitter module (available separately) HCS22, $40

All kits and assembled units include operators manual, power supply with wall transformer/transmitter module, and 8K bytes of RAM. All units are supplied without keyboard encoder chip (not necessary when using encoded keyboard, IC18—optionally available). All item numbers that list enclosures also include backup battery holder (6 "C" cells), less batteries. Serial-port and video-display-processor upgrades for items 3 and 4 and various other components are also available.

Please include $8 for shipping and handling in the continental United States, $12 elsewhere. New York residents please include 8 percent sales tax. Connecticut residents please include 7.5 percent sales tax.

Editor's Note: Steve often refers to previous Circuit Cellar articles. Most of these past articles are available in book form from BYTE Books, McGraw-Hill Book Company, POB 400, Hightstown, NJ 08250.

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BY COLLEEN ROE WILSON

COPROCESSING IN MODULA-2

The key to writing concurrent programs is coordination

One of the main differences between Modula-2 and its ancestor, Pascal, is that Modula-2 contains specific programming constructs to permit the development of real-time concurrent programs. Thus, you can use Modula-2 to write operating systems and other low-level software instead of using assembly language, the language in which operating systems are traditionally written.

CONCURRENCY

Truly concurrent programs execute at exactly the same instant in time—implying the use of separate computers. True concurrency occurs in distributed processors such as those found in control systems and other real-time applications.

When several people use a single computer, however, concurrency refers to interleaved execution. Such programming is at the heart of large time-sharing systems, where many users on a single computer can run programs at the same time. Each person perceives only the execution of his own program, while the operating system performs a juggling act partitioning the processing power among the users. Interleaved execution, then, is the seeming concurrency of many processes running on one processor.

Whether we call it true concurrency or not, the problems inherent in writing this type of program are much the same. The main problem is timing. Concurrent programs must deal with nondeterministic events that occur at arbitrary times.

Suppose you have two computers connected by some kind of communications link. You want to write a program so that two people sitting in two different places can exchange messages by typing at their respective keyboards. Each computer must perform this basic sequence of actions:

- When a key is struck on computer A's keyboard, A must retrieve that key's value and send it to computer B.
- When a character arrives at computer A from computer B, A must

(continued)



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ILLUSTRATED BY LAURA CORNELL

display it in the next free position on its screen.

Does this sound simple enough? Let's take a look at what can happen. If you stop and think about how you type at a keyboard, it becomes obvious that you can't expect a fixed pattern to the keyboard input and the arrival of data on the link. Two users might carry on a question-and-answer conversation so that only one person types at a time. On the other hand, two users might argue and type simultaneously. Either way, the program needs to know what to do. This nondeterministic activity differentiates real-time programs from typical application programs with fixed read/write interfaces. You can't predict how many reads (input from the keyboard) or writes (output to the link) the program will have to deal with or how they will be ordered.

The nondeterministic nature of concurrent programming leads to some interesting problems—deadlock or "deadly embrace" being the best known. Suppose a time-sharing system is trying to run two programs. Both programs need exclusive use of the computer's tape drive and a particular printer to run. The operating system starts program A, which acquires the tape drive. Having used its time slot, program A is suspended while the operating system starts program B. Program B immediately acquires the printer and is suspended. When A starts up again, it attempts to acquire the printer and fails, so its execution is suspended until the printer is freed. When B starts up again, it attempts to acquire the tape drive and is likewise suspended until the drive is freed. The two programs are deadlocked. Neither can proceed until the other frees the resource needed.

The key to writing successful concurrent programs is coordination. You must make sure that programs that are either cooperatively or independently executing interact with each other in a constructive—or at least nondestructive—manner. Modula-2 has programming constructs dealing with concurrency to aid in this coordination.

COPROCESSES

Coprocessing is a technique that helps you implement coordination when writing concurrent programs. For example, suppose you write two programs to execute as coprocesses—Text and Disk. Text prompts you to enter text from the keyboard for disk storage (it could be an editor). Disk is a low-level driver program that interacts with the disk to read and write records. The two coprocesses interact as follows:

- Text prompts you for keyboard input and puts the characters into a buffer as it receives them until it finds the record terminator.
- Text signals Disk that a record is ready in the buffer and suspends execution.
- Disk retrieves the record and writes it to the disk.
- Disk signals Text that the record has been written and suspends its execution.
- Text resumes execution at the point of suspension and prompts you for more input.

Thus, Text and Disk coprocess the information by passing it back and forth. This producer(Text)/consumer (Disk) relationship is the classic relationship between coprocesses.

You can expand this concept to include more than two processes. Suppose you want various processes to exchange messages during execution. They need to be able to send messages to other processes and to receive the same—a sort of electronic interprocess mail scheme. One special process is the postmaster. It receives and stores messages and then distributes them as requested by the designated receiving process. The postmaster acts as a coprocess with the other processes that can request to send or receive messages. When sending, the requesting process suspends execution while the postmaster picks up the message in its buffer and resumes when the postmaster is done. When receiving, the requesting process suspends while the postmaster fills its buffer with the message and then continues.

WRITING COPROCESSES IN MODULA-2

Two essential mechanisms are needed to implement the mechanics of coprocessing: first, a means of identifying and executing a program that establishes it as a process; second, a method so that two coprocesses can signal each other to coordinate their activities. Modula-2 has facilities for these mechanisms imbedded within it. Modula-2 programmers do not have to get around the language to write coprocesses; the language directly supports this kind of programming.

The most fundamental support of coprocesses provided in Modula-2 is the data type PROCESS, which can be imported from the module SYSTEM. We expect languages to support our abstract number systems with such data types as REAL and INTEGER, but this is something new: a process materialized in a data type. The need for it is obvious: a language that manipulates processes must be able to refer to them in a concrete manner.

Coprocesses use these PROCESS variables to communicate with each other. Therefore, when you create a coprocess, you must bind it to one of these variables. Likewise, when these programs pass control to one another, they must use PROCESS variables to indicate their targets. Modula-2 contains two procedures that provide this control: NEWPROCESS and TRANSFER, both of which are imported from the module SYSTEM.

NEWPROCESS, which creates a coprocess within the system and binds it to a PROCESS variable, is called by

```
NEWPROCESS(p: PROC,a:
  ADDRESS,s: CARDINAL,VAR c:
  PROCESS);
```

In this statement, *p* is the name of a procedure that contains the code you want to constitute the process, *a* is the

(continued)



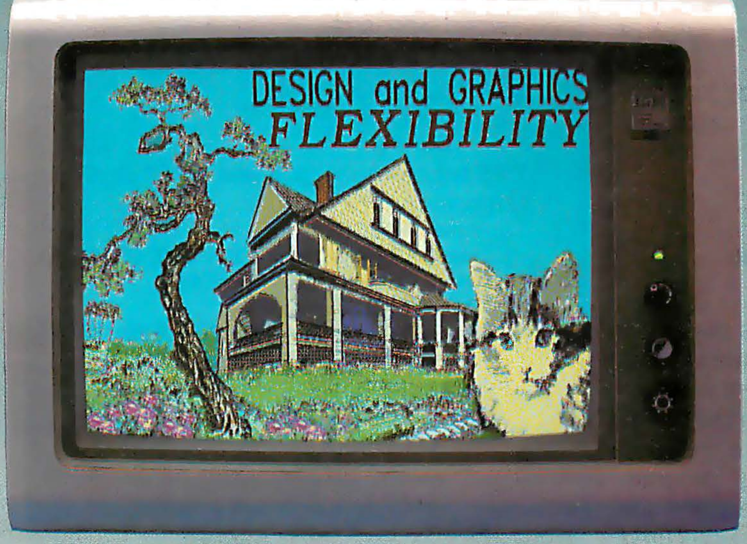
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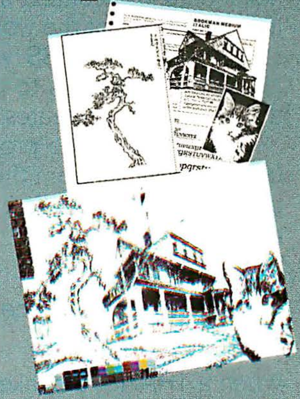


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address of a storage area that serves as the working space for the process (local data and context are stored in it), *s* is the size of the working space, and *c* is a PROCESS variable that NEWPROCESS sets to the value of the coprocess it creates.

TRANSFER is the procedure that transfers control from the calling coprocess to the one called. It is invoked by

```
TRANSFER(VAR
  thisprocess,coprocess:
  PROCESS);
```

When a TRANSFER takes place, the calling coprocess is suspended and its context (data values, current program counter, etc.) saved. When the called coprocess executes the reverse TRANSFER, the calling program resumes execution at the point immediately following its just-executed TRANSFER statement. This is the significant difference between procedural calls and TRANSFERs. Each time you call a procedure, execution returns to the beginning of the program and local storage is reallocated. Coprocesses maintain context between TRANSFERs.

The actual implementation of the data type PROCESS and the procedures NEWPROCESS and TRANSFER varies with each machine and compiler. However, you need not be concerned with this. The data abstraction provided by Modula-2 lets you merely manipulate the PROCESS variables with these procedures. Your interface is constant across machines. Contrast this with assembly-language programming, where you need significant knowledge of the operating-system internals to manipulate the data structures representing processes.

CODING AN EXAMPLE

Now that we've established what facilities exist in Modula-2 to program coprocesses, let's look at an example. Starting at the top of the module definition of TermHandler (see listing 1), you import the needed concurrency structures from SYSTEM: the data types PROCESS, ADDRESS, and WORD, and the procedures NEW-

Listing 1: *An example of coprocesses coded in Modula-2.*

```
MODULE TermHandler;
  FROM SYSTEM IMPORT ADDRESS, PROCESS, NEWPROCESS, TRANSFER,
    WORD, ADR, SIZE;
  FROM SYSIO IMPORT GetChar, PutDisk;
  CONST bufsize = 80;
        nterm = 16;
        CR = 13C;
  TYPE buftype = ARRAY[0..bufsize - 1] OF CHAR;
  VAR buffer: buftype;
      nchar: INTEGER;
      wspT: ARRAY[0..nterm - 1],[1..200] OF WORD;
      wspD: ARRAY[1..200] OF WORD;
      D,C: PROCESS;
      T: ARRAY[0..nterm - 1] OF PROCESS;
      thisterm: INTEGER;
    PROCEDURE TextIn;
      VAR newchar: CHAR;
          status: BOOLEAN;
          localbuf: buftype;
          count: INTEGER;
      BEGIN
        count: = -1;
        LOOP
          GetChar(thisterm,newchar,status);
          IF status THEN
            CASE newchar OF
              CR: nchar: = count;
                  buffer: = localbuf;
                  TRANSFER(T[thisterm],D);
                  count: = -1
              ELSE
                INC(count);
                localbuf[nchar]: = newchar;
                IF count = bufsize - 1
                  THEN
                    nchar: = count;
                    buffer: = localbuf;
                    TRANSFER(T[thisterm],D);
                    count: = -1
                END
            END
          END;
          TRANSFER(T[thisterm],C)
        END;
      END TextIn;
  PROCEDURE TextToDisk;
    BEGIN
      LOOP
        PutDisk(buffer,nchar);
        TRANSFER(D,T[thisterm])
      END
    END TextToDisk;
  BEGIN
    NEWPROCESS(TextToDisk,ADR(wspD),SIZE(wspD),D);
    FOR thisterm: = 0 TO nterm - 1 DO
      NEWPROCESS(TextIn,ADR(wspT[thisterm]),
                 SIZE(wspT[thisterm]),T[thisterm])
```

(continued)

```
        END;
        thisterm: = 0;
        LOOP
           TRANSFER(C,T[thisterm]);
           thisterm: = thisterm + 1 MOD nterm
        END
    END TermHandler.
```

PROCESS, TRANSFER, ADR, and SIZE. ADDRESS and WORD are self-explanatory primitive data types, ADR is a function that returns the initial address of the variable passed to it, and SIZE is a function that returns that variable's storage allocation size. Assume the existence of a module named SYSIO, from which you import GetChar and PutDisk. In the CONST section you define the buffer size (bufsize) and the record terminator CR (carriage return). In the VAR section you define the shared buffer (buffer) and the shared character count (nchar). In addition, you define working spaces for the two coprocesses you will create (wspT and wspD).

Suppose you want to handle keyboard-to-disk transfers for a number of terminals—an order-entry system, for example. Listing I shows an array of processes (T) and working spaces (wspT). The procedure GetChar is passed a terminal-port number (thisterm) and returns a status (true means new character returned while false means the opposite) as well as the keyboard character (newchar). If a character has arrived since the last GetChar call, it is returned; otherwise the status reports the failure. The reason will become clear in a moment.

As the main body of code for TermHandler begins, process D is created, followed by the nterm terminal processes. Then the program enters a loop continually coprocessing with each of the individual terminal handlers. Each one manages its own character count (count) and buffer (localbuf). When a handler detects a CR or a full buffer, it moves its own buffer and count to the global buffer (buffer) and global count (nchar) and transfers to process D to dump the record. (Although it is more common for coprocesses to share pointers to variables than actual variables, these examples use them to make the code more readable.) You can see that if GetChar waited for a character to arrive—in other words, if it did not use the status—a single terminal could hold up all the others if it produced no input.

What does coprocessing achieve in this example? First, when a specific terminal handler issues a TRANSFER back to process C, its context is saved in its workspace. Therefore, the next time it is activated, the values of count and localbuf are appropriately set. This would not be true if you used procedural calls instead of coprocesses.

Second, because each handler maintains its own data structures, the overall program is kept fairly simple. You don't have to manage an array of buffers and counters. Each handler is concerned with only a single buffer and counter, and the code is recycled *nterm* times. You also gain flexibility. A more sophisticated version of TermHandler could associate processing priorities with some terminals and choose to ignore others. In fact, in a coprocessing situation TermHandler could create new terminal handlers on request (instead of using a fixed number) or only transfer to a specific handler on certain conditions.

CONCLUSION

Coprocesses cooperatively process information by interleaved execution on a single computer. You must be careful to ensure that processes interact constructively, and Modula-2 automatically contains the programming constructs to aid in this coordination. These coprocesses provide a means of passing control between programs without losing the desired execution sequence or the context. ■


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BY JAMES HAWLEY

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The need for a graphics tablet is quickly apparent if you try to do high-resolution drawings from a keyboard. Although you can create complex pictures with the control keys and cursor, you will soon want a true drawing machine because of the directional and speed limitations of keyboard drawing.

The Zenith Z-100 is truly a graphics computer with 640 by 225 pixels in three planes (eight colors). The machine devotes 64K bytes to each plane and has the ability to create 640 by 480 pixels in eight colors. The ZBASIC graphics commands offer a quick method of creating custom graphics programs.

To attain true graphic creativity you need to use a stylus for input. You can draw with a light pen but it is often awkward to use vertically and difficult to tell exactly where the pen is pointing on a pixel-by-pixel basis. A graphics tablet solves these problems.

There are many methods of interfacing analog input to a microcomputer's bus but it is simplified by bus-compatible analog-to-digital (A/D) converters. The National Semiconductor ADC1001 enables you to interface a 10-bit digital (1024-point) signal to the Zenith S-100 bus with only two support chips.

The graphics pad described here uses Koala Technologies' KoalaPad for the analog *x, y* input that feeds the two ADC1001s connected to the S-100 bus. To modify the KoalaPad, you open it by unscrewing the screws on the bottom, holding the unit together and flipping it over, and then lifting the pad away from the circuit board. Remove the black and blue wires from the bottom of the board and, with wire-wrap wire, solder them onto pins 4 and 9 (respectively) of the chip on the lower left side of the circuit board (next to resistor number 23). These two lines will now carry the 0–3-volt analog signal (see photo 1). Tape the wires out of the way and gently replace the pad. Then put on the cover, turn the unit over, and screw it back together. The KoalaPad is now ready to plug into the empty socket on the S-100 card. A brief description of the circuit is shown in figure 1. You can use the wire-wrap wire-and-solder method to build the board but the 3M press-pin method is easier. It allows rapid assembly and disassembly. The 3M socket and insertion tool make up

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the 3M wiring system, which is sold as the Whiz Kit by Ragon Inc. of Minneapolis, Minnesota. Its ease and speed justify the high cost of the sockets.

Listing 1 gives you all the programming necessary to get the *x*, *y* values you need for drawing or cursor movement from the circuit board. If you intend to compile the program, it is a good idea to repeat the OUT and INP routines and compare the values you get. This error checking is helpful because the KoalaPad can generate some bogus values because of the execution speed of compiled code.

If the ZBASIC language were changed to take full advantage of the interlace mode, then Zenith would be able to offer true high-resolution color graphics at the lowest price in the industry. ■

Listing 1: *This program is all you need to access the KoalaPad.*

```
10 'LISTING #1
20 OUT 127,0 'START CONVERSION
30 A=INP(127) 'INPORT TOP 8 BITS
40 B=INP(127) 'IN BOTTOM 2 BITS
50 A=A*4:B=B/64:X=A+B '10 BITS
60 OUT 126,0 'START CONVERSION
70 A=INP(126) 'INPORT TOP 8 BITS
80 B=INP(126) 'IN BOTTOM 2 BITS
90 A=A*4:B=B/64:Y=(A+B)/4
```

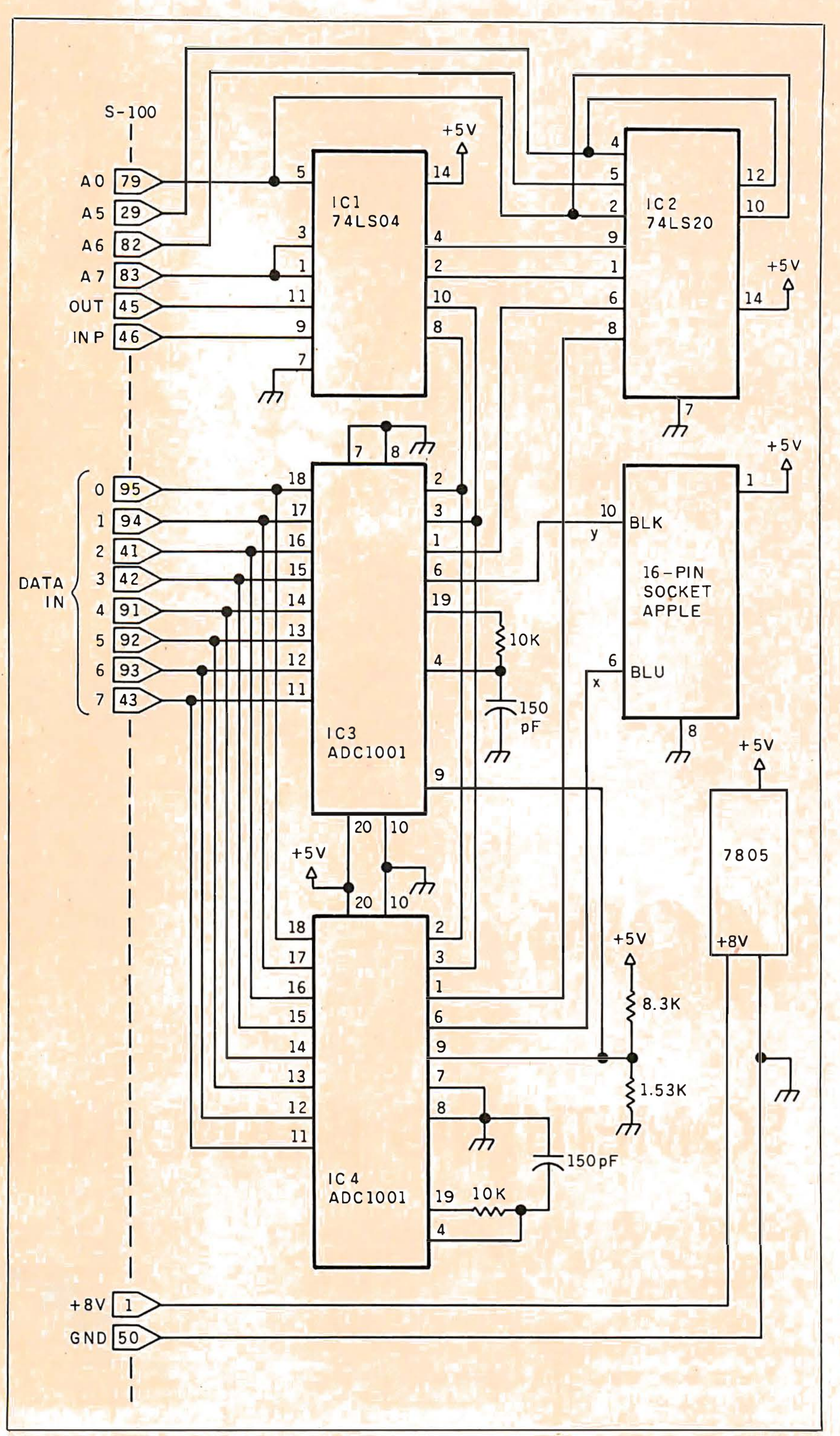


Figure 1: *The* 74LS04 *inverts address signals to the* 74LS20 *to create two chip-select signals for the two* ADC1001s *(U3 and U4). It also inverts the* OUT *and* INP *lines and sends their signals to U3 and U4 as* $\overline{\text{WR}}$ *and* $\overline{\text{RD}}$. *The clocks on pins 19 and 4 of the* ADC1001s *use a resistor capacitor circuit, and reference voltage for the circuit comes from resistors across* GRD *and* +5.

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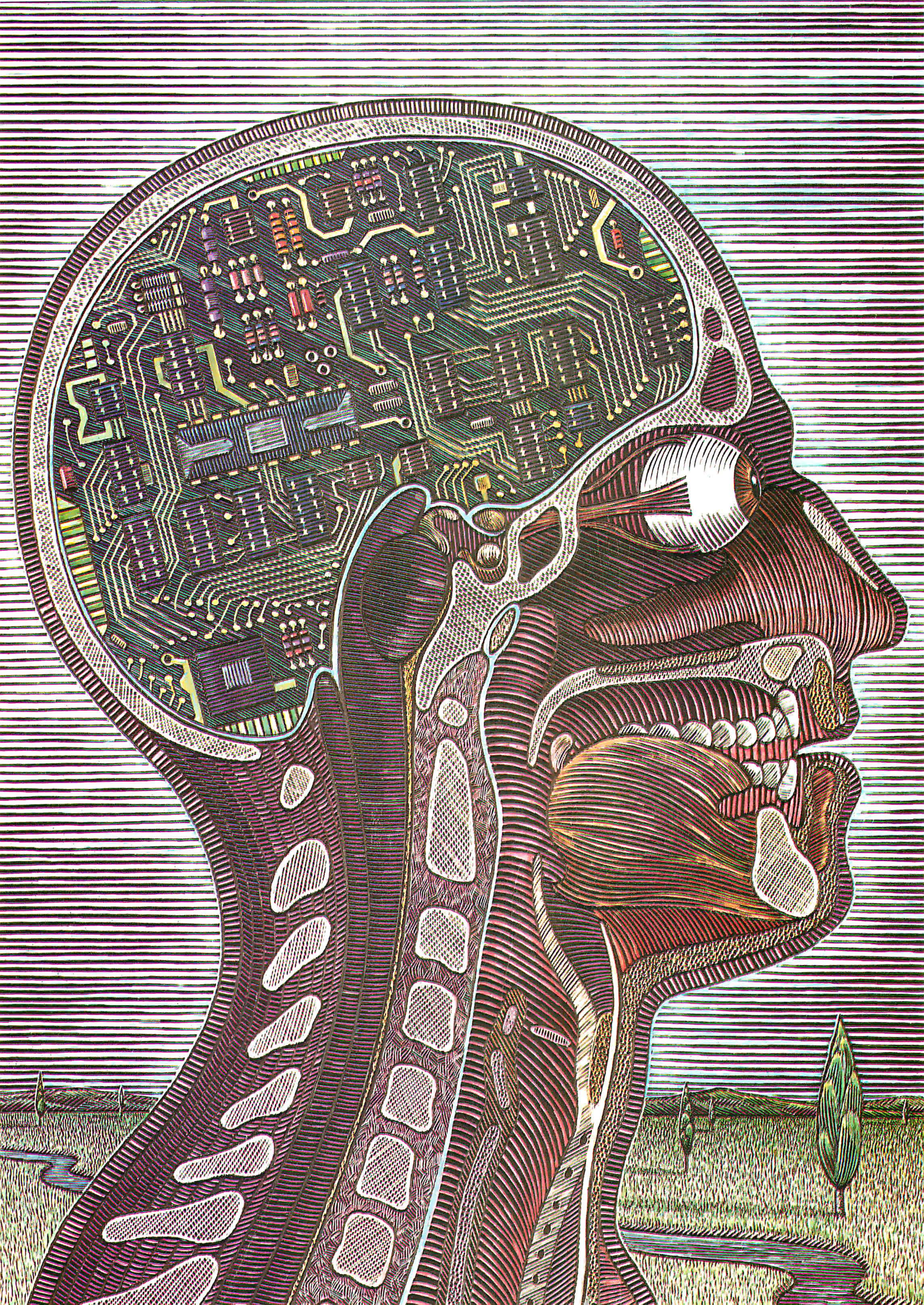
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Understanding artificial intelligence requires understanding intelligence itself. Marvin Minsky of MIT explores the concept of intelligence and considers whether we will be able to communicate with extraterrestrial intelligence when we encounter it. Some of the conceptual structures needed to make computers perform operations natural to the human mind are covered by Roger Schank and Larry Hunter of Yale.

Computer science is among the first fields to benefit from AI. John Anderson and Brian Reiser of Carnegie-Mellon describe their interactive LISP program that teaches people to program in LISP, while Yale's Lewis Johnson and Elliot Soloway explain the operations of their LISP program that finds nonsyntactic bugs in Pascal programs.

If we are to have powerful AI on personal computers, we must have efficient hardware and software. Michael Deering of Schlumberger Research surveys some efficient architectures for AI. After noticing the recent flowering of LISP on personal computers, MIT's Patrick Winston provides an introduction to the language. Carl Hewitt, developer of an early logic programming language, questions whether logic programming will be able to develop intelligent systems for complex applications in the real world.

In their article, Dana Ballard and Chris Brown of Rochester University explain how the miracle of vision rests on hierarchical representations of information as well as on parallel processing. Parallelism is explored further by Geoffrey Hinton of Carnegie-Mellon, who presents two theories of how learning could occur in brain-like networks. Jerome Feldman of Rochester elaborates on key issues in massive parallelism in both natural and artificial intelligence. John Stevens of the University of Toronto takes a bold and intriguing look at the possibilities of copying the brain's own circuitry directly. He starts with the device physics of the brain and goes on to discuss silicon-based designs.

The methods for building expert systems discussed by Robert Michaelsen, Donald Michie, and Albert Boulanger include not only those based on rules but also those based on deeper representations of knowledge. Beverly and William Thompson explain a rule-based expert system written in Pascal.

Space limitations prevented the inclusion of Michael Fichtelman's expert system in Logo and Phillip Robinson's description of a custom AI chip developed at Syracuse University. Look for these articles in forthcoming issues.

Many of the technical terms used in the context of AI involve subtle variations on the traditional computer science definitions. Please consult the glossary on page 138 for definitions of several of these terms.

—*Phil Lemmons, Editor in Chief*



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COMMUNICATION WITH ALIEN INTELLIGENCE

BY MARVIN MINSKY

It may not be as difficult as you think

WHEN FIRST WE MEET those aliens in outer space, will we and they be able to converse? I believe that, yes, we will—provided they are motivated to cooperate—because we'll both think in similar ways. I propose two kinds of arguments for why those aliens may think like us, in spite of having very different origins. These arguments are based on the idea that all intelligent problem solvers are subject to the same ultimate constraints—limitations on space, time, and materials. For animals to evolve powerful ways to deal with such constraints, they must have ways to represent the situations they face, and they must have processes for manipulating those representations. These two requirements are:

Economics: Every intelligence must develop symbol systems for representing things, causes, and goals, and for formulating and remembering the procedures it develops for achieving those goals.

Sparseness: Every evolving intelligence will eventually encounter certain very special ideas—e.g., about arithmetic, causal reasoning, and economics—because these particular ideas are very much simpler than other ideas with similar uses.

The economics argument is that the power of a mind depends on how it manages the resources it can use. The concept of *thing* is indispensable for managing the resources of space and the substances that fill it. The concept of *goal* is indispensable for managing how we use the time we have available—both for what we do and what we think about. Aliens will use these notions too, because they are both easy to evolve and because there appear to be no easily evolved alternatives for them.

The sparseness theory tries to make this more precise by showing that almost any evolutionary search will soon find certain schemes that have no easily accessible alternatives, that is, other different ideas that can serve the same purposes. These ideas or processes seem to be peculiarly isolated in the sense that the only things that resemble them are vastly more complicated. I will discuss only the specific example of arithmetic and conjecture that those other concepts of objects, causes, and goals have this same island-like character.

Critic: What if those aliens have evolved so far beyond us that their concerns are unintelligible to us and their technologies and conceptions have become entirely different from ours?

Then communication may be infeasible. My arguments apply only to those stages of mental evolution in

(continued)

Artificial-intelligence pioneer Marvin Minsky is Donner Professor of Science in the Department of Electrical Engineering and Computer Science at Massachusetts Institute of Technology (545 Technology Square, Cambridge, MA 02139). In the late 1950s, Minsky, together with John McCarthy (now at Stanford), created MIT's AI Laboratory, of which Minsky was the director for several years. Minsky has long been interested in SETI (the Search for Extraterrestrial Intelligence) and participated in the important 1971 conference on communication with extraterrestrials, held in Soviet Armenia and organized by Carl Sagan.

A distinctive aspect of intelligence is the ability to solve new, different problems.

which beings are still concerned with surviving, communicating, and expanding their control of the physical world. Beyond that, we may be unable to sympathize with what they come to regard as important. Yet even then we can hope to communicate with the mental mechanisms they use to keep account of space and time; these could remain as sorts of universal currency.

Critic: How can we be sure that things like plants and stones or storms and streams are not intelligent in other ways?

If you can't say in what respects their intelligence is similar, it makes no sense to use the same word. They certainly don't seem good at solving the kinds of problems that challenge our intelligence.

Critic: What's so special about solving problems? Please define intelligence precisely so that we'll know what we are discussing.

It's not one author's place to tell other people how to use a word that they already understand. Let's just use intelligence to mean what people usually mean: the ability to solve hard problems—like how to build spaceships and long-distance communication systems.

Critic: Then please define what a hard problem is. For instance, we know that human intelligence was involved in building the pyramids—yet coral-reef animals build things on an even larger scale. Should we therefore be able to communicate with them?

No. Humans do indeed solve such problems, but it is only an illusion that coral-reef animals do. An important factor is speed. No single bird discovers how to fly: Evolution used a trillion bird-years to find out how—yet man learned to fly in tens of human-years. And while a person might take several years to find a way to build a structure like an oriole's nest or a beaver's dam, no oriole or beaver could ever learn to do such things at all without exploiting the ancient nest-machines their genes construct inside their brains. A distinctive aspect of what we call intelligence is this ability to solve a wide range of new, different kinds of problems. This is why it makes sense to try to communicate with an individual animal that can learn quickly how to solve new hard problems.

What enables us to solve hard problems so quickly? Here are some ingredients that seem to me so essential that I would expect intelligent aliens to use them, too:

Subgoals—to break hard problems into simpler ones
Subobjects—to make descriptions based on parts and relations
Cause-symbols—to explain and understand how things change
Memories—to accumulate experience about similar problems
Economics—to efficiently allocate scarce resources
Planning—to organize work before filling in details
Self-awareness—to provide for the problem solver's own welfare

Still, aren't these only a few of the myriads of other possibilities? Why can't our aliens do all such things in completely alien ways? I believe that these problem-solving schemes are not as arbitrary as they seem.

The Sparseness Principle

Why does it seem so obvious to us that two and two equal four? Such mysteries have long concerned philosophers—why certain concepts seem to come into our minds as though they need no prior experience or evidence. My answer is that this may be due, at least in part, to the following *computational phenomenon*.

The Sparseness Principle: Whenever two relatively simple processes have products that are similar, those products are likely to be completely identical.

Because of this, we can expect certain a priori structures to appear, almost always, whenever a computational system evolves by selection from a universe of possible processes. The ideas of number and arithmetic are examples of this, and my conjecture is that this may be why different people can communicate so perfectly about such matters, although their minds may differ in many other ways. This may apply to aliens, too. Let me explain the sparseness principle by recounting two anecdotes. One involves a mathematical experiment, the other a real-life experience.

A Mathematical Experiment—I once set out to explore the behaviors of all possible processes—that is, of all possible computers and their programs. There is an easy way to begin that search: you just list all possible finite sets of rules, one by one. This is easy to do using methods that Alan Turing described in 1936; these are what today we call "Turing machines." Naturally, I didn't get very far because the variety of such processes grows exponentially with the number of rules in each set. However, with the help of my student, Daniel Bobrow, I managed to examine the first few thousand of such machines—and we found that among them there were only a few distinct kinds of behaviors. Some of them simply stopped without accomplishing anything. Many of the others just erased their input data and did nothing else. Most of the remainder quickly got trapped in circles, senselessly repeating the same steps over again. There were only a few left that did anything interesting at all—and these were all essentially the same: Each of them performed a counting operation that repeatedly increased by one the length of a string of symbols. In honor of their ability to do what resembles a fragment of simple arithmetic, let's call these *A-machines*. Let's think of this exploration as exposing parts of some infinite

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"universe of possible computational structures." Then this tiny fragment of evidence suggests that such a universe may look something like figure 1.

The Xs represent those useless processes that scarcely do anything at all, while the As represent those little counting machines, which in effect are all identical. Little processes like these, inside our minds, could be seeds of our more mature ideas about arithmetic. My point is that it seems inevitable that somewhere in a growing mind some A-machines must come to be.

Now, possibly, there are some other really different ways to count. So there may appear much later some of what we represent as *B-machines*, which are processes that act in ways that are similar but not identical to the ways A-machines behave. But our experiment hints that even the simplest possible B-machine will be so much more complicated that it is unlikely any brain would discover one before it first found many A-machines.

I think of this little thought experiment as resembling an abstract version of those first experiments in which Stanley Miller and Harold Urey set out to explore with real chemicals the simplest combinations of constituents. They started with a few elements like hydrogen, oxygen, nitrogen, carbon, and phosphorus and found that those chemicals react first to make simple molecules and then go on to form peptides, sugars, nucleotides, and whatnot. Of course, we would have to wait much, much longer before the appearance of tigers, woodpeckers, or Andromedans.

A Real-Life Episode—Once, while I was still a child in school, I heard that *minus times minus is plus*. How strange it seemed that negatives could cancel out—as though two wrongs could make a right, or "this statement lies" could be a truth. I wondered if there could be something else, still like arithmetic but having yet another sign. Why not make up some number things, I thought, that go not just two ways, but three? I searched for days, making up new little multiplication tables. Alas, each system ended either with impossible arithmetic (e.g., with one and two the same), with no signs at all, or with an extra sign. Eventually, I gave up. If I had had the courage to persist, as Gauss did, I might have discovered the arithmetic of complex numbers or, as Pauli did, the arithmetic of spin matrices. But no one ever finds a three-signed imitation of arithmetic because, it seems, it simply doesn't exist.

Try, for example, to make a new number system that's like the ordinary one except that it *skips* some number—say, 4. It just won't work. Everything will go wrong. You'll have to decide what 2 plus 2 is. If you say that this is 5, then 5 will have to be an even number, and so also must 7 and 9. Then, what's 5 plus 5? Is it 8, or 9, or 10? You'll find that to make the new system at all like arithmetic you'll have to change the properties of all the other numbers. Then, when you're done, you'll find that you have changed only those numbers' names and not their properties at all.

Similarly, you could try to make two different numbers be the same—say, 139 and 145. But then, to make subtraction work, you'll have to make 6 the same as 0 and 4 plus 5 equal to 3. Suddenly, you'll find that the sum of two positive numbers is smaller than either of them—and that scarcely resembles arithmetic at all. (In fact, this leads to *modular arithmetic*, which has a certain usefulness in abstract mathematics but is worse than useless for keeping track of real things.) And so it goes.

There is just no way to take a single number out or put another one in. Nor can you change a single product, sum, or prime.

What gives arithmetic this stark and singular rigidity? You cannot make the smallest hole in it or make it stretch or bend the slightest bit. You have to take it as it stands, the whole thing, all or nothing, unchangeable, because it's isolated as an island in that universe of processes. That selfsame A-machine exists, immutably complete, as part of every other process that can generate an endless chain of different things.

I sometimes wonder if it's dangerous to make our children dwell so long on arithmetic since, when seen this way, it leads to such a singularly barren world. True, some children find in it a universe of different things to do. Most children, though, just find it dull—a source of endless rote and pointless pain; it's like the tedium of working clay too cold to mold into any other shape.

From all this, I conclude that any entity who searches through the simplest processes will soon find frag-

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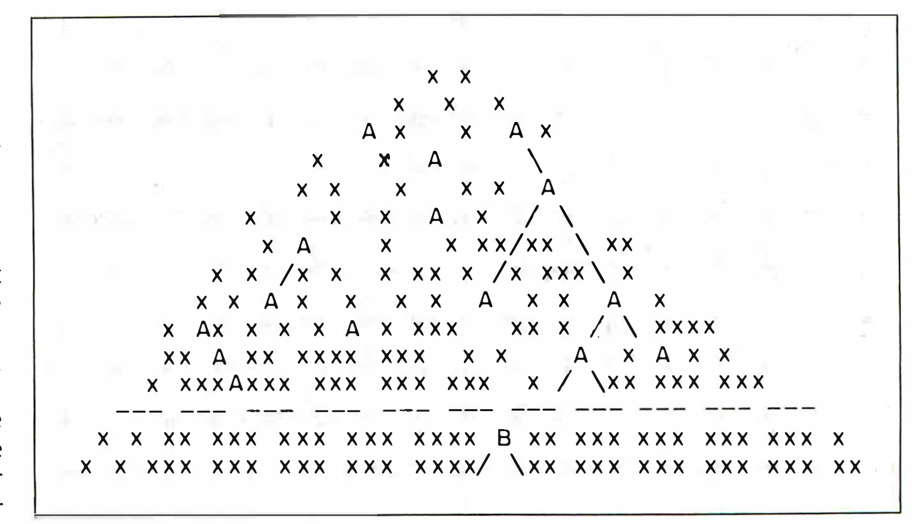


Figure 1: A *universe of possible computational structures.*

ments that do not merely resemble arithmetic but are arithmetic. It is not a matter of inventiveness or imagination, only a fact about the geography of the universe of computation, a world far more constrained than that of real things.

Thesis: All processes or formalisms that resemble arithmetic are either identical to it or else unthinkably complicated. This is why we can communicate perfectly about numbers.

What has this to do with aliens? Only that they too must have evolved by searching through some universe of possible processes, and any evolutionary process must first consider relatively simple systems and thus discover the same isolated islands of efficiency.

Finally, we ought to ask why processes occur that way without some similar ones nearby? It is hard to formulate this precisely, because the meaning of *similar* depends on what you want to use it for. One way to explain it is to point out that a small set of rules can generate a vast world of implications and consequences. But there is no converse because usually a small set of rules can't describe a large and complex thing. This is simply a matter of arithmetic: There just aren't enough small sets of rules to go around! And that explains why we cannot take some set of rules, use it to generate a universe of consequences, make a few changes in that universe, and then describe that end result, again in terms of only a few rules. Now, that altered universe has become one of miracles, not of laws. There are not enough small sets of rules to produce the effect of continuity.

Causes and Clauses

An alien mind would probably be entirely different from ours if how we think were just an evolutionary accident. And then, communication would likely not be feasible. But although every evolution is composed of many accidents, each one tends to first try relatively simple ways at every stage. Since we're the first on earth to develop complex languages, and since these languages probably employ many relatively simple principles, it is likely that alien species will share many of these. I propose this in a form so strong that it may seem entirely preposterous at first: I believe that many aspects of our language/grammar forms may be almost inescapable.

Why do we say things like "*It* soon will start to rain?" Why must we always postulate some agent-cause even when there is no actor on the scene? It doesn't matter if we're right or wrong; we'll find a cause or imagine one. I claim we seek some cause for every difference, move, or change. Sometimes our language syntax forces this on us, but I claim it is not merely a matter of verbal form; it stems from deeper causes in the ways we think. My guess is that even before our ancestors began to speak, they first developed special brain machinery for representing objects, differences, and causes, and our language/grammar later reflected these. Specifically, I suspect that many of our thought processes are based on using the following kinds of mental symbol representations:

Object-symbols representing things, ideas, or processes—In languages, they often correspond to nouns. Our minds tend to describe every situation, real or mental, in terms of separate object-things and the relations between them.

Difference-symbols representing differences between, or changes in, objects—In languages, they often correspond to verbs. When any object undergoes a change or two objects are compared, the mind ascribes some differences to them.

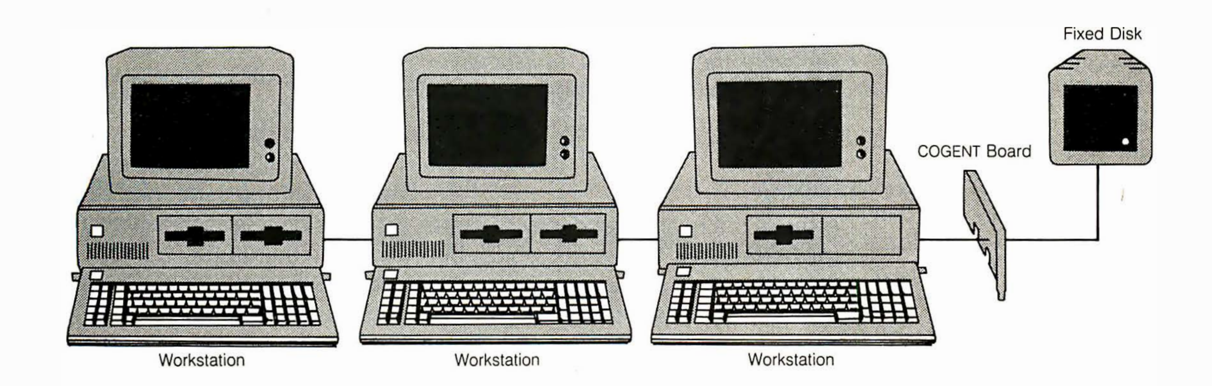
Cause-symbols—When any difference is conceived, the mind finds a cause for it, a something that is held responsible. And we use a clever mental trick to represent causes in much the same ways that we represent objects.

Clause-structures—For describing complicated situations, we have a trick that lets us treat any expression

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or description, however complicated, as though it were a single component of another description. In languages, this corresponds to using embedded phrases and clauses.

It is that final self-embedding trick of representing prior thoughts as things that gives our minds their awesome power. For this permits us to reuse the same brain machinery over and over again, at each step replacing an entire conceptualization by a compact symbol. That way, we can build up gigantic structures of ideas as easily as our children build great bridges and towers from simple separate blocks. That way, we can build new ideas from old ones—and that is what enables us to think. This applies to our computers as well.

This must be why our languages also have structures that we can reuse: Our thoughts themselves must use the same machinery repeatedly. That's how our thoughts extend themselves to infinite variety. And, unless aliens do that too, they cannot turn their thoughts to the prior products of their thoughts. Without this trick of turning symbols on themselves, you can't have general intelligence, however excellent your repertoire of other skills may be.

Critic: You might as well argue that the aliens will speak English if you claim they too use nouns and verbs and compound embedded sentences. But what if they don't think in terms of objects and actions at all?

I don't think it's an accident that we think in terms of thing and cause. Whatever may occur, that form of representation leads us always to wonder who or what is responsible. And so, this evolutionary trick leads us to search to find dependencies that help predict—*and hence control*—not just the world outside but also what may happen in the mind. Perhaps it's also why we all grow up believing in a *self*: perhaps that "I" in "I just had a good idea" stems from that same machinery. Because if you are compelled to find something to cause the things you do, that something needs to have a name. You call it "me." I call it "you."

Critic: But what's so great about dependencies? Why can't some aliens perceive entire scenes as wholes instead of breaking them down into those clumsy parts? Why not, instead, see what there really is, holistically—a steady flow of flux in space in time, instead of arbitrary form-filled mind-made fragments of approximations to reality?

It surely is a healthy tendency to yearn for better ways to see the world. But worshipping as-yet-undiscovered transcendental schemes can blind us to the power we draw from our usual ways of separating things. Each animal must pay a corresponding price in energy and nourishment for each machine it carries in its brain. Just as clause structure in language lets us focus our entire word machine on each part of a description, our concept of seeing separate things lets us factor situations into parts and then apply our whole mind machine to each part of the problem. Enthusiasts of holism have never understood the hidden cost a mind would have to pay to "see everything at once." We'd never be able to see anything clearly at all.

There have been many speculations on how brains might use something like holograms for memories. But on one side there is no evidence for this; on the other there are few advantages to it. Holograms store no more information than other methods, and computer scientists know other, better ways to add redundancy to memory to make it robust and injury resistant. It is true that holograms can simplify certain kinds of recognitions, for instance, deciding whether a picture contains copies of some specific other picture. But that also makes it much more difficult to make most other kinds of decisions, to say whether a picture contains two subpictures that share some specified relationship. In fact, a hologram may be almost the worst possible way to represent relations among the things it represents, because memory and learning are useful only when they inform us about relations that are at least partially predictable. We do not want our memories to give equal weights to every arbitrary feature of a situation. If a scene contains 50 features, you don't want to equally consider all the quadrillion possible subsets of those features. And so we need some methods for isolating and grouping that can emphasize the most usefully predictable subsets. In short, without the additional constraints on relations between features, which result in the concept of an *object*, we'd simply never see the same thing twice. Then we'd have no way to learn from our experience. No knowledge could accumulate.

Causes and Goals

How does having memory help—when no two problems are ever quite the same in all respects? Our past experience would seem to have no relevance unless we had some ways to see which aspects of the world remain the same, while others change. This is why knowledge cannot have much use unless expressed in terms of relations between *predictable* features and the actions that we can take. But given these it then may become possible to predict which actions might cause undesirable features to disappear.

To say that "y happened because of x" is, in effect, to say that x can help you to predict which actions can lead to y. It helps to control its environment if an animal can find such *causes*—fragments of predictability that work better than chance. But such predictions aren't useful when too many small effects add up. What are causes anyway? The very concept of a cause involves a certain element of style: A causal explanation must be brief. Unless an explanation is compact, we cannot use it to predict. We would agree that x is a cause of y if we see that y depends much more on x than on most other things. But we wouldn't call x a cause if it were a discourse that carried on and on, mentioning everything else in the

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whole world and never coming to any point. This applies to objects too.

There can't be any objects, things, or causes in worlds where everything that happens depends, more or less equally, on everything else that happens.

It makes no sense to talk about a *thing* in such a world, because our very notion of a thing assumes some constellation of properties that stays the same or changes ways we can predict, when other things around it change. When you move an object, its location changes—but not its color, weight, material, size, or shape. How convenient that our world lets us change a thing's place and still leave so many other properties unchanged. If this were not the case, the number of combinations to keep track of would grow exponentially with the number of features we perceive and we would have no sense of what *causes* things to happen.

To deal with something complicated, you must find a way to describe it in terms of substructures within which the effects of actions tend to be localized. To know the cause of a phenomenon is to know, at least in principle, what can change or control it without changing everything else. This is useful when it enables us to change one thing without making other things worse.

For a mind to discover causes in its world, it must have sensors that detect changes that are predictably related to the actions it can take. Fortunately, evolution tends automatically to select just such matched sets of sensors and effectors, because in virtually any environment an animal's survival is enhanced if its actions are based on good predictions. So we can expect evolutionary processes to accumulate mechanisms that reflect the causal laws that operate in their environments. And it would seem that the most powerful methods are those that let you make predictions about the effects of contemplated action chains, that is, the ability to make plans.

Problems seem hard when their solutions aren't obvious. The most general way we know to solve problems is to set up systems that have some way to make "progress toward a goal." In the late 1950s, A. Newell and H. A. Simon worked out a theory of what they called the "General Problem Solver." This is a theory of how to reach a goal by *making progress*—finding actions that can replace each problem that has a *high-level difficulty* by other problems, each of which has a lower-level difficulty. No one can prove that all intelligent problem solvers, however alien, must use this selfsame principle. But until we find another, comparably general idea—and none is on our horizon—it is hard to imagine how an intelligence could evolve without exploiting some such idea of goal.

RELIABLE COMMUNICATION

Before we ask how aliens communicate, we ought to ask how humans can. Is there ever a word that means the same to any two of us? Everyone must have wondered once, "Could two persons have different meanings for every word, yet never sense that anything is wrong?" What if each thing that's green or blue to me is blue and green to you? The sparseness theory claims that we need have no fear of that, at least for technical concepts, since one of the two outwardly indistinguishable meanings would probably be vastly more complicated than the other and would never have been conceived in the first place. Sparseness means we can trust one another.

We know very little of where that idea might lead because we know so little about how sparseness isolates any particular concept. But the general idea does seem to support the mathematical and physical intuitions proposed by Hans Freudenthal in *LINCOS*, his book on alien communication, perhaps even in regard to the miniature models he suggests for discussing social and administrative subjects. There is one problem though: Introspection is a poor guide for guessing which of our common-

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sense concepts are really simple, because many things we find easy to do use brain machines whose complexity we cannot sense. For example, we find it easy to stand on two feet, but some aliens might find that quite astonishing.

What other ideas are likely to be universal in the sense of being islands in that sea of possible ideas? Surely the mathematical notions of utility, linear approximation, probability, and the simplest program-like processes are. These could serve to communicate much about trade and commerce, basic facts of biology, and even many principles of mental life—e.g., about objects, goals, and memories. At some point, though, sparseness must fail, because things that are more complicated will have all kinds of variations and alternatives, and communication will encounter obstacles of every sort.

THEREFORE

There is little more that I can say today with any scientific certitude. Tomorrow there could be more, perhaps because of soon-to-come gains in computational power that could let us explore a little further into the mysterious ocean of all possible simple machines. There we might find a few more ideas isolated enough to share with other minds. Such explorations also might tell us more about the origin of life itself by showing us the simplest schemes that could support the simplest forms of evolutionary search. ■

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A GLOSSARY OF ARTIFICIAL-INTELLIGENCE TERMS

AND, OR, AND STREAM PARALLELISM: different techniques for implementing parallel operations, based on *and*, *or*, and pipelined execution hierarchies.

BAGS: formal mathematical objects that differ from sets in that they allow duplicate items.

BLACKBOARD: used in systems composed of independent modules as a means of communication. The blackboard is a common area of memory containing system-state data that all modules can access.

FRAME: a knowledge structure (or database) used to describe the attributes that an object possesses, arranged in a "slot and filler" format. Each slot and its contents carry information about a particular aspect of the object.

GRAIN SIZE: when used in conjunction with parallel processing, grain size refers to the complexity of the code chunks allocated to each processor. For example, if processor A is assigned to perform an addition operation while processor B is assigned to perform a sort operation, the grain size of the code assigned to processor A is smaller than that assigned to processor B.

HEURISTIC: a technique that improves the efficiency of a problem-solving process, even though its use cannot be strictly justified. In AI, heuristics are typically used to reduce the time required to solve extremely complex search problems.

KNOWLEDGE ENGINEER: an AI programmer who constructs expert systems.

PREDICATES AND DEMONS: a predicate is a type of function that tests for some condition involving its arguments. A demon is a procedure that activates automatically in response to recognizing a predefined state.

SCRIPT: a frame-like knowledge structure used to represent related sequences of events. The slots in a script contain information concerning an event (where the event occurs, people involved, objects manipulated, etc.), and the events are linked in a causal chain.

SEMANTIC NET: a graph of nodes and connecting links; the nodes represent objects, and the links represent relationships. A family tree is a good example of a semantic net.

TAGGED MEMORY ARCHITECTURE: in AI applications, tagged memory architectures use part of each memory word to convey information about the data stored in the remaining bits of that word, including the data type and format.

UNIFICATION: a pattern-matching method; the result of a unification is the assignment of values to the variables of two patterns so that both patterns become identical.

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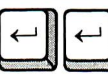
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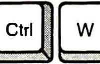
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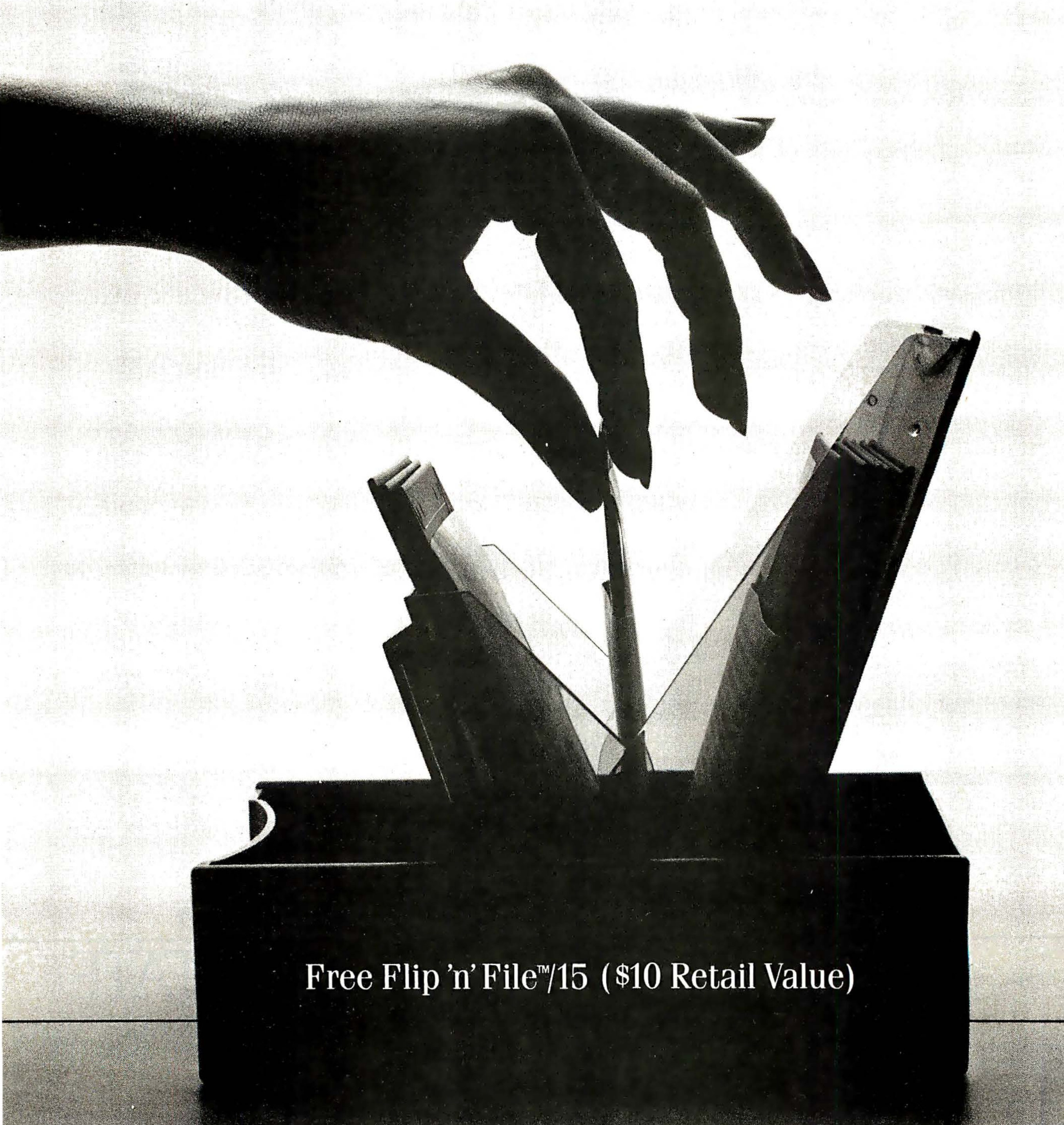
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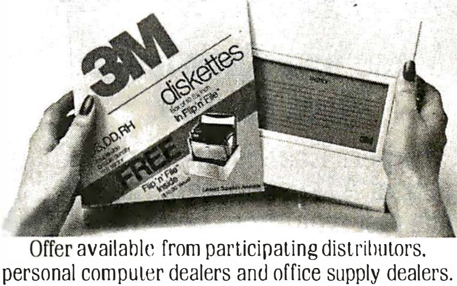


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THE QUEST TO UNDERSTAND THINKING

BY ROGER SCHANK AND LARRY HUNTER

It begins not with complex issues but with the most trivial of processes

ARTIFICIAL INTELLIGENCE, or AI, takes as its subject matter some of the most daunting questions of our existence. What is the nature of mind? What are we doing when we are thinking, feeling, seeing, or understanding? Is it possible to comprehend how our minds really work? These questions have been asked for thousands of years, but we've made little tangible progress at answering them.

AI offers a new tool for those pursuing the quest: the computer. As anyone who has used one can attest, computers often create more problems than they solve. But for probing the issues of mind and thought, that is just what we need.

The fundamental use of computers in helping us understand cognition is to provide a testbed for our ideas about what the mind does. Theories of mind often take the form of process descriptions. For example, a theory of question answering might claim that people first translate a question into an internal representation, use that representation as an index into memory, translate the recalled memory into an appropriate form for an answer, and then generate the words to communicate it. (This example is offered not as a real theory of question answering but as an example of what a process theory of mind might look like.)

Process theories seem to be a good way of describing what might go on inside the brain. One problem with them, however, is that all too often what looks like a good description really isn't specific enough to make the theory clear. "Use the representation as an index into memory" isn't a good explanation of the processes behind remembering a fact. How are facts recalled? How is the memory organized? What happens when memory gets very large? What if a fact isn't directly encoded in memory but can be inferred from something that is? A researcher trying to write a program that embodies the above simplistic theory would run into all of these problems and more. That's why we need to write programs. Programming forces us to be explicit, and being explicit forces us to confront the problems with our theories.

Not long ago, AI researchers like ourselves focused on what they considered to be manifestations of highly intelligent behavior: playing chess, proving mathematical theorems, solving complex logical puzzles, and the like. Many AI researchers devoted a lot of energy to these projects and found powerful computational techniques for accomplishing such "intelligent" tasks. But we discovered that the techniques we developed are not the same ones that people actually use to perform these tasks, and we have instead begun to concentrate on tasks that almost any adult finds trivial: using language, showing common sense, learning from past experiences.

LANGUAGE

We began studying these "trivial" tasks by trying to write programs that

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People understand a great deal more than the lexical content of an utterance.

could use English (or other natural languages) in a useful way. We wanted such programs to be able to understand the written word well enough to summarize it, translate it into another language, or answer questions about it. We were immediately confronted with the fact that people understand a great deal more than just the immediate lexical content of an utterance. For example, most people would agree that the sentence "John bought a new car" contains a reference to money, even though the word "money" does not appear in the sentence. Any program that understands that sentence would have to be able to answer "Yes" to the question "Did John spend money?"

How could a program know that? One approach might be to associate "money" with the word "bought," claiming that "buy" means "trade money for." This method uses the meanings of the various words in the sentence to build up a representation of the meaning of the whole sentence. That is more or less the right approach, but it has some problems. For one, words are ambiguous, and the inferences we make about their meanings can easily be wrong. "Buy," for example, doesn't always mean money changes hands, as in: "John bought Mary's argument." Ambiguity is so widespread that any program dealing with natural language must have powerful methods for handling it.

Another problem is that often underlying meanings do not come from the definitions of any particular word. Consider the following story: "John went to a restaurant. He ordered a sandwich. The waiter brought it quickly, so he left a large tip." The meaning of this story obviously includes the fact that John ate the sandwich and paid for it. However, those actions are not implicit in any particular word in the story. How might a computer program infer them? It would have to know about what goes on in restaurants. A person could also conclude that John probably looked at a menu, that he sat at a table, that a cook made the sandwich, and so on. The program needs to be able to fill in the unmentioned gaps in a text with information about the events being described.

There is a solution to both problems: The program must be constantly generating expectations about what will happen next. Ambiguity is rarely noticed by human speakers because the context makes clear which meaning is correct. For a program to be able to resolve ambiguity, it must build up a "context" as well. In other words, the program must have some idea of what will happen next, based on what has happened previously and what it already knows about these kinds of situations. Expectations are very helpful in resolving ambiguity; the expected sense of an ambiguous word is the one that should be assumed. The expectations set up by "The bartender poured scotch on . . ." makes it easy to use the proper sense of "the rocks."

Expectations also help fill in the gaps in a story. They commonly come in bunches or *packages*. When we hear about a restaurant, we expect to hear about a variety of objects, events, and people. There should be a menu, the patron should look at the menu, pick something, tell the order to a waiter or waitress, wait for a while, be served, eat the food, have the table cleared, get a check, pay the check, leave a tip, and depart. As is obvious from this example, expectation packages can be temporally ordered, which makes it possible to infer that "John ate his sandwich" in the earlier example. When an expectation is satisfied, the program can infer that the expectations temporally prior to it are probably also satisfied. People know about common sequences of actions in the world and use that knowledge to generate expectations. There is no way to understand language without knowing something about the subject matter under discussion.

To build programs that test these ideas, we had to figure out what kinds of expectations exist and specifically how they are used. First, we looked to human behavior to guide us. People constantly generate expectations at many different levels of specificity. We have expectations about what syllable sounds are likely to be heard next that help us resolve ambiguous sounds into words. We have lexical expectations about what words or classes of words will come next. We have expectations of events that are likely to occur. We also have a variety of expectations about other things, like the kinds of goals that various people may have, plans and counterplans involved in pursuing those goals, and emotional reactions to various events.

Then we thought about how a program might handle this. In some sense, every natural-language parser uses expectations. The difference between a traditional, strictly syntactic parser and a more conceptual parser is the source of its expectations. A syntactic parser uses only knowledge about grammar. A conceptual parser uses information from many sources, grammatical and otherwise. While a traditional parser sees syntactic analysis as a preliminary process for other analyses, a conceptual parser sees syntax as only one of many sources of information used simultaneously to understand text.

Many of the low-level expectations of our parsers come from the vocabulary used to represent meaning. Some of our programs have used conceptual dependency (CD) to represent meanings (see reference 1). The basic CD form has slots for an action, an actor, an object, and a directional component (from or to). Each CD action has associated semantic constraints on the kinds of entities that can fill its slots. For example, the CD action *ingest* requires that its object be edible and its actor be alive. When any word that refers to "ingest" appears in a

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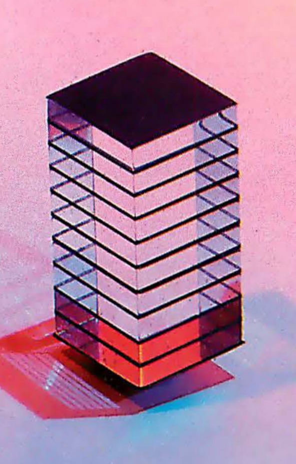
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text, expectations are generated to hear about an edible object (generally after the word meaning "ingest") and a living actor (generally before "ingest"). Notice that the expectations generated are both semantic (predicting a word or meaning) and syntactic (predicting where the word might be found). Of course, even the CD action may be ambiguous. One way to clear up the ambiguity in such cases is to generate the expectations from both possible meanings and pick the action whose expectations are met by the remaining words in the story. This technique could be used to clarify the meaning of "buy" in the earlier example; "buy" would generate two sets of expectations, one predicting a valuable object and the other predicting an opinion. When one expectation set was satisfied, the program could deactivate the other.

There are many other ways to clear up ambiguities. More complex expectation schemes can provide better information. Consider the restaurant story above. The sentence "The waiter brought it quickly, so he left a large tip" has an ambiguous pronoun, "he." Standard rules for pronoun reference fail here; sex and number don't differentiate, and "he" does not refer to the most recent agreeing antecedent, "waiter." The only way to clarify the meaning of this pronoun is by the expectation that patrons leave tips for servers. You might try associating this information with the appropriate meaning for the word "tip," but patron and server are not just semantic restrictions on slot fillers. John might be a patron in this episode, but he might act as a server in some other situation. The patron/server/tip expectation and the identification of John as a patron must come from a package of expectations about restaurants.

When we began to use packages of expectations in programs, we discovered a few things about packages. First, any story will refer to many packages, and the packages can relate to each other in many different ways. Packages can be grouped together themselves (date = drive, restaurant, drive, movie, drive) or can fill slots in some other package (the "pay" slot of restaurant might be filled by "wash dishes"). They can occur at the same time (eating and taking an airplane) or be incompatible (driving an automobile and taking an airplane). Packages can also have word senses associated with them. In the restaurant package, "tip" is more likely to mean "money" than "end point." This kind of associated lexicon doesn't solve the problem of ambiguity, but it is a helpful tool.

We also ran into some problems with packages. How could a program figure out which package to use at any given time? It is reasonable to add activation conditions to a package that specify the situations in which that package might be relevant. Early programs just looked at each package to see if its conditions had been met. As the number of packages increased, their organization had to improve. We needed some way of finding the right set of expectations at the right moment, without looking at every package. As we built programs that used packaged expectations and gave them real stories (taken verbatim from the UPI newswire), we noticed that sometimes expectations failed. These failures were often very interesting events. We began working on ways to determine the difference between a failed expectation and an unresolved one that should be inferred.

Another problem was picking what was to be a package and what wasn't. There are many things about *eating at home* that are like *going to a restaurant*. Do the expectations about eating at home come from the same package or a totally different one? How about eating in different restaurants? We needed a theory of how to organize and find groups of expectations.

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Briefly, we began by looking at language. We wanted to generate a program that would read a few sentences and answer questions about them. We have found that, in order to do this, we need to build expectations about the subject matter of the text. Those expectations come from many diverse sources of knowledge and are bundled together into packages. We then have to consider what kinds of packages there are and how we can organize and use them. What began as a study of language has turned into a study of knowledge and knowledge organization—in other words, a study of memory.

MEMORY

Where do predictions come from? How do we know what to expect next? We use relevant previous experiences to help us understand. Newborns can't comprehend restaurant stories, and people who have worked in restaurants can read more into seemingly insignificant events. We encode what we see in terms of what we have already experienced. That is why two people can see the same event and yet understand it very differently—they each bring different beliefs and expectations to bear. Our ability to understand a situation comes from our ability to compare it to relevant previous situations. The knowledge we gain from experience—episodic memory—is the same knowledge we use to understand—semantic memory.

How does this relate to our prediction packages? The first thing we noticed was that using packages might be an efficient way to remember episodes. Instead of having to store every event in an experience, a program could just save a pointer to the prototype (*restaurant*, for example) along with those parts of the experience that weren't part of the package (for example, the patron was John, the food was a sandwich, the tip was large). Memory need only register those parts of an episode that differentiate it from the prototype. Since packages contain what we expect in a situation, they are effectively prototypes; hence, they can serve to organize memory of events. Our packages now have another role to play: They should accomplish the functions of event memory as well as provide the expectations that aid in understanding.

If packages are to function as memory as well as processing structures, they have additional requirements. First and foremost, a memory system must be dynamic. The memory must be altered by its experiences. A memory system that fails to respond to new inputs and learn from its experiences is not very useful. A memory system that produces expectations must be able to respond to expectation failures by reorganizing itself to provide better expectations in the future. Second, a memory system must be able to find what it knows. This may not seem very hard, but it is. The task of memory is to take a given event and find related events. But what constitutes a "related" event, and how do we know where to look for one? These two goals—remembering and learning—drive our theorizing about the structure of memory. We need to understand how knowledge is structured and how it can change.

We also have a powerful technique with which to investigate the structure of human memory: reminding. Reminding is a ubiquitous phenomenon; people are constantly reminded of one thing by another. You can be reminded of an object, a person, or a situation. In the course of normal conversation, people are often reminded of previous events. During the mental processing of that conversation, some memory is activated to help understand the new input. The fact that one experience reminds us of another indicates that we are using the same structure to process one as to remember the other. By examining the process of reminding, we can explore the structure of memory.

Armed with our new conception of memory structures, let's return to our restaurant example. Suppose that when John received the bill, the waiter

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Common sense is knowing about a lot of things and using what you know in a variety of situations.

had made an arithmetic error and charged him too much. John noticed this and complained. The waiter was apologetic and not only fixed the error but offered John a free dessert. John—or any dynamic memory system trying to understand what is happening—should record this deviation from the expected routine. If he were later to notice a similar error while buying auto parts, he might be reminded of his experience in the restaurant. He might then expect compensation from the store to make up for the mistake. How can an experience in an auto-parts store remind you of an experience in a restaurant? There must be some memory structure that is used to understand both experiences. In addition, by storing information about expectation failure (and its results) in the shared structure, we automatically make an appropriate generalization.

What does this tell us about the organization of memory? Surely not all the expectations are the same across these events; John doesn't expect to see a menu or be served a lobster dinner in the auto-parts store. But some expectations are indeed the same: He expects to find out what is available, to tell someone what he wants, to receive it, to get a bill for what he has ordered, and to pay the bill. Some major scenes happen in one event and not in the other; there is no equivalent to being directed to a table by a hostess in the auto-parts store. Also, the specifics added to the generalized scenes are different. For example, in an auto-parts store you find what you want by looking through fat catalogs of numbered parts sorted by model and year; in a restaurant, you look at the menu.

We can draw several conclusions about memory structures. Packages are nested, that is, packages have subpackages. In AI terminology, the packages are called MOPs (for memory organization packages), and the subpackages, scenes. Scenes are shared—most appear in many MOPs. Examples of scenes might be *pay* and *order*. It is important to note here that there is no "correct" list of packages. The packages that any dynamic memory system uses at any particular time depend on its own prior experiences. Furthermore, a MOP contains information about the specific details of its own scenes. These details are called *colorations*; for example, the restaurant MOP might color the pay scene by specifying the acceptable types of payment in a restaurant (cash, credit, dishwashing, etc.).

The ability to share scenes provides a mechanism for making useful generalizations. When there is an expectation failure and the source of the expectation is part of a shared structure, the failure and any new expectations based on that failure are stored in that structure. When a similar situation occurs, even in a different package, the previous failure comes to mind (is reminded) because it is stored in the shared scene. Then it can be used to help guide processing. A program using this system might learn to count its change in the auto-parts store after being shortchanged in the restaurant, since both use the pay scene. This combination of failure-driven learning and shared memory structures is quite powerful. Expectation failure can also be used to build new MOPs from old ones by changing the colorations or the order of scenes (for example, in fast-food restaurants, you pay before you eat).

Many more kinds of memory and processing structures are used in our AI theories and programs than we can describe here, but the basic requirements of a useful memory organization should be clear. (For more information, see references 2 and 3.) What

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may not be clear is how important memory and its organization are to nearly all cognitive activity. Getting just the right piece of knowledge at the right moment from our huge and constantly changing memory is not only crucial for language understanding but crucial for exhibiting common sense (which is really just knowing about a lot of things and being able to use what you know in a variety of situations), for applying expert knowledge, for writing interesting stories, and for accomplishing a host of other tasks. Being able to learn from experience and apply that knowledge in relevant situations is an important step toward actual intelligence.

WHAT IS AI?

The term "artificial intelligence" has been much abused of late, and we would like to try to clarify what we mean by it. Programs that manifest theories of knowledge do interesting, sometimes even impressive feats. But many programs that are not attempting to model cognition also do impressive things. The public perception of AI has focused on the *artificial*. Computers are indeed doing things we never imagined machines could do. Computer scientists and engineers are constantly expanding the usefulness and power of their machines. That is important science and engineering, but it is not AI. AI focuses on *intelligence*, something that remains mysterious and elusive. Most good AI programs aren't terribly useful, and many very useful, "smart" programs aren't AI at all. If this distinction were understood, we could avoid a lot of confusion and disappointment.

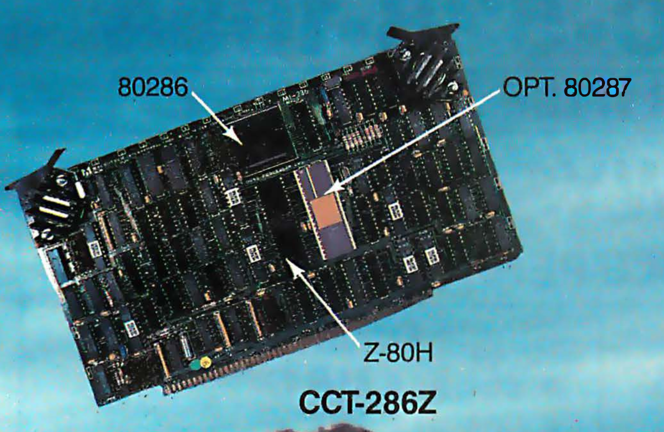
So-called expert systems are a case in point. These programs, more accurately dubbed "rule-based," do not attempt to reason the way a human expert would. They often do very useful tasks, and that's great, but they are not model theories of intelligence. A human expert is not someone who is just following the rules. He has the *experience* to know when he is seeing an exceptional case, and he can recall relevant past cases to help him figure

(continued)

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out what to do. AI theories of expert behavior must describe how an expert knows when something doesn't fit his general rules and what to do about it. AI theories need to account for how experts change and add to the rules they use, based on the success or failure of those rules.

Artificial intelligence is a much more basic science than is popularly believed. Many of our best AI ideas require a great deal of work before they can become useful applications. And when an AI idea is turned into a useful system, in some sense it isn't AI anymore. The construction of such a system requires all kinds of non-AI programming effort—to make the idea work in a real environment, on real computers, in some useful way. Such a system is made possible by the AI idea, but the program's merit comes from its functionality, not its heritage. The fact that a program is based on an AI idea is no way to judge its functionality.

Are there any applications of AI? We think so. If we are gaining insights into how people think, then our findings should help people think better. Perhaps AI's most important applications will not be the programs that we write but the newfound ability to understand how people think. As we find out more about how people read, understand, and create, we may be able to help them do those things better. Perhaps AI's most promising applications are in education—helping to teach people how to read, remember, and think based on a fundamental knowledge of those processes.

Let's consider the problem of teaching children—or adults—to read. In trying to write programs that can read, we have learned a great deal about the reading process. Perhaps we can transfer some of this into improved techniques for teaching reading. Of course, this is not always a straightforward task, but we believe it is possible. Expectations play a central role in understanding text. As children build up expectations about words and stories, they become better readers. Language ability is strongly tied to knowing the content of the material, so the books children read should relate to what they know. We may be able to write better reading textbooks by using expectation packages that children know about. We can write textbooks that encourage them to use their knowledge to fill in the details behind the text, to make inferences. Since AI has focused on language for most of its existence, it has a lot to contribute to reading education. But that's not all AI has to offer; its promise extends throughout education and beyond. AI should eventually provide insights into how to learn and remember better, how to improve explanatory faculties, and even how to extend creativity.

Artificial intelligence is part of the grand attempt to understand thinking. We believe it is making important contributions to that endeavor, and that is the goal of our science. The programs we write are experiments, not results. Our interest is intelligence, not artifact. As we make progress, our results may prepare the way for the automated companions that could become an indispensable part of everyday life. These will not be our real results, though. The real results will be a new kind of understanding of ourselves, an understanding that is ultimately much more valuable than any program. ■

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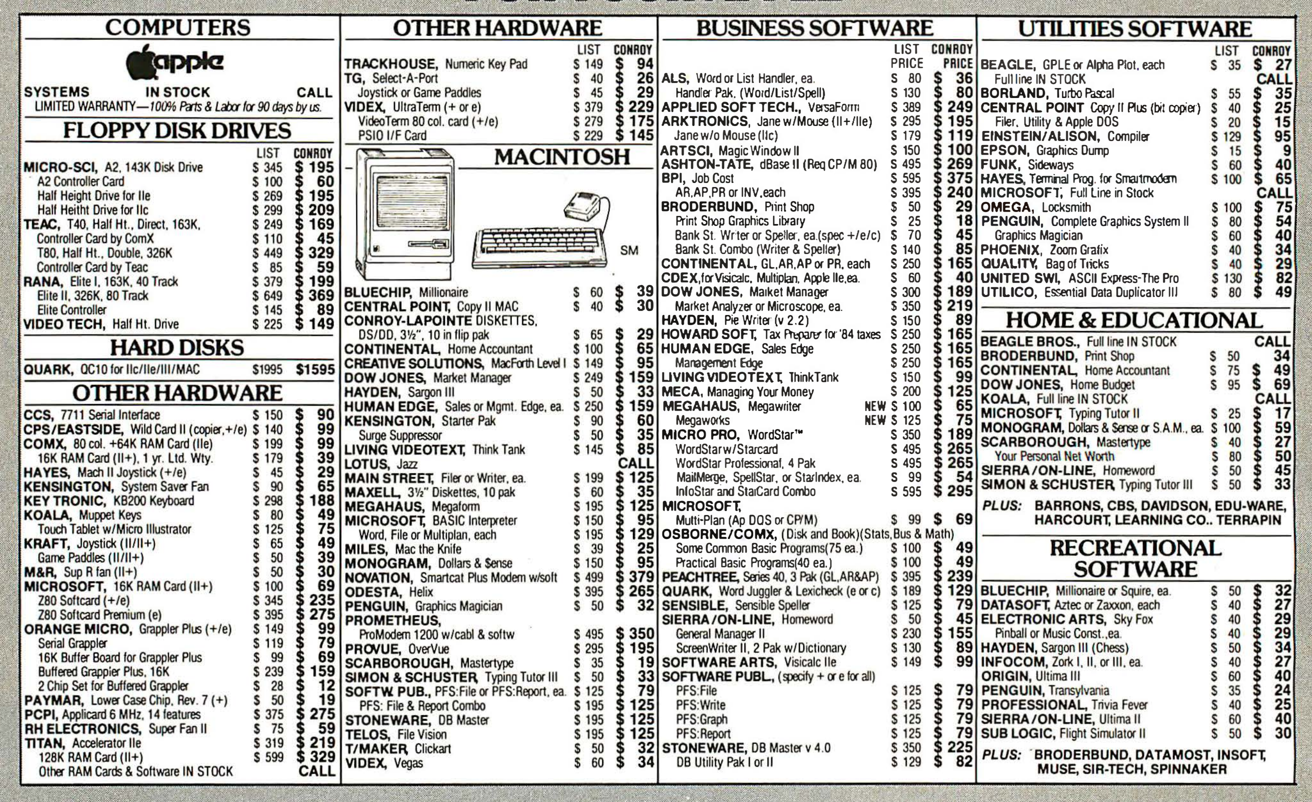
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THE LISP TUTOR

BY JOHN R. ANDERSON AND BRIAN J. REISER

It approaches the effectiveness of a human tutor

FOR THE LAST FIVE YEARS, we have been studying how students learn mathematical, logical, and programming skills. We have reached the point where we can develop computer-based tutors for such domains. This article discusses our work on a LISP tutor. LISP is one of the main programming languages of artificial intelligence (AI) and has gained importance with the rising prominence of AI.

Universities like ours, Carnegie-Mellon University (CMU), are seeing a rapidly increasing demand for courses in LISP. Many students here learn it as their first programming language. But LISP is quite difficult because of its symbolic nature and its use of recursion and because of the need to learn abstract AI programming techniques. We see a remarkable range of mastery from courses designed to teach LISP. Some students find that a single course serves as their entry into the world of AI; others leave feeling they have learned nothing.

Studies of students learning such cognitive skills have revealed that private tutoring appears to be much more effective than conventional classroom instruction. Classroom learning involves listening to lectures, reading texts, and working alone on homework problems. Private tutoring provides the student with an experienced person to guide his reading and problem solving. In a comparison involving LISP, we found that students with private human tutors needed only 11 hours to learn as much as classroom students learned in 43 hours. In both situations most of the time was spent actually trying to write LISP programs rather than reading or reviewing the instruction. The major role of the tutor is to make the problem-solving episodes more effective learning experiences.

Educational psychologists have observed that private tutoring is an advantage with many different types of material. One study (see reference 1) compared students who spent the same amount of time learning—some with private tutors and some in the classroom—for two different subjects, probability and cartography. Ninety-eight percent of the tutored students did better on performance tests than the average classroom student did. Interestingly, the major benefit occurred with the poorer students. There was relatively little advantage of private tutoring for the best students.

Our goal has been to develop a computer-based tutor that is as effective in teaching LISP as a human tutor. GREATERP (Goal-Restricted Environment for Tutoring and Educational Research on Programming) is an attempt to combine artificial-intelligence technology and a psychological theory of skill acquisition into an effective teaching device. This tutor is itself a large LISP program that runs under Franz LISP on VAXes. We have already begun field testing this tutor in CMU classrooms and have seen it lead college students to faster, more effective learning of LISP programming. In this article, we discuss how the tutor works, why it is effective, and the prospects for moving a version of it to personal computers.

GREATERP is only one of the tutors

(continued)

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that we have developed at Carnegie-Mellon. The Advanced Computer Tutoring Project at CMU currently has tutors under development for high-school algebra and geometry, and we have plans to create tutors for calculus and other programming languages such as Pascal and Prolog. The LISP tutor provides an example of our approach in bringing AI techniques into educational-software development.

INTELLIGENT TUTORING

These tutoring projects are examples of a particularly promising approach to educational software called *intelligent tutoring* (see reference 2). Such systems differ from other AI approaches to education by their attempt to provide effective instruction in problem solving the way a human tutor does.

There are a number of components typically found in an intelligent tutoring system. First, there is a *domain expert*, which can actually solve the problems. (GREATERP contains a system that can write LISP functions from problem specifications.) Second, there is a *bug catalog*, which contains all the possible deviations a particular student can make from the ideal expert behavior. Third, there is a *tutoring module*, which constitutes an expert system for instruction. It is based on three sets of principles: one for determining from a student's behavior what he knows and what confusions or *bugs* he has, another for deciding when to interrupt him in the problem-solving process and what to say, and a third to figure out what problems a student should do and when he should advance to new material. Typically, these decisions are based on an internal model that the tutor keeps of the student's knowledge and difficulties so far, enabling it to tailor its instruction to each individual student.

Finally, the tutoring system must contain an interface for communicating with the student. Its construction requires human-engineering decisions concerning how to present information understandably, how to query the student, how the student should enter answers, and what information should be maintained on the screen.

Until recently, intelligent tutoring was a topic for advanced research but didn't seem to offer a viable method for delivering educational software. This situation has changed for two reasons. First, an increasing expertise in cognitive psychology and artificial intelligence allows us to build such tutors much more efficiently and rapidly. For example, we can develop lesson material on our LISP tutor at a faster rate than that estimated for conventional educational software (200 hours per hour of instruction). Second, while an intelligent tutor requires a larger, faster computer, hardware costs are dropping to where it is becoming cost-effective to purchase the equipment required.

DESIGN OF THE LISP TUTOR

The goal underlying our design of the LISP tutor is simple: A student should be able to work on a problem in a "friendly" environment, as if he were using a smart, structured editor. However, whenever he makes a planning or coding error or asks for help, the tutor should provide helpful information that guides the student back to a correct path to the solution. In addition, we wanted our tutoring environment to represent the conceptual structure of programming problems better than a simple screen editor.

In order to monitor a student's progress and discover and instruct about errors, the tutor must be able to solve the problems the student is working on. Therefore, the first component in the LISP tutor is the *ideal model*, a simulation of the programming knowledge ideal students use in solving problems. This ideal model is based on a detailed theory of how students learn to program (see reference 3).

We used GRAPES (Goal-Restricted Production System, see reference 4) to represent the rules programmers have for solving problems. Each problem-solving rule is represented in the system as a production rule. Each production rule contains an IF part, which is a set of conditions used to determine if the rule applies, and a THEN part, which specifies what to do in that situation. The following are English versions of two of the hundreds of GRAPES production rules known by the tutor:

IF the goal is to combine LIST1 and LIST2 into a single list
THEN use the function APPEND and set as subgoals to code LIST1 and LIST2

IF the goal is to check that a recursive call to a function will terminate and the recursive call is in the context of a MAP function
THEN set as a subgoal to establish that the list provided to the MAP function will always become NIL after some number of recursive calls

The first is a straightforward production rule about the use of the LISP function APPEND to make one list from two other lists. The second is a rather esoteric production rule that an advanced programmer might have. When the ideal model codes a LISP function, it applies many production rules like these to plan and then write the code. It also contains a large set of *buggy* rules that represent misconceptions novice programmers often develop during learning.

The ideal model represents the knowledge we want the student to acquire. But the tutor must also represent what he currently knows or does not know and his approach to each particular problem. The tutor follows the student as he types in his code, symbol by symbol, and tries to figure out what correct or buggy production rule would have led to that input. If the rule found is a correct one, then the tutor stays silent and waits for further input. If, on the other hand, the input is in error, the tutor interrupts with advice. Thus, as long as the student follows a path leading to a correct solution, the tutor stays in the background.

(continued)

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Inquiry 165

The LISP tutor works through the algorithm step by step.

The LISP tutor is designed to provide as much guidance as necessary. When it finds that the student is having difficulty coding a problem, it takes him from "coding mode" into "planning mode"; that is, the tutor works through the algorithm with the student, step by step, using an example. After the algorithm is constructed, the student can return to coding, presumably with a better idea of what he should do to get his code to work properly.

We have designed this tutor with a strong commitment to immediate feedback. As soon as the student makes a mistake, the tutor responds with an appropriate diagnostic message. Because a student can write his code a small piece at a time, the feedback appears as soon as one item is wrong. By contrast, in the standard learning situation a student only receives feedback after he codes the entire function—or set of functions—and tries to run it. There is considerable psychological evidence that humans learn better with immediate feedback.

The tutor also provides guidance by hinting toward the correct solution if the student is having difficulty. These hints take the form of queries and reminders about current goals. If necessary, the tutor can provide the next small piece of code so that the student can continue. This is done at the student's request or after he has made more than the maximum number of allowed errors—usually two—for that portion of code. The goal here is for the student to do as much of the work as possible. Students learn much more effectively by doing than by watching. By providing the next portion of code, the tutor enables the student to work through the rest of the problem in cases where he might otherwise have given up. As a consequence, he can tackle more and more difficult problems.

A major design feature of the tutoring interface provides the student with a structured editor through which to enter code. This editor automatically balances parentheses and provides placeholders for the arguments of each function. For example, to write a function definition in LISP, you must use the function defun followed by the function name, a parameter list, and the function body. To begin, the student types a left parenthesis and the word defun. As soon as he types the space following that word, the tutor redisplays the code as

```
(defun <NAME> <PARAMETERS>
  <PROCESS>
  )
```

The symbols in angle brackets indicate arguments that must be coded. The tutor places the cursor underneath <NAME> and highlights it to indicate that the function name must be coded next.

This structured editor relieves students of the burden of balancing parentheses and checking syntax. It enables them to focus on the more conceptually difficult aspects of LISP. Our results show that this leads to faster learning of these major techniques and skills—with no deficit in syntax knowledge. Students removed from the tutor perform as well as or better on all aspects of coding, including algorithm design, memory for LISP functions, and syntax, than those conventionally taught.

The editor also facilitates communication between the student and the tutor. Our studies of interfaces have shown that in the normal question-and-answer format of most educational software, the tutor and the student can easily get "out of sync" on complex problems, where the student is not sure what part of the problem the tutor is talking about. In the LISP tutor, the student types directly into the code, replacing one of the placeholders, and thus it is always clear what part of the problem is being coded. Furthermore, these symbols help to communicate the conceptual structure of the programming problem. For example, when the student types the iterative construct prog, the tutor provides the template for iteration:

```
(prog <LOCAL VARIABLES>
  <INITIALIZATIONS>
  <BODY>
  <REPEAT>
  )
```

This template helps to structure the problem into a list of local variables, initializations of those variables, code for the program body (i.e., the repeated actions), and a return to the start of the loop. In many cases a symbol is expanded into more detailed symbols; for example, the <BODY> is coded as two portions: a <TERMINATING CASE> and the <UPDATING CODE>.

When an error arises or the student requests assistance, the tutor constructs an English explanation based on templates associated with each production rule. These explanation templates allow the tutor to describe an error or provide a hint by using a general rule *and* making reference to the specific problem being coded. However, writing programs to *understand* natural language is an enormously difficult and expensive task. In fact, students' descriptions of their algorithms are often hard for even human tutors to understand. Therefore, when the student is working with the tutor to design an algorithm, rather than having him type in English responses to the tutor's questions, we provide a menu of choices for his responses. This menu is constructed from the English descriptions of the correct and buggy production rules under consideration.

LEARNING LISP WITH THE TUTOR

Currently the LISP tutor contains approximately 325 production rules about planning and writing LISP programs and 475 buggy versions of those rules. It is effective in diagnosing and responding to between 45 and 80 percent of the student's errors, depending on the complexity of the

(continued)

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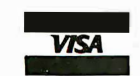
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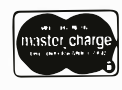
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Table 1: *The* LISP *curriculum.*

1. Basic LISP functions
2. Defining new function
3. Conditionals and predicates
4. Structured programming
5. Progs, input/output, and evaluation
6. Integer-based iteration
7. Integer-based recursion
8. List-based recursion
9. List-based iteration
10. Advanced recursion
11. Advanced programming constructs: Maps, Dos, Lets
12. Property lists and arrays
13. Search techniques
14. An advanced problem: Waterjug
15. List structure and destructive functions
16. Macros and advanced function types
17. Advanced topic: Pattern Matching
18. Advanced topic: Implementing Production Systems

Listing 1: *The dialogue between student and computer tutor to define the function* rightp.

Define **rightp**. It takes 3 arguments, **side1**, **side2**, and **side3**, which represent the lengths of the three sides of a given triangle, where **side3** is the longest side. **rightp** tests whether the three sides form a right triangle. In a right triangle, the sum of the squares of **side1** and **side2** is equal to the square of **side3**. However, your function should allow for a measurement error of 2 percent. In other words, your function should return **t** if the sum of the squares of the first two sides is within 2 percent of the square of the third side.

For example **(rightp 3 4 5.01)** = t, because 3 squared + 4 squared = 25, which is within 2 percent of 5.01 squared.

1. **(defun rightp (side1 side2 side3)** (cond))

   Yes, you could use **cond** here, but there is a much easier way to test if the sum of the squares of the first two sides is within 2 percent of the square of the third. You can use a predicate, since we only have one test to do.

2. (defun rightp (side1 side2 side3)
   (lessp (difference) <NUM2>))

   You want to code the amount of difference between the sum of the squares of the first two sides and the square of the third side, and you do *not* care which of those two numbers is larger. So we want to take the absolute value of their difference.

3. (defun rightp (side1 side2 side3)
   (lessp **(abs (difference** <NUM3> <NUM4>))
   <NUM2>))

   Which do you want to do first?
   PRESS: IF YOU WANT TO:
   1 Write code to get the sum of the squares of the first two sides.
   2 Write code to get the square of the third side.

   Menu choice: 1

4. (defun rightp (side1 side2 side3)
   (lessp (abs (difference **(plus)** <NUM4>))
   <NUM2>))

(continued)

Each lesson takes from one to four hours to complete.

lesson and the amount of testing we have conducted. The curriculum we have designed is shown in table 1. The system successfully tutors students through problems on lessons 1 to 10, each lesson taking from one to four hours to complete. Each topic involves a small instructional booklet and many problems practicing the skills taught in that lesson. Our goal in designing these booklets was to keep the written instruction to a minimum. There is considerable evidence that written technical instruction is most effective when it is brief (see reference 5).

Most of the time in any lesson is spent going through problems. Listings 1 and 2 illustrate sample dialogues in which the tutor monitors the student's progress through simple problems. This does not present the tutor as it really appears. Instead, it shows essentially *teletypewriter* versions of the student-tutor dialogue. The actual interaction involves the use of several display windows: a *code window* in which the student types the code, a *tutoring window* in which tutoring feedback is displayed, and a *goals window* in which reminders are presented.

In the teletypewriter versions the tutor's output is given in normal type characters, while the student's input is shown in bold characters. These listings present "snapshots" of the interaction; each time the student provokes a response, we have listed his input along with the tutor's response (numbered for convenience). The total code as it appears on the screen is shown, although the student has added only what is different from the previous code (shown in boldface type). For example, in line 2 of listing 1 he has typed **(lessp (difference** as an extension of the code in line 1.

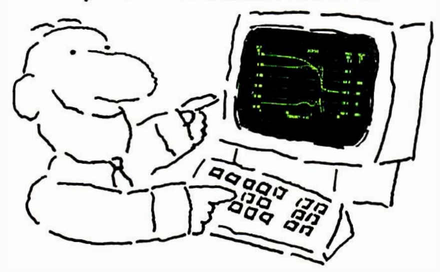
It is important to note several things

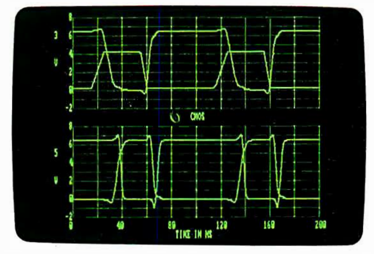
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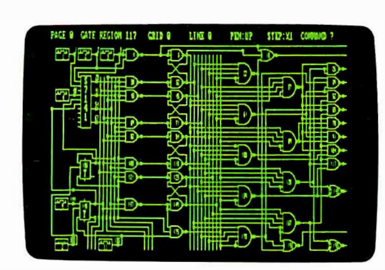








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Inquiry 361

No. You should create a helping function for this code, rather than coding it directly. Our function, **rightp**, is now 4 levels of embedding deep, and the relation we are about to code—the sum of squares of two numbers—would be a useful helping function. Thus, let's code the sum of the squares of the first two sides using a helping function.

5.
```
(defun rightp (side1 side2 side3)
  (lessp (abs (difference (sumsq <ARGUMENTS>) <NUM4>))
    <NUM2>))
```

What do you want the helping function **sumsq** to do?

PRESS: IF YOU WANT TO:

1 Take 2 arguments, the square of the first side and the square of the second side. Compute their sum.

2 Take 2 arguments, the first side and the second side. Compute the sum of the squares of these numbers.

3 Have the tutor choose.

Menu choice: 1

No. We wouldn't need a helping function *just* to compute the sum of two numbers. You should create your helping function so that it does more than just a sum.

It would be better to define **sumsq** so that it takes two arguments, in this case. [1] the first side, and [2] the second side, and computes the sum of the squares of these numbers.

Menu choice: **2**

6.
```
(defun rightp (side1 side2 side3)
  (lessp (abs (difference (sumsq side1 side2) (times)))
    <NUM2>))
```

You should use a helping function that you have already coded, **square**. Since this function computes the square of a number, you can use it to code the square of the third side.

7.
```
(defun rightp (side1 side2 side3)
  (lessp (abs (difference (sumsq side1 side2) (square side3))) (plus)))
```

I don't understand that, Rob. How are you going to code 2 percent of the square of the third side?

[EXPLAIN]

OK. I'll explain what I wanted. You could either code this directly or create a helping function here to code 2 percent of the square of the third side. Let's create a helping function just to make things easier. We'll call this helping function **percentage**. **We** will define **percentage** when we are finished coding **rightp**.

What do you want the helping function **percentage** to do?

PRESS: IF YOU WANT TO:

1 Take 2 arguments, one hundredth of 2 and the square of the third side. Compute their product.

2 Take 2 arguments, 2 and the third side. Compute the given percentage of the square of its second argument.

3 Take 2 arguments, 2 and the square of the third side. Compute the given percentage of its second argument.

4 Take 1 argument, the square of the third side. Compute 2 percent of its argument.

5 Have the tutor choose.

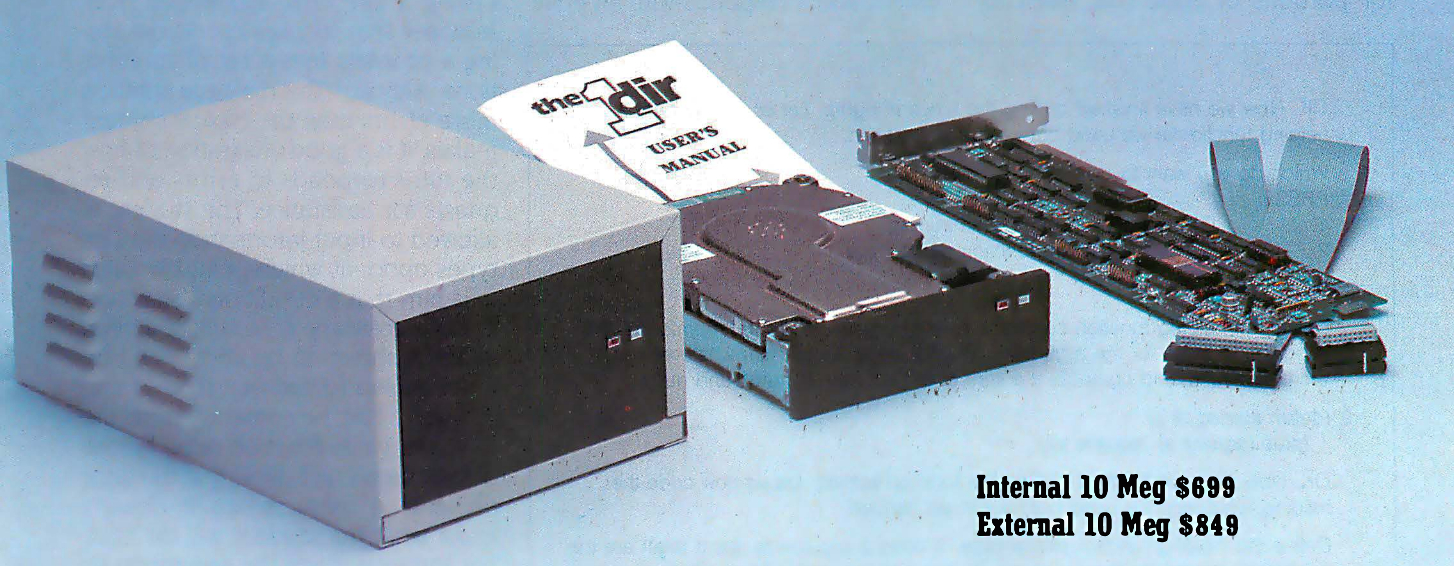
Menu choice: **3**

Very good.

8.
```
(defun rightp (side1 side2 side3)
  (lessp (abs (difference (sumsq side1 side2) (square side3)))
    (percentage 2 (square side3))))
```

(continued)

The Hard Disk With The Software Shell

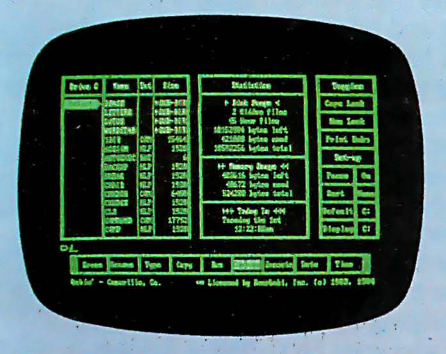


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Inquiry 327

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about these dialogues. First, recall that the tutor balances parentheses and provides placeholders (e.g., <CASE>, <NAME>, <NUM>) for portions of code that need expanding. Second, despite the large portions of code added from one line to the next, it understands each separate word or symbol the student enters, and it responds with an error message if necessary for any of those items.

```
    OK. Now we have finished coding the function rightp. Let us now code the
    helping function(s) we used but haven't yet defined.

    Which do you want to do first?
    PRESS:          IF YOU WANT TO:
    1               Define the helping function sumsq.
    2               Define the helping function percentage.

    Menu choice: 1

    Define the helping function sumsq. It takes 2 arguments. (num1 num2) are the
    suggested names for the arguments, but you may name them whatever you
    wish. sumsq should compute the sum of the squares of num1 and num2.

 9. (defun sumsq (s y)
      (plus (square s) (square y)))

    OK. Now we have finished coding the function sumsq. Let us now code the
    helping function(s) we used but haven't yet defined.

    Define the helping function percentage. It takes 2 arguments. (pcnt total) are the
    suggested names for these arguments, but you may name them whatever you
    wish. percentage should compute pcnt percent of total.

10. (defun percentage (x y)
      <PROCESS>

[EXPLAIN]

    OK. I'll explain what I wanted. Let's figure out how to code x percent of the
    second number.

    How can you code x percent of the second number?
    PRESS:          IF YOU WANT TO:
    1               Multiply the second number by one-hundredth of x.
    2               Multiply the second number by x.
    3               Divide the second number by 100.
    4               Have the tutor choose.

    Menu choice: 1

    Good.

11. (defun percentage (x y)
      (times <NUM1> <NUM2>))

    What do you want to do first?
    PRESS:          IF YOU WANT TO:
    1               Write code to get one-hundredth of the first number.
    2               Write code to get the second number.

    Menu choice: 1

12. (defun percentage (x y)
      (times (quotient x .01) <NUM2>))

    No, that is not the right number. How are you going to specify one hundred in
    LISP?

13. (defun percentage (x y)
      (times (quotient x 100) y))

    OK. Now we have finished coding the function percentage. There are no more
    helping functions to define.
```

THE rightp PROBLEM

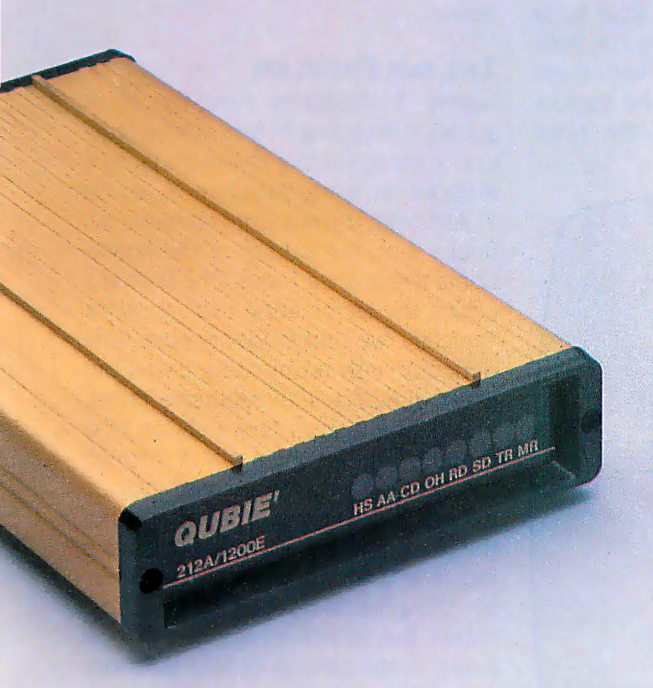
Listing 1 presents a dialogue from lesson 4 that focuses on decomposing a problem into a set of subfunctions. Although this dialogue contains more errors than the typical student makes, it is a good illustration of how the tutor responds to errors and requests for assistance. The student is allowed to input information until he types cond, at which point the tutor tells him that a conditional structure is not necessary. (The actual screen setup is shown in figure 1.) Next he types (lessp (difference (line 2) and receives a hint; he correctly inserts the absolute value function (abs) before difference in line 3. Note that the tutor presents a menu when it doesn't know what the student will do next. For instance, since the arguments to difference in rightp can be in either order, it needs to know which one will be typed next, and it asks him via the menu following line 3.

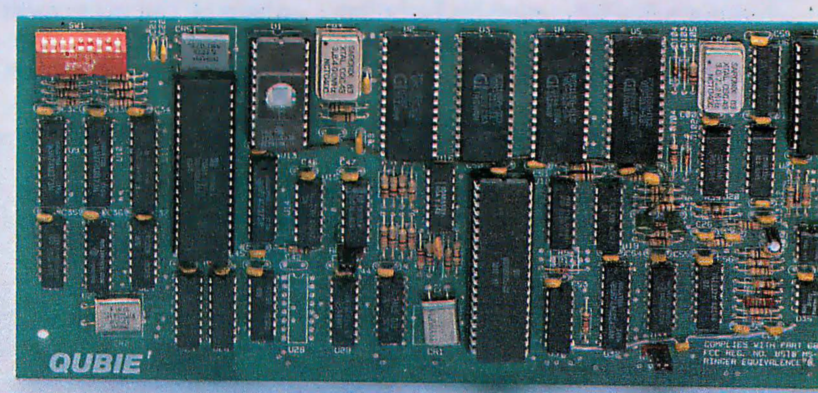
After line 4 the tutor gives the student information about when it is useful to code a separate helping function. It queries him after line 5 to make sure they agree on what that helping function will compute. This is an example of the tutor's planning mode. In this case, the student is mistaken about what the subfunction should do; the tutor corrects him. After line 7 it determines that his code will not achieve the goal. However, this input does not match any of the buggy rules in the ideal model, so the tutor provides minimal feedback: it indicates that it cannot understand the input and queries the student to remind him about what he should be trying to code. This hint is not enough for the student, who asks for an explanation by hitting a special key, whereupon the tutor helps him specify another helping function, percentage.

The final form of rightp is displayed in line 8. In line 9 the student defines the helping function sumsq without error and goes on to define percent-

(continued)

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age in line 10. He is stuck as to what to do after typing the function body and requests an explanation. The tutor helps him refine his algorithm. After this he defines percentage with one error in line 12.

After the student defines rightp and its helping functions, the LISP tutor puts him into a real LISP environment where he can experiment with them and try variations. After he experiments to his satisfaction, the tutor provides the next problem in the lesson.

```
Yes, you could use COND here, but there is a much easier
way to test if the sum of the squares of the first two sides
is within 2% of the square of the third. You can use a
predicate, since we only have one test to do.

                        CODE FOR rightp

(defun rightp (side1 side2 side3)
    (cond )
    )

                           GOALS

Define the function rightp.  (rightp 3 4 5.01) = t.
*** Test if the triangle is a right triangle. ***
```

Figure 1: *The screen configuration after line 1 in listing 1.*

```
In examples A and B what do you have to do to get the result
of fact called with n?
PRESS:              IF YOU WANT TO:
1.      Multiply n by one less than n.
2.      Multiply n by fact of one less than n.
3.      Add n to the result of fact called with one less than n.
4.      Have the tutor choose.
Menu Choice: 2
                        CODE FOR fact
(defun fact (n)
    (cond ((zerop n) 1)
          <RECURSIVE-CASE>))

                          EXAMPLES
        fact (n)          fact (n-1)
A.   (fact 1) = 1      (fact 0) = 1
B.   (fact 3) = 6      (fact 2) = 2
```

Figure 2: *The screen configuration before line 4 in listing 2.*

THE fact PROBLEM

Listing 2 illustrates how the tutor guides the coding of a recursive function such as finding the factorial of a number, an early problem in lesson 7. Although the student has some difficulty with the syntax of the conditional test in lines 1 and 2, he basically codes the terminating test correctly. Typically, we find students have little difficulty with terminating cases but great difficulty with recursive cases. The dialogue after line 3 shows how the tutor guides the student through the design of the recursive function. It leads him to construct examples of the relationship between fact (n) and fact (n – 1) and then asks him to identify the general relationship. Figure 2 shows the screen image at a critical point in the design of this function.

The dialogue after this point shows two classic errors students make in defining recursive functions. The first in line 4 is to call the function directly without combining the recursive call with other elements. The second, in line 6, is to call the function recursively with the same argument rather than a simpler one.

After the student finishes coding the function, he goes to the LISP window and experiments with it. He must trace the function and the recursive calls embed and unravel. Figure 3 shows the screen image at this point, with the code on top and the trace below it.

EVALUATING THE LISP TUTOR

We should emphasize that the tutorial knowledge in these interactions was not especially handcrafted for these problems; it shows the general approach used by the tutor. That is the power of an intelligent tutoring system. Once we have a system that can tutor recursion problems, for example, we can easily add problems on that topic. Furthermore, although some testing is necessary to build our catalog of student errors and misconceptions, once coded, the tutor can

(continued)

```
--- YOU ARE DONE.  TYPE NEXT TO GO ON AFTER ---
--- TESTING THE FUNCTIONS YOU HAVE DEFINED  ---

(defun fact (n)
    (cond ((zerop n) 1)
          (t (times n (fact (sub1 n))))))

                 THE LISP WINDOW

=> (trace fact)
(fact)

=> (fact 3)
1 <Enter> fact (3)
|2 <Enter> fact (2)
| 3 <Enter> fact (1)
| |4 <Enter> fact (0)
| |4 <EXIT>  fact  1
| 3 <EXIT>  fact  1
|2 <EXIT>  fact  2
1 <EXIT>  fact  6
6
```

Figure 3: *The screen configuration at the end of the dialogue in listing 2.*

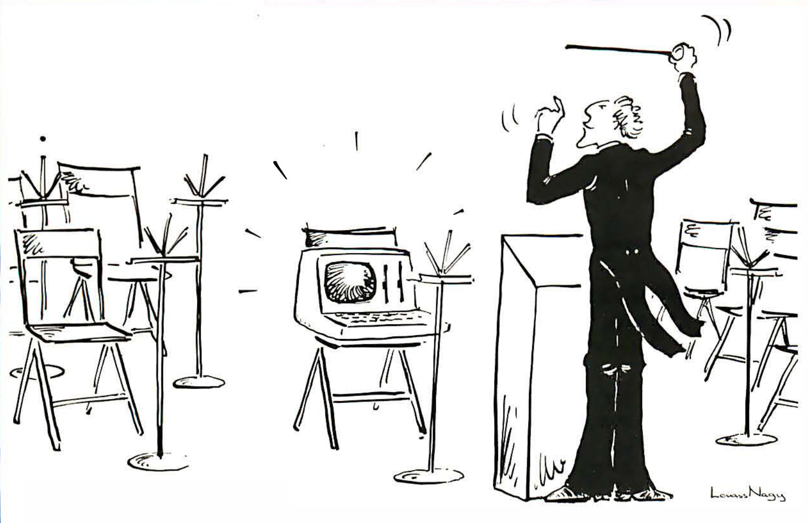
lead students through a variety of correct solutions and respond to a wide range of errors. Thus, it is generative in the sense that it creates instructional interactions rather than using preprogrammed sequences.

Generally, students are happy with the tutor and rate it better than learning experiences they have had in other introductory programming courses. Their major complaints are that it uses too many menus and is sometimes slow. We are implementing optimizations and improvements to resolve both these problems. Interestingly, students are more appreciative of the tutor's guidance and more tolerant of its speed as the lessons increase in difficulty.

We have run one evaluation of the tutor, comparing it to experienced private human tutors and "on-your-own" condition. We found that the advantage of private tutoring—human or computer—over the on-your-own condition increased as the material became more difficult. The students finished lesson 1 basically with the same speed and success in all three conditions. However, those in the on-your-own condition often had great difficulty getting through the recursion material; in fact, some did not finish the material in the allotted time. We had to extrapolate how long it would have taken them to finish it. Averaging the actual and extrapolated times, the students took 11.4 hours with the human tutors, 15 hours with the computer tutor, and 26.5 hours "on-your-own" to learn six lessons. Polls of students in a traditional classroom suggest that it takes over 40 hours to cover the material in that situation.

We tested the three groups just before the recursion exercises. We found essentially identical performances even though they were learning at different rates. In another evaluation, we found students working with the tutor learned nine lessons of material faster and performed better on competence tests than students learning without the tutor. Thus, the basic conclusion is that the human

(continued)



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Listing 2: *The dialogue involved in defining the function* fact, *which computes the factorial of the number given.*

Define the function **fact**. It takes a number argument, **n**, and computes the factorial of **n**, which is the result of multiplying **n** × n−**1** × **n**−**2** . . . × 1. For instance, (**fact 3**) = **3** × **2** × **1** = **6**. By definition, the factorial of 0 is 1.

1. (**defun fact (n)**
   (**cond ((equal)** <ACTION>)
   <RECURSIVECASE>))

   I assume that you are trying to test if the number argument is equal to the number zero. There is a special function for testing equivalence to zero. Try to use that function instead of **equal**.

   What code can you write to test if the condition for terminating case is true? Try writing a predicate.

2. (defun fact (n)
   (cond ((**zero** <ACTION>)
   <RECURSIVECASE>))

   Did you mean zerop (y or n)? **y**

3. (defun fact (n)
   (cond ((**zerop** n) **1**)
   <RECURSIVECASE>))

   Is the value of **fact** in the recursive cases calculated by:

PRESS:	IF YOU WANT TO:
1	Calling **fact** recursively with **n**.
2	Multiplying **n** by **fact** of **n** minus 1.
3	Getting **1 2** . . . **n** and then multiplying the results.
4	Have the tutor choose.

   Menu choice: **3**

   That is a reasonable way to think of doing factorials but it is not a plan for a recursive function. Since you seem to be having trouble with the recursive cases let us work through some examples and figure out the conditions and actions for each of these cases.

   The recursive relationship is the relationship between **fact** called with **n** and **fact** called with:

PRESS:	IF YOU WANT TO:
1	n minus 1
2	n equal to 0
3	n plus 1
4	Have the tutor choose.

   Menu choice: 1

   We will consider some concrete examples. We will characterize the recursive relationship between **fact** called with 1 and **fact** called with 0.

   What is the value of (**fact 1**)?
   Answer: **1**

   What is the value of (**fact 0**)?
   Answer: 1

   EXAMPLES

	fact (n)	fact (n − 1)
A.	(fact 1) = 1	(fact 0) = 1

   We will consider some more concrete examples. We will characterize the recursive relationship between **fact** called with 3 and **fact** called with 2.

   What is the value of (**fact 3**)?
   Answer: **6**

(continued)

What is the value of (fact 2)?
Answer: 2

EXAMPLES

	fact (n)	fact (n − 1)
A.	(fact 1) = 1	(fact 0) = 1
B.	(fact 3) = 6	(fact 2) = 2

Since there is only one recursive case characterized by the examples you have just worked out, the condition in this case can be just coded as T. We will focus on characterizing the action in this case.

In examples A and B what do you have to do to get the result of **fact** called with **n**?

PRESS:	IF YOU WANT TO:
1	Multiply **n** by one less than **n**.
2	Multiply **n** by **fact** of one less than **n**.
3	Add **n** to the result of **fact** called with one less than **n**.
4	Have the tutor choose.

Menu choice: **2**

We have now worked through a series of examples that illustrate the recursive relation. We will now return to the goal of trying to produce LISP code that specifies the recursive relation.

4.
```
(defun fact (n)
  (cond ((zerop n) 1)
    (t (fact )))
```

You will have to use **fact** at some point but right now you want to multiply.

5.
```
(defun fact (n)
  (cond ((zerop n) 1)
    (t (times <NUM> <NUM2>))))
```

What do you want to do first?

PRESS:	IF YOU WANT TO:
1	Write code to get the number argument.
2	Write code to get the recursive part.

Menu choice: 1

6.
```
(defun fact (n)
  (cond ((zerop n) 1)
    (t (times n (fact n)))))
```

You cannot just code **n** at this point. What you want to do is subtract one from **n**.

7.
```
(defun fact (n)
  (cond ((zerop n) 1)
    (t (times n (fact (difference ))))))
```

difference would work in this case but it is more appropriate to use the function **sub1** when you are subtracting 1 from a number.

8.
```
(defun fact (n)
  (cond ((zerop n) 1)
    (t (times n (fact (sub1 n))))))
```

tutor is still best, the computer tutor not that far behind (and constantly improving), and the traditional on-your-own condition much worse.

TODAY AND TOMORROW

Currently, we get satisfactory performance of the tutor on a VAX 725 with 3 megabytes of memory devoted to a single student. Our planned optimizations should enable it to handle a pair of students simultaneously running on the same machine. These implementations are cost-effective in expensive private schools like CMU or in industry; however, they are clearly out of range for the general public. The amount of computational power required is considerable. Even in future, more efficient implementations we estimate a minimum of 1 megabyte of memory will be necessary to tutor one student on one machine. By the late 1980s the computational power to deliver such instruction should be more generally available. For instance, in conjunction with IBM, CMU is planning to have on campus by 1986 a personal computer with 1 megabyte of memory capable of 1 million instructions per second. Such a machine will be more than adequate to implement the LISP tutor.

These technological trends encourage optimism about the future of intelligent tutoring efforts, of which the LISP tutor is one. We hope that, with continued research in domains such as high-school mathematics and college-level programming, we will soon establish the conceptual foundations to use the computational power that will be available. The prospect is great of providing every student with the educational benefits of a private human tutor. When this happens, the consequences for American education will be nothing short of revolutionary. ■

ACKNOWLEDGMENT

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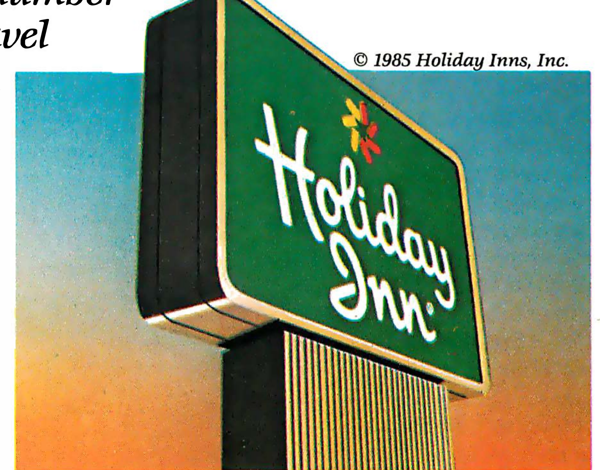


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PROUST

BY W. LEWIS JOHNSON AND ELLIOT SOLOWAY

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PROUST (Program Understander for Students) is a knowledge-based system that finds nonsyntactic bugs in Pascal programs written by novice programmers. When students compile a program successfully, PROUST is automatically invoked to analyze it. PROUST reports any bugs that are in the program to the student.

PROUST is not merely a tool that helps programmers find bugs, nor is it confined to a narrow class of bugs, such as uninitialized variables. It is designed to find *every* bug in most beginners' programs. PROUST is currently capable of correctly identifying all of the bugs in over 70 percent of the programs that students write when we assign them moderately complex programming problems. When PROUST finds a bug, it does not simply point to the lines of code that are wrong; instead, it determines how the bug can be corrected and suggests why the bug arose in the first place. Our aim is to build an instructional system around PROUST that assigns programming problems to students, reads their work, and gives them helpful suggestions.

In designing PROUST we found it necessary to deal directly with the variability of bugs in beginners' programs. If a programming problem is assigned to a class of 200, the students will write 200 different programs (assuming that they do not cheat). There is variability both in their programs' designs and bugs. Some bugs, such as missing variable initializations, are accidental omissions that can be easily recognized and corrected. Other bugs result when the programmer fails to reason through the interactions between components. In isolation, each piece of the program may appear correct, but when combined, the program doesn't work. Still other bugs result from misconceptions about programming. The code may appear correct to the programmer, but it doesn't do what he or she expects, for reasons he or she does not understand. Bugs resulting from misconceptions are the most serious; students stand to benefit the most from having such problems pointed out to them.

If a debugging system is to cope with the various types of errors that programmers make, it must understand what the programmer is trying to do. Debugging systems usually don't concern themselves with what the program is supposed to do, they only analyze what the program actually does (see references 1, 2, and 3). Figuring out how a program is supposed to work is not easy; to do it a debugger requires information about the programming problem and knowledge about how to write programs. Nevertheless, identifying the programmer's intentions is worth the effort, because this knowledge makes it possible to identify more bugs, as well as to understand their causes.

To show how knowledge of the pro-

(continued)

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grammer's intentions assists debugging, we will present two examples of "buggy" programs and discuss why alternative approaches to automatic debugging fail to identify such bugs. Then we will describe how PROUST analyzes such programs. Finally, we will present some statistics showing PROUST's performance on large numbers of students' solutions to a typical assignment in an introductory programming class. This will help support our claim that PROUST's approach is adequate for the majority of novice programmers' programs.

EXAMPLES OF PROGRAM BUGS

Here is a simple programming problem called the Averaging Problem:

> Write a program that reads in a sequence of positive numbers, stopping when 99999 is read. Compute the average of these numbers. Do not include the 99999 in the average. Be sure to reject any input that is not positive.

The student's program must compute the average of a series of positive numbers. It must ensure that the input to the program is in fact positive. The input terminates when a specific value—99999—is read. Values such as this, which signal the end of input, are called *sentinel values.*

Figure 1a shows a sample solution to the Averaging Problem. This program works except for the following bug: if you type 99999 immediately after typing a nonpositive value, the program will continue to prompt for data after the 99999 is read. When the program finally does terminate, the average will be incorrect. For example, suppose that you input 5, −5, 99999. Instead of terminating when the 99999 is read, the program requests another input. If the user then entered another 99999, the program would not print the average as 5, but instead would print (5+99999)/2, or 50002.

The program interprets 99999 as data when the sequence 5, −5, 99999 is read because when the program reads the −5, it enters the input-validation loop, which starts with line 10, WHILE Val <= 0 DO. This loop is intended to iterate until a positive value is typed in; 99999 is positive, so when the 99999 is read, control leaves the input-validation loop. However, the program was written with the assumption that when the input-validation loop is exited, the current value of Val is valid input data. In this case, Val is not valid data; it is 99999, the sentinel value. The loop nevertheless processes 99999 as if it were data. To guard against this case, there should be a test for the sentinel after the input-validation loop.

Figure 1b is PROUST's output describing the missing sentinel-test bug. The error is described in two ways: First it is described in English; then PROUST generates an example of data that causes the program to fail.

Now look at the program in figure 2a. This is another solution to the Averaging Problem, and the bug in this program is also fairly obscure. If you type a positive value followed by a negative value, the negative value will be included in the average. Thus if you type −2, 2, 99999, the average will be 2, but if you type 2, −2, 99999, the average will be 0.

Unlike the example in listing 1a, the programmer has not left out the sentinel test but has written the test in the form of a WHILE statement instead of an IF statement. The student probably has a misconception about the distinction between the two state-

(a)

```
 1  PROGRAM Average( Input, Output );
 2    VAR Sum, Count, Val, Avg: REAL;
 3    BEGIN
 4      Sum := 0;
 5      Count := 0;
 6      Writeln( 'Enter Value:' );
 7      Read( Val );
 8      WHILE Val< >99999 DO
 9        BEGIN
10          WHILE Val<=0 DO
11            BEGIN
12              Writeln( 'Invalid entry, reenter' );
13              Read( Val );
14            END;
15          Sum := Sum+Val;
16          Count := Count+1;
17          Writeln( 'Enter value:' );
18          Read( Val );
19        END;
20      IF Count>0 THEN
21          Writeln( 'No data entered' )
22        ELSE BEGIN
23          Avg := Sum/Count;
24          Writeln( 'The average is,'Avg );
25        END;
26      END.
```

(b)

PROUST's output:

You're missing a sentinel test. If a sentinel value is input immediately following a nonpositive value, your program will treat it as valid data.

To see this, try the following data in your program:
5 −5 99999

Figure 1: *(a) One novice programmer's attempt at implementing the Averaging Problem. (b)* PROUST *explains the bug lurking in the program in concise English sentences and even offers data illustrating the error.*

ments and does not understand how the control flow in a WHILE loop works. As long as the body of the loop is straight-line code, the student has no problem. However, if the body of the loop contains tests, the student thinks that the tests should be written as WHILE statements to ensure that they repeat when the body of the loop does. We will refer to this misconception henceforth as the WHILE-for-IF misconception. PROUST's output for this example, shown in figure 2b, takes the misconception into account and explains it to the student.

The bugs in figures 1a and 2a illustrate the following points. First, bugs frequently cannot be detected if you don't know what the program is supposed to do. Both of the programs shown run no matter what input is read; to determine that there is a bug, you must recognize that the programs output different results than they should. Bugs such as these are not unusual; the missing sentinel-test bug occurs in 18 percent of novice programmers' solutions to the Averaging Problem.

Second, novice programmers need help identifying such bugs. These bugs cause the programs to fail only after unusual inputs—ones that novice programmers are unlikely to test. In the case of the WHILE-for-IF misconception, even if the programmer tests the case in question, he or she will probably not understand why the program fails because he or she expects the WHILE statement to perform a different function than it actually does.

(a)

```
 1  PROGRAM Average( Input, Output );
 2    VAR Sum, Count, Val, Avg: REAL;
 3    BEGIN
 4      Sum := 0;
 5      Count := 0;
 6      Writeln( 'Enter value:' );
 7      Read( Val );
 8      WHILE Val<>99999 DO
 9        BEGIN
10          WHILE Val<=0 DO
11            BEGIN
12              Writeln( 'Invalid entry, reenter' );
13              Read( Val );
14            END;
15          WHILE Val<>99999 DO
16            BEGIN
17              Sum := Sum+Val;
18              Count := Count+1;
19              Writeln( 'Enter value:' );
20              Read( Val );
21            END;
22        END;
23      IF Count=0 then
24          Writeln( 'No data entered' )
25        ELSE BEGIN
26          Avg := Sum/Count;
27          Writeln( 'The average is',Avg );
28        END;
29    END.
```

(b)

PROUST's output:

You are using a WHILE statement at line 15 where you should have used an IF statement. You probably want the code starting at line 15 to execute once each time through the loop; your code will make it execute many times.

The statement in question is:
WHILE Val<>99999 DO . . .

Figure 2: *(a) Another novice programmer's attempt at implementing the Averaging Problem. (b)* PROUST *once again explains what the problem with the program is, what the programmer wanted to do, and what he actually did.*

Alternatives to Intention-Based Debugging

To support our claim that debugging requires knowledge of the programmer's intentions, we will examine the principal alternatives to intention-based debugging and show why they fall short. The methods we have considered are analysis of I/O (input/output) behavior, analysis of data flow, and recognition of patterns of buggy code.

Debugging by analyzing I/O behavior involves determining when the output of the program is incorrect and suggesting bugs that might have caused the faulty behavior (see reference 2). This approach treats debugging as similar to medical diagnosis (see reference 4). The faulty behavior can be thought of as the symptoms of the program, and the bugs can be thought of as the diseases. There are two problems with this approach: A program's symptoms cannot always be determined, and these symptoms cannot always be related to the bugs. The bugs in the programs in figures 1a and 2a affect the output of the program only occasionally; recognizing when this happens requires knowledge about what the output should look like. Since the WHILE-for-IF example fails to test the input for validity after the first positive value is read, it appears that this program is missing an input-validation test. It is only after inspecting the code that it becomes clear that the bug is not in the input-validation test but in the sentinel test.

Another debugging approach you might try is data-flow analysis (see reference 1). This is the approach many error-checking compilers use.

(continued)

Data-flow analysis checks for clear anomalies in the pattern of data definition and for use of data in a program. It can determine when a variable is defined and never used or when a variable is never defined. However, if there are no anomalies in data flow, data-flow analysis will not detect any bugs. Neither example in the preceding section has data-flow anomalies, so this method would not detect the bugs.

You might also try analyzing the structure of the program itself to see whether it suggests the presence of bugs. You could build a library of templates for common bugs, such as missing sentinel tests or WHILE statements in place of IF statements, and then match these templates against the program to identify the bugs. The problem with this approach is that you have no way of knowing where to match the bug templates in the program. For example, the WHILE-for-IF example has three different WHILE loops. How could you tell which WHILE loop really should be an IF statement or if any of them should be an IF statement? You could try to make the bug template more specific by making it apply only when there are two loops with the same exit test, one inside the other. But that would make the template too specific; it would not apply to other cases where WHILE statements appear instead of IF statements.

All of these approaches to debugging attempt to identify bugs without any understanding of what the program is supposed to do, and any such approach does little more than make guesses as to what bug is involved. In order to do better, a debugging system has to be able to infer the programmer's intentions and relate them to the code.

PROUST's Approach

PROUST is written in T, a dialect of LISP. The full system contains roughly 15,000 lines of LISP code and runs on a VAX-11/750. A stripped-down version called Micro-PROUST has been developed in conjunction with Courseware Inc., of San Diego, California (see the text box "Micro-PROUST for the IBM PC" above for more information). Micro-PROUST is capable of recognizing the kinds of bugs that are described in this article; however, there are a variety of tricky bugs that PROUST can identify but Micro-PROUST cannot. (If you are interested in PROUST's full diagnostic capabilities, consult reference 3.)

PROUST's analysis of programs is based on knowledge of the programming problem. Students may solve the problem in a variety of ways and their programs may have a variety of bugs, but they are all trying to solve the same problem. Knowledge of the problem makes the variability of novice solutions more manageable. It also provides important information about the programmer's intentions.

To provide PROUST with descriptions of the programming problems, we devised a problem-description language. We described each problem in this language and provided PROUST with a library of the descriptions. Each problem description in PROUST's problem-description language is a paraphrase of the English-language problem statement that we hand out to students.

To understand the students' programs, PROUST also needs to know how to solve the problem. Solutions to a given programming problem may be implemented in a variety of different ways. Suppose that there was only one way to test input for validity in a Pascal program, namely, to insert a WHILE loop at the top of the main loop, such as in figures 1a and 2a. Once PROUST knew that a program must validate input, it would know to look for such a loop, as well as for the sentinel test that must follow. However, there are several ways of validating input. Listing 1 shows a loop that tests input in a different way. Instead of there being one input validation loop, there are two; one is at the bottom of the loop and the other precedes the loop. No additional sentinel test is required when this method is used, because, as soon as input is validated, control flows to the main exit test of the WHILE loop. Therefore, without knowing what method the programmer is using for validating input, PROUST cannot tell whether to look for a sentinel test within the body of the loop. In figure 1a it is an error not to have such a sentinel test, but in listing 1 it is not. PROUST needs knowledge about programming so that it can understand how each student designed and implemented his or her solution. Once it understands the programmer's intentions, it can then use knowledge about common bugs to identify them in the student's program.

PROUST analyzes programs by synthesis. When PROUST examines a program, it looks up the corresponding problem description in its library. It makes hypotheses about the methods programmers may use to satisfy each requirement in the problem description. Each hypothesis is a possible correct implementation of the corresponding requirement. If one of these hypotheses fits the student's code, then PROUST infers that the requirement is implemented correctly. If PROUST's hypotheses do not fit the student's program, then PROUST checks its database of com-

Micro-PROUST for the IBM PC

Micro-PROUST is a subset of the larger implementation of PROUST. It is capable of dealing with a limited range of novice programs and is currently set up to handle only those example solutions to the Averaging and Rainfall Problems provided with it. Micro-PROUST runs in Gold Hill Computers Inc. Golden Common LISP on an IBM Personal Computer with 512K bytes of memory. The source code and example programs are available for downloading from BYTEnet Listings. The telephone number is (603) 924-9820. The file PRSTREAD.ME contains directions on how to run Micro-PROUST.

mon bugs to see if it can explain the discrepancies.

PROUST's Problem Descriptions

Problem descriptions in PROUST consist of programming goals and sets of data objects. Programming goals are the principal requirements that must be satisfied; sets of data objects are the data that the program must manipulate.

The first step in translating an English-language problem statement into PROUST's problem-description language is to make the various goals that are mentioned in the problem statement explicit. Recall that the text of the Averaging Problem is the following:

> Write a program that reads in a sequence of positive numbers, stopping when 99999 is read. Compute the average of these numbers. Do not include the 99999 in the average. Be sure to reject any input that is not positive.

Solutions to this problem operate on a sequence of input data; let us call this sequence New. The following goals can be extracted from the problem statement:

- Read successive values of New, stopping when a sentinel value, 99999, is read.
- Make sure that the condition New <= 0 is never true.
- Compute the average of New.
- Output the average of New.

We must now take these goals and use them to generate a problem description for PROUST. Each data object that the goals refer to is named and declared. Each goal extracted from the problem statement is recorded in the problem description. The resulting problem description is shown in figure 3.

Like all the data structures that we discuss in this article, problem descriptions are in list notation and every statement and expression is enclosed in parentheses. The name of the program is indicated with a Define-Program statement. Objects are named using Define-Object statements. Goals are indicated using Define-Goal statements.

Listing 1: *Yet another way to implement the input validation for the Averaging Problem.*

```
Read( Val );
WHILE Val<=0 DO
  BEGIN
    Writeln( 'Invalid entry, reenter' );
    Read( Val );
  END;
WHILE Val<>99999 DO
  BEGIN
    Sum := Sum+Val;
    Count := Count+1;
    Writeln( 'Enter value:' );
    Read(. Val );
    WHILE Val<=0 DO
      BEGIN
        Writeln( 'Invalid entry, reenter' );
        Read( Val );
      END;
  END;
```

Object names are preceded by question marks. There are two objects defined in the Averaging Problem description, ?Sentinel and ?New. The question-mark notation is used frequently in artificial-intelligence (AI) programs; it indicates that the variable is not a literal value but is a parameter that must be substituted when the data structure is used. For example, the input-data object ?New will be substituted with the name of the Pascal variable that the student uses for storing the input data. The object ?Sentinel has the value 99999; wherever ?Sentinel appears in the problem description it can be substituted with 99999.

Objects can be either constant-valued or variable-valued. In this example, ?Sentinel is a constant, with the value 99999, and ?New is a variable. In PROUST's general problem-description language objects can have a variety of properties associated with them; however, we will not use any such properties in this simple example.

Goal statements consist of a name of a type of goal, followed by a list of arguments. In the form (Average ?New) for example, Average is a type of goal (to compute an average), and ?New is the argument of the goal. This form requires that the program compute the average of ?New.

Arguments to goal expressions can take a variety of forms. They can be objects, predicates, or even other goal expressions. In the expression (Input-Validation ?New (<= ?New 0)), one argument is an object (?New), and the other is a predicate ?New <= 0. In LISP, function names and operators precede their arguments, which is why the <= precedes the ?New and 0 in the expression (<= 0). If goals are nested, as in (Output (Average ?New)), the outer goal refers to the value computed by the inner goal. Thus this goal requires that the program output the average of ?New.

In this example PROUST's problem descriptions are a reasonable approximation of the original English-language problem statements. These problem descriptions describe what the programs must do but not how they are supposed to do it. PROUST must analyze each individual program and determine how it is intended to satisfy the problem requirements.

Programming Knowledge

Programming knowledge in PROUST is frame-based (see reference 5). In frame-based systems knowledge is organized into frames, each of which corresponds to a particular concept that the system "knows" about. Frames are similar to records in relational databases, although the operations that can be performed on frames are somewhat different. Knowledge in frames is organized into slots, which function as record field names, and fillers, which are the values assigned to each slot.

The two kinds of programming knowledge that we will consider here are goals and plans (other types of programming knowledge are discussed in reference 6). Goals are problem requirements that appear in

(continued)

problem descriptions. Plans are stereotypic methods for implementing goals. A large part of writing programs consists of identifying goals that must be satisfied and selecting plans to implement these goals. Similarly, PROUST retrieves plans from its knowledge base for each goal referred to in the problem description. It compares these plans to the student's program to determine which fits the program best.

Figure 4 shows PROUST's definition for the Sentinel-Controlled-Input goal. The goal definition contains a series of slots: InstanceOf, Form, MainSegment, etc., together with fillers for each of these slots: Read&Process, MainLoop:, ?New, etc. These slots serve various functions, only some of which we will discuss here. The most important slots are the Instances and InstanceOf slots. The Instances slot lists the various plans in PROUST's knowledge base for implementing this goal. This slot's filler is a list of five items, each of which is the name of a plan. The InstanceOf slot indicates the class to which this goal belongs. The goal class in this case is Read&Process, which is the class of all goals that involve reading a sequence of values and processing them.

Figure 5 shows a plan, the Sentinel-Process-Read-While plan. This is one of the instances of the Sentinel-Controlled-Input goal. This plan is a simplified version of the one PROUST actually uses. Plans are also defined in terms of slots and fillers. The most important slot is the Template slot, which describes the form the Pascal code implementing this plan should take. Plan templates consist of Pascal statements, subgoals, and labels. The Pascal statements are written in list notation rather than ordinary Pascal syntax; for example, the form (WHILE (< > ?Input ?Stop) . . .) in Pascal syntax would appear as WHILE ?Input < > ?Stop DO . . . . Symbols that are preceded by question marks are pattern variables; these are substituted when the plan is used. ?New is substituted by a Pascal variable containing the input data, and ?Stop is substituted by a constant, the sentinel value. The ?* statement is a "wild card" pattern that can be substituted by an arbitrary sequence of Pascal statements; this is just a placeholder in the plan. Subgoals are indicated by (SUBGOAL . . .) forms in the template; these are goals that must in turn be implemented using other plans.

Matching Plans

Let's look at how plans and goals are used to understand a program. The plan in listing 1 has been implemented correctly. You will see how PROUST hypothesizes a plan that the program might use and then matches this plan against the program. In this case the match succeeds because the plan is implemented correctly. In the next section we will examine what happens when plans fail to match because the student's code has bugs.

The first step, before any analysis of goals and plans takes place, is to parse the student's Pascal program. This results in a parse tree. All subsequent analysis of the program is performed on the parse tree rather than on the original program text.

When PROUST analyzes a program, it selects goals from the problem description one at a time. Let's suppose that the goal that is selected first is (Sentinel-Controlled-Input ?New ?Sentinel). PROUST substitutes any

(continued)

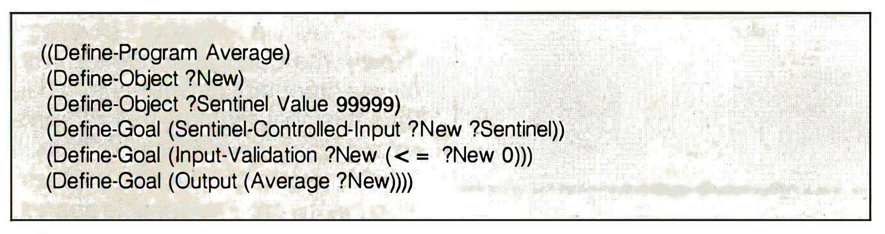

```
((Define-Program Average)
 (Define-Object ?New)
 (Define-Object ?Sentinel Value 99999)
 (Define-Goal (Sentinel-Controlled-Input ?New ?Sentinel))
 (Define-Goal (Input-Validation ?New (< = ?New 0)))
 (Define-Goal (Output (Average ?New))))
```

Figure 3: *The Averaging Problem translated into* PROUST*'s problem-description language.*

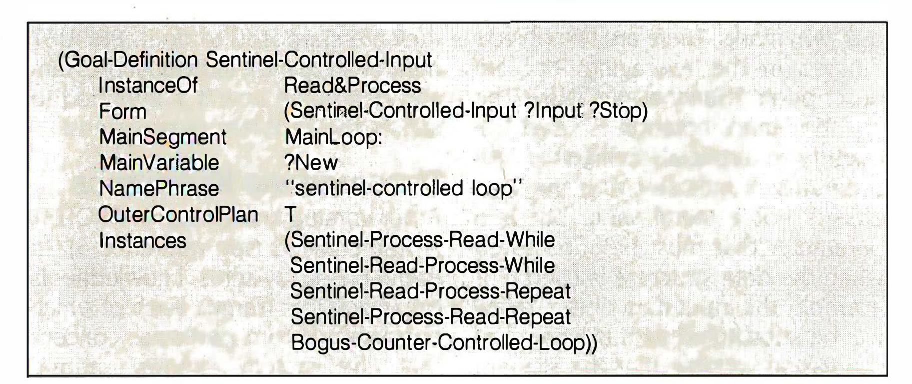

```
(Goal-Definition Sentinel-Controlled-Input
    InstanceOf          Read&Process
    Form                (Sentinel-Controlled-Input ?Input ?Stop)
    MainSegment         MainLoop:
    MainVariable        ?New
    NamePhrase          "sentinel-controlled loop"
    OuterControlPlan    T
    Instances           (Sentinel-Process-Read-While
                         Sentinel-Read-Process-While
                         Sentinel-Read-Process-Repeat
                         Sentinel-Process-Read-Repeat
                         Bogus-Counter-Controlled-Loop))
```

Figure 4: *The definition of the goal* Sentinel-Controlled-Input *in* PROUST*'s problem-description language.*

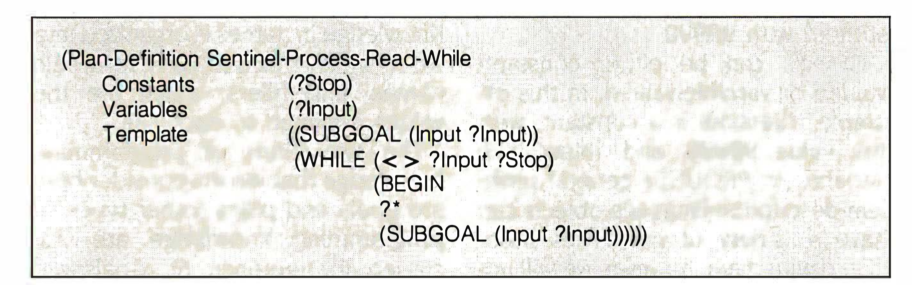

```
(Plan-Definition Sentinel-Process-Read-While
    Constants       (?Stop)
    Variables       (?Input)
    Template        ((SUBGOAL (Input ?Input))
                     (WHILE (< > ?Input ?Stop)
                            (BEGIN
                             ?*
                             (SUBGOAL (Input ?Input)))))
```

Figure 5: *A plan for implementing the goal* Sentinel-Controlled-Input.



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Inquiry 216

PROUST *substitutes any objects whose values are already known into the goal expression.*

objects whose values are already known into the goal expression. At this point the only information available about ?New and ?Sentinel is what appears in the problem description. There the value of ?Sentinel is listed as 99999, but the value of ?New is not listed. Therefore, the value of ?Sentinel is substituted into the goal expression, but ?New is left unchanged. The resulting goal expression is (Sentinel-Controlled-Input ?New 99999).

PROUST must now retrieve from its programming knowledge base plans that could be used to implement the goal Sentinel-Controlled-Input. It retrieves the filler of the Instances slot of the definition of Sentinel-Controlled-Input shown in figure 4. This filler is a list of five items: Sentinel-Process-Read-While, Sentinel-Read-Process-While, Sentinel-Read-Process-Repeat, Sentinel-Process-Read-Repeat, and Bogus-Counter-Controlled-Loop. Each of these is the name of a plan. PROUST selects the first plan from the list, Sentinel-Process-Read-While. This will be PROUST's initial hypothesis of how the program implements the goal Sentinel-Controlled-Input.

Just as known values of objects were substituted into the goal expression (Sentinel-Controlled-Input ?New ?Sentinel), these same substitutions must now be performed on the selected plan. To see what substitutions must be made, PROUST examines the Form slot of the definition of Sentinel-Controlled-Input, (Sentinel-Controlled-Input ?Input ?Stop). The Form slot indicates which pattern-variable names are used in the plans that implement the goal. By comparing the Form slot to the goal being analyzed, PROUST determines that each occurrence of ?Input in the selected plan should be replaced by the value of ?New. Each occurrence of ?Stop should be replaced by the value of ?Sentinel or 99999. Because the value of ?New is not known, PROUST simply replaces ?Input with the variable name ?New. PROUST assumes that the process of matching the plan against the program will determine what the value of ?New is.

Figure 6 shows how the Sentinel-Process-Read-While plan is matched against the program example in figure 1a. Matching starts with the WHILE loop. The pattern in the plan for the WHILE loop is (WHILE (< > ?New 99999) . . .). There are two WHILE loops in this program: WHILE Val < > 99999 DO . . . and WHILE Val <= 0 DO . . . . PROUST tries to match each pattern against each of these statements. (WHILE (< > ?New 99999) . . .) matches WHILE Val < > 99999 DO . . . , provided that Val is substitued for ?New. (WHILE (< > ?New 99999) . . .) does not match WHILE Val <= 0 DO . . . because the statement has a <= test instead of a < > test, and because it tests against 0 instead of 99999. Therefore PROUST selects WHILE Val < > 99999 DO . . . as the match for the plan pattern. Since Val must be substituted for ?New so that the pattern matches, Val is recorded as the binding for ?New. Afterward, any component of the plan that has ?New in it will have Val substituted for ?New.

The next plan component that PROUST matches against the program is (BEGIN . . .). There are several different BEGIN statements in the program that could be matched against this pattern. However, in the plan template the (BEGIN . . .) pattern appears inside of the WHILE pattern that was just matched. This means that the BEGIN statement that this pattern matches must be located inside of the WHILE Val < > 99999 DO . . . statement. Therefore, there is only one BEGIN statement that has an appropriate match.

When PROUST tries to match the (SUBGOAL (Input ?New)) components, a different type of processing is required. These plan components are goals; to match them against the program, PROUST must go through the same plan-selection

(continued)

READ PLAN
(Read Val)
?New = Val
Sentinel-Process-Read-While

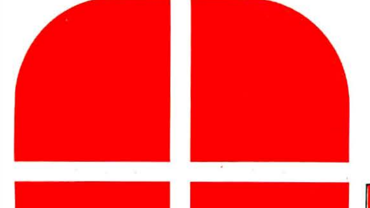
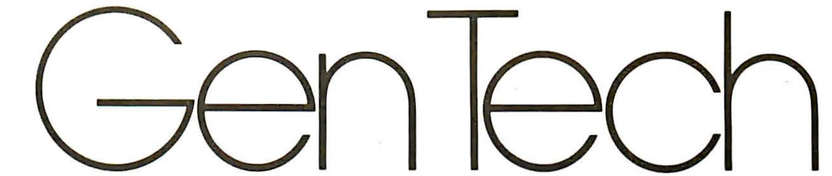
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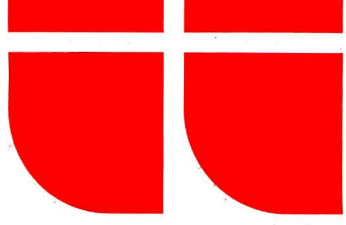
```
Writeln( 'Enter value:' );
Read( Val );
WHILE Val< >99999 DO
  BEGIN
    WHILE Val< =0 DO
      BEGIN
        Writeln( 'Invalid entry, reenter' );
        Read( Val );
      END;
    Sum := Sum+Val;
    Count := Count+1;
    Writeln( 'Enter value:' );
    Read( Val );
  END;
```

```
((SUBGOAL (Input ?Input))
 (WHILE (< > ?Input 99999)
   (BEGIN
    ?*
    (SUBGOAL (Input ?Input)))))
```

?New = Val
READ PLAN
(Read Val)

Figure 6: *This shows how the* Sentinel-Process-Read-While *plan is matched against the program in figure 1.*



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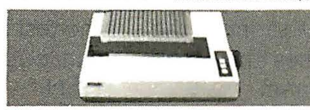
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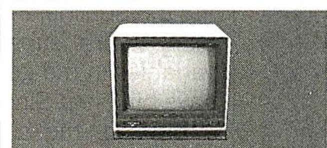
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Since PROUST first generates a possible implementation and then matches it against the program, it is performing analysis by synthesis.

process that it went through in selecting the Sentinel-Process-Read-While plan. It first substitutes all pattern variables in the goal expression that have bindings. Since ?New has Val as a binding, the subgoal expression becomes (Input Val). PROUST then retrieves plans from the plan database that implements Input. One such plan is the READ PLAN, which employs a Pascal Read statement to input the value. This plan matches the Read statements in the program.

This example shows how PROUST analyzes programs by predicting the plans that might be used and then testing these predictions. By selecting from a range of different plans and subplans for each goal, PROUST is able to generate a variety of different ways of implementing each goal. Since PROUST first generates a possible implementation and then matches it against the program, it is performing analysis by synthesis. In general, generating plan hypotheses and matching them against programs is rather more complex than the scenario presented here; for more information, see reference 3.

IDENTIFYING BUGS

When the Sentinel-Process-Read-While plan was matched against the program in figure 1a, the plan matched exactly. Since there were no match errors, there must not have been any bugs in that particular plan. It is frequently the case, however, that none of the plans that PROUST predicts matches the program. When this happens PROUST must look for bugs that account for the mismatches in one of the plans. In this section we will discuss one of these mismatches in connection with the WHILE-for-IF example in figure 2a and show how it leads to the discovery of a bug.

The bug in the WHILE-for-IF example is discovered in processing the Input-Validation goal. One of the plans that PROUST suggests for implementing this goal is the so-called Bad Input Loop Test plan. This plan consists of a WHILE statement that tests the input to see if it is out of range, an error message inside the WHILE loop, an Input subgoal that rereads the input if it is out of range, and a test to see if the exit condition for the main loop has been satisfied.

Listing 2 illustrates a correct implementation of this plan (solving the Averaging Problem).

The Bad Input Loop Test plan matches the WHILE-for-IF example of figure 2a in all but one respect: there is no test for the exit condition of the main loop, such as IF Val < > 99999 THEN . . . . Where an IF statement is expected, a WHILE statement appears instead. PROUST has thus encountered a *plan difference*, i.e., a difference between the expected plan and the code. When PROUST encounters plan differences it does not give up on the plan; instead, it tries to find a way of interpreting the plan differences as bugs.

In most cases plan differences are explained by means of *bug rules*. Each bug rule has a test part, which examines the plan differences to see whether the rule is applicable, and an action part, which explains the plan differences.

Figure 7 shows the bug rule that is invoked to explain the plan differences in the WHILE-for-IF example. The rule is written in slot-filler notation; one set of slots constitutes the test part of the rule, and another set constitutes the action part. In the WHILE-for-IF rule the test part consists of a Statement-Type slot and an Error-Pattern slot. The Statement-Type slot indicates that the plan com-

ponent that failed to match the program must be an IF statement. The Error-Pattern slot has the value (IF . WHILE); this indicates that a WHILE statement was found when an IF statement was expected. These test conditions are both met in the WHILE-for-IF example, so the action part of the rule is activated. The action part of this rule consists of a Bug slot; the filler of this slot is a description of the bug associated with the plan difference. The bug in this case is a WHILE-for-IF confusion. PROUST's bug analyses of student programs consist of bug descriptions such as this. When PROUST presents its findings to the student, it takes each bug description and generates an English-language translation for it and, if appropriate, generates data illustrating the presence of the bug.

Listing 2: *A correct implementation of the* Bad Input Test *plan.*

```
WHILE Val<=0 DO
  BEGIN
    Writeln( 'Invalid data, please reenter' );
    Read( Val );
  END;
IF Val <> 99999 THEN
  . . .
```

```
(Define-Rule WHILE-for-IF
  Statement-Type     IF
  Error-Pattern      (IF . WHILE)
  Bug                (WHILE-for-IF Confusion (FoundStmt ,*MRet*)
                                   (HistInst  ,*HistoryNode*)))
```

Figure 7: *The* WHILE-*for*-IF *bug rule invoked by* PROUST *to explain the plan difference between the faulty part of the program of figure* 1 *and the correct implementation of this part in listing* 1.

TEST RESULTS

PROUST has been tested on large numbers of beginners' programs. We assigned a class of novice programmers the Rainfall Problem (an elaboration of the Averaging Problem), which is shown in figure 8a.

We modified the Pascal compiler our students were using so that it would save copies of every syntactically correct program that they compiled. This allowed us to examine not only the final solution the students handed in, but also every intermediate version of their program. Since the first versions are likely to be the buggiest, this let us test PROUST under the most difficult conditions possible.

Figure 8b shows the results of running PROUST on the Rainfall Problem. There are 206 different attempted solutions to the Rainfall Problem in the test set. Of these, PROUST was able to derive a complete understanding of 79 percent of the programs, identifying 94 percent of the bugs, a percentage far higher than people are able to achieve. The chart also indicates that 6 percent of the bugs were not recognized and 55 were false alarms. Bugs are counted as not recognized if they are either misdiag-

(continued)

(a)

Write a Pascal program that will prompt the user to input numbers from the terminal; each input stands for the amount of rainfall in New Haven for a day. Note: Since rainfall cannot be negative, the program should reject negative input. Your program should compute the following statistics from this data:

1. the average rainfall per day
2. the number of rainy days
3. the number of valid inputs (excluding any invalid data that might have been read in)
4. the maximum amount of rain that fell on any one day

The program should read data until the user types 99999; this is a sentinel value signaling the end of input. Do not include the 99999 in the calculations. Assume that if the input value is nonnegative, and not equal to 99999, then it is valid input data.

(b)

Total number of programs:	206	
Number of programs with bugs:	183	(89 percent)
Number of programs receiving full analyses:	161	(79 percent)
Total number of bugs:	570	
Bugs recognized correctly:	533	(94 percent)
Bugs not recognized:	29	(6 percent)
False alarms:	55	
Number of programs receiving partial analyses:	35	(17 percent)
Total number of bugs:	191	
Bugs recognized correctly:	71	(37 percent)
Bugs deleted from analysis:	70	(37 percent
Bugs not recognized:	50	(26 percent)
False alarms:	19	
Number of programs PROUST did not analyze:	9	(4 percent)

Figure 8: *(a) The Rainfall Problem was assigned to a class of novice programmers to test the effectiveness of* PROUST. *(b) This shows the results of running* PROUST *on the Rainfall Problem.*

Ultimately, PROUST will be incorporated into a programming curriculum for students.

nosed or missed entirely. Bugs are counted as false alarms if they are either not present in the program or if they are present but misdiagnosed. Consequently, misdiagnosed bugs are counted both as false alarms and as not recognized, which inflates the total number of diagnosis errors.

When PROUST fails to understand a program completely, its ability to recognize bugs deteriorates; 17 percent of the programs were analyzed partially. In such cases PROUST deleted from its bug descriptions those bug analyses that were questionable, given that the program was only partially understood. The bug descriptions that remained were frequently wrong, but at least PROUST was able to warn the student to take the analysis with a grain of salt. The remaining 4 percent of the programs deviated from PROUST's expectations so drastically it could not analyze them at all. In these cases no bug report was generated.

We are not yet sufficiently satisfied with PROUST's accuracy to make it generally available to students. The false-alarm rate should be lower, and the fraction of programs that PROUST analyzes completely should be higher. When part of a program cannot be analyzed, PROUST should try to determine why that part of the program cannot be analyzed and try to account for the unanalyzed code. Once this is done we expect PROUST to succeed on 80 to 85 percent of the programs it analyzes. At that stage we will make it available to students on line.

Conclusion

PROUST is capable of high-quality analysis of bugs in novice programs. It is almost at the level where it could be incorporated into a programming curriculum and provide significant benefits to students. Here we have given a simplified view of how PROUST finds bugs. The next step is to build an automated programming course around PROUST. Such a system would not only correct students' mistakes but would also suggest additional problems for the students to solve to give them practice where they need it. ■

AUTHORS' NOTE

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Additional papers dealing with bug classification, automatic debugging, and the cognitive underpinnings of programming can be obtained by writing to the following address: Cognition and Programming Project, Department of Computer Science, Yale University, POB 2158 Yale Station, New Haven, CT 06520.

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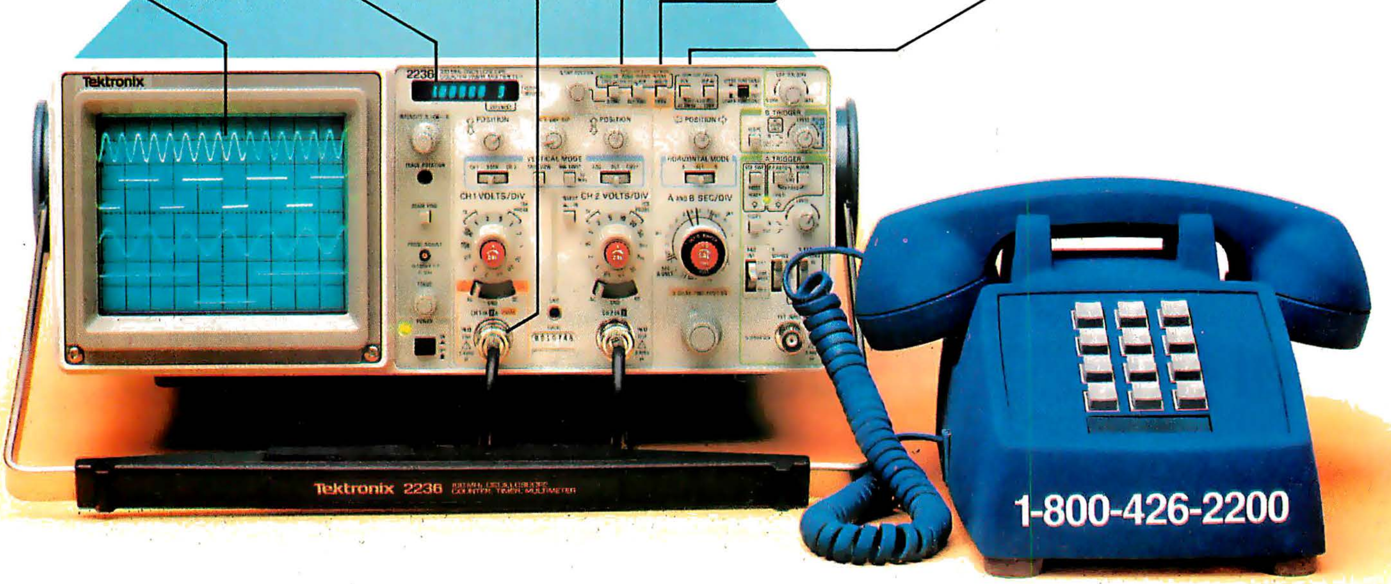
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ARCHITECTURES FOR AI

BY MICHAEL F. DEERING

Hardware and software for efficient processing

AS ARTIFICIAL-INTELLIGENCE software grows in complexity and as AI applications move from laboratories to the real world, computational throughput and cost are increasingly important concerns.

In general, there are two motives for increasing the efficiency of computations. One is the need to obtain faster computation, regardless of cost. This may be due to explicit real-time constraints or to current methods being taxed well beyond the limit of complexity or timely response. The other motive seeks to obtain a better cost/performance ratio. Behind both, however, is usually the imperative of real-world market pressures.

Opportunities for increased efficiency in AI computations exist at every level. Improved instruction-set designs combined with improved AI language semantics allow more powerful compiler optimization. Concurrent machines allow parallel execution of LISP and declarative constructs, raising issues of *and, or,* and *stream parallelism.* Custom VLSI (very-large-scale integration) hardware for current AI performance bottlenecks includes devices such as hardware unifiers, associative memory, and communication hardware for coordinating parallel searches. Many of these speedups are orthogonal and can potentially increase performance by several orders of magnitude. However, this is not always the case; some language optimizations have a tendency to serialize computation, thereby negating the gains of parallelism.

As part of an effort to design a massively concurrent architecture for AI computation (the Fairchild FAIM-1 project—see the text box on page 202), this article examines several potential throughput increases and their interactions.

MISCONCEPTIONS

There are several misconceptions about what needs to be done to improve computational throughput for AI. Since most AI programming is done in LISP, many researchers believe the key is simply to make LISP faster. However, this approach ignores other, easily obtainable potential speedups.

Other computer scientists see no reason to concentrate on anything other than the fundamental problem of parallelism, an approach that presumes a routine solution of a very difficult problem: decomposing arbitrary AI computations to effectively use thousands of parallel processors. A problem with this approach is that most programs, even ones with a high degree of inherent parallelism, almost always have several serial bottlenecks. As an example, most parallel programs need to gather the result of one batch of parallel computations for reflection before generating the next batch. In many cases, these serial processes dominate the running time of the entire program. So you cannot ignore the issue of how to extract as much serial speed as possible from languages and machines. Otherwise, once you've built an expensive parallel machine hundreds of times faster than existing machines, a new compiler or microcode might make some existing serial machines even faster. The machine coded unifier in the Crystal AI language, for instance, is two orders of magnitude faster than the LISP-coded unifier in the pre-

(continued)

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decessor PEARL AI language (see reference 3).

Software Improvements

One way to improve AI language implementations would be to compile the language directly to machine code. Most AI "languages" are not computer languages but packages of routines on top of an existing language, usually LISP. While this is a great way of rapidly prototyping a language and results in considerable savings in development costs over a traditional full compiler, it does not lead to very efficient implementations. If increasing the speed of AI applications leads to the extreme of building custom parallel processors, it is silly not to compile AI languages directly onto these processors. There is a large body of computer science knowledge on compilation that can be brought to bear, and great potential for performance increases. (Consider the 100-times plus speed difference between most LISP-based Prolog interpreters and Warren's DEC-20 Prolog compiler—see reference 17.)

Make sure that the language is compilable. Because most AI languages have been interpreted, issues of compilability generally have not been thought through. Language features that seemed efficient in an interpreted environment may be very slow when compiled, if they are compilable at all. A proper choice of features in light of a compiled environment leads to more efficient program execution.

Another problem with many AI languages is the lack of general tools to support common applications. While it can be argued that this allows users to write their own customized tools (which may be very efficient), most users will do a much worse job than the language implementor could. For example, PEARL did not directly support any particular theorem-proving or search system (such as forward and backward chaining), leaving users to their own devices. But the MRS system (reference 11), while providing a convenient meta-level control for users to write their own search systems, also provides a range of built-in search strategies, from backward chaining to full-resolution theorem proving. An extensive library of well-written routines of general use speeds the operation of typical user programs (not to mention their development).

Hardware Considerations

It is often claimed that conventional computer instruction sets are not well suited for AI software, but there have been few attempts to quantify the reasons why. For older-generation machines, you can easily point to severe address-space limitations and the lack of flexible pointer-manipulation facilities (reference 6). But what of the new, modern machines, such as the DEC VAX, Motorola 68000, National Semiconductor 16000, and various RISC (reduced instruction set computer) machines—how do they compare with the custom LISP machines (references 13 and 15)? To obtain insights into instruction-set design, I examined several LISP systems and the fine details of their implementation (reference 5). I learned, among other things, that it is very important to identify how rich an environment you wish to support. For example, contrary to many people's expectations, on a large application program Franz LISP (reference 8) on a DEC VAX-11/780 was not significantly slower than Zetalisp on a Symbolics 3600. The difference was that nearly all type-checking and generic-function capabilities were either turned off (by the programmer) or missing in Franz LISP, where the overall environment was much poorer. Assuming that such features are not frills, I also examined the expense of providing them on different architectures.

Flexible LISP processing depends on dynamic type checking and generic operations. Associating the data type directly with the data object means that the data type will always be at hand during processing, and this is the reason that tagged memory architectures are well suited to LISP processing. Because of this association, the speed of various processors on the generic LISP task depends on how fast the processors can effectively emulate a tagged-memory architecture.

I performed a number of experiments to compare LISP systems on different processor instruction sets. As a representative sample, table 1 shows the timing results for a simple aggregate function incorporating some of the most common LISP primitives—CAR, CDR, plus, and function call/return.

More extensive benchmarks have borne out roughly the same speed ratios. Not unexpectedly, the variance

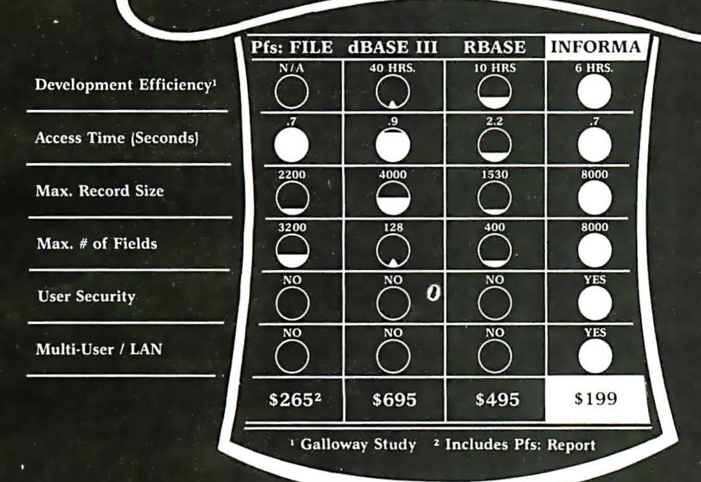
(continued)

Table 1: *The timing results of the aggregate function* foo *for three* LISP *implementations on six different processors.*

LISPs vs. Processors on
(defun foo(x)(+(car x)(cdr x)))

Machine	Zetalisp	Franz LISP	PSL
VAX	53.8 µs	13.9 µs	5.6 µs
68000	65.2 µs	43.6 µs	5.8 µs
68010	68.6 µs	43.6 µs	10.6 µs
68020	16.1 µs	19.9 µs	3.1 µs
MIT CADR	19.0 µs	n/a	n/a
3600	6.4 µs	n/a	n/a

Anything Better Would Have To Be Magic



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Max. # of Fields	3200	128	400	8000
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[1] Galloway Study [2] Includes Pfs: Report

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Listing 1: MC68010 *assembly-language code for the* LISP *function* CAR. *The code in boxes can be replaced by enhancements to the instruction set to decrease the code's execution time.*

```
Zetalisp car for 68010

     ;To take the car we do a few lines of in line code and
     ;then index jump to a subroutine. (Space for time.)
     ;The cons cell to take the car of is assumed in a0.

;dispatch to CAR subr based upon the tag in upper bits of a0

     4    move1 a0,d2          ;put a copy of the arg into d2

    24    lsll   #8,d2         ;first 8 of: shift copy over by 9 bits

  ┌───────────────────────────────────────────────────────────────────┐
    10    lsll   #1,d2         ;last 1 of: shift copy over by 9 bits

    14    andl   #0x1F0,d2     ;and off non-tag (shifted over)

     4    movel  d2,a2         ;need tag in A-reg for dispatch

    18    jsr    CAR(a2)       ;branch to car table indexed by type

          ;At return, the car of the object is in a2
  └───────────────────────────────────────────────────────────────────┘

;The CAR subroutine.

CAR + DTP-CONS: ;CAR procedure entry point

          ;for nornal cons cell.

;We will arrive here if the argument passed to car was of type

;"pointer to cons cell". Other objects passed to car = > error


;follow the point to the car

     4    moveal    a0,d2          ;put a copy of the arg into d2

  ┌───────────────────────────────────────────────────────────────────┐
    14    andl   #0xFFFFFF,d2      ;and off tag

     4    moveal    d2,a2          ;put d2 into an address register

    12    moveal    (a2),a2                  ;follow the car pointer.
  └───────────────────────────────────────────────────────────────────┘

;dispatch to TRANSPORT subr based upon the tag

; in the upper bits of a2

     4    movel a2,d2          ;put a copy into d2

    24    lsll   #8,d2         ;first 8 of: shift copy over by 9 bits
```

(continued)

exceeded 50 percent. Slight modifications of the compilers or instruction sets produced similarly large changes in the speeds.

Existing Franz LISP and PSL (reference 12) compilers for the DEC VAX and Motorola 68000 were used to compile foo. Type checking was turned off to obtain the fastest speeds. (Both PSL and Franz LISP were told not to verify that the arguments of + were small integers; Franz LISP did and PSL did not check for numeric overflow.) The timing figures were generated by examination of the assembly code produced and some actual machine timings. The timings of Zetalisp for the 3600 and CADR were taken by running existing systems. Zetalisp-like operations for the DEC VAX and Motorola 68000s were hand-coded, and the timings were produced in the same way as those for PSL and Franz LISP. The 68000 and 68010 were 10-MHz, no-wait-state machines. The 68000 used 24-bit addresses, leaving the upper 8 data bits free for tag values. The 68010 used 32-bit addresses and required removal of the tag bits with an AND operation before addresses could be used. The 68020 timings are estimates based upon the best "cache case" timings in the 68020 data book and are not as accurate as the timings for the other machines. The 68020 is assumed to be running at 16 MHz with an external 16K-byte memory cache and memory-management unit (MMU), giving a memory-access time of 185 nanoseconds. (The 68020 has an additional small instruction cache on board.)

Other experiments examined the architectural requirements for fast computation of some AI operations not directly supported by LISP, in particular unification and associative search. When AI languages are fully compiled, these two functions often become the computational bottlenecks. For traditional microprocessor instruction sets, the requirements of these operations turned out to be the same as for LISP primitives: fast simulation of tagged architectures. More specifically, the instructions and

capabilities that would make a conventional microprocessor better suited for LISP (along with Prolog, Krypton, MRS, PEARL, etc.) are

- "Extract bit field and dispatch": an instruction to extract a sequence of bits from an operand, then add these bits to a dispatch table address, and jump indirect. This is necessary for rapid handling of tag values in generic operations, type checking, and for helping with unification.
- "Extract two bit fields, concatenate, and dispatch": an instruction for dispatching on the context of *two* operands (needed for the same reason as the one-argument version).
- The memory address system of the processor should ignore the upper address bits of data addresses that are not otherwise in use. This allows the wasted space in 32-bit pointers to be used as a tag field.

In the Zetalisp-like code, more than 30 percent of the time on the 68000s was spent in emulating the bit-field dispatch instructions. Stripping off the tag bits accounted for approximately another 10 percent. It is therefore estimated that if the existing microprocessors had hardware support for these features, full type-checking LISPs (like Zetalisp) could run almost twice as fast. These percentages come from hand-implementing several Zetalisp primitives on current microprocessors. As an example, listing 1 shows the 68010 assembly language code for CAR. The number of processor clock cycles per instruction is shown in the left-hand column. The boxed code can be replaced by a single instruction (see listing 2).

Listing 2 shows CAR for the 68010 recoded, assuming two architectural refinements. First, assume that the upper 7 bits of all addresses are ignored by the virtual-memory system. Second, assume one additional instruction, "extract bit field and dispatch." This instruction takes the bit field out of the second argument, as specified by the first argument (format: <#starting-bit, field-width>), adds it to the third argument (the jump-table

(continued)

```
   10   lsll   #1,d2           ;last 1 of: shift copy over by 9 bits
   14   andl   #0x1F0,d2          ;and off non-tag (shifted over)
    4   movel  d2,a3           ;need tag in A-reg for dispatch
   10   jmp    TRANSPORT(a3)   ;branch to car table
                               ;indexed by type.
                               ;The reason for this jump is to check
                         ;for possible invisible pointers, unbound, etc.

TRANSPORT + NORMAL: ;jump entry point for normal
                    ;cons cell contents
    8   rts         ;We're all done, return
_____

182 clocks, @10MHz = 18.2µs
```

Listing 2: *The modified listing 1 code, incorporating architectural refinements to the processor's instruction set.*

```
;Now the car routine is recoded using the new instructions:

;index jump to a subroutine.

;dispatch to CAR subr based upon the tag in upper bits of a0

   22   extract-dispatch <#26,#6>,a0,CAR

;The CAR subroutine.

CAR + DTP-CONS: ;CAR procedure entry point for

                ;normal cons cell.

;follow the pointer to the car

   12   moveal (a0),a2   ;the upper 6 bits of a0 are ignored.

;dispatch to TRANSPORT subr based upon the tag

;in the upper bits of a2

   22   extract-dispatch <#26,#6>,a2,DISPATCH

TRANSPORT + NORMAL: ;jump entry point for normal

                    ;cons cell contents

    8   rts         ;We're all done, return
_____

64 clocks, @10MHz = 6.4µs, 2.8 times faster
```

base address), and indirectly jumps through this address. (The 68020 has a fast bit-field extraction instruction. This accounts for much of its increased speed over the older 68000 on the LISP task in table 1.)

For new, fully custom machine designs that are tailored specifically for AI, such features can all be built in. With a tagged architecture, many generic operations, such as add, do not need to be dispatch subroutine calls. Rather, the processor can examine the tags of the arguments to an add instruction and, if they are simple integers, directly perform the add. If the arguments are of a more exotic numeric type, the processor can generate a software interrupt to an appropriate routine. Further, for such designs it is very helpful to have a "smart" memory subsystem capable of rapidly chasing down indirect pointers as on the DEC PDP-10 and the custom LISP machines. Additional customization of an AI instruction-set design generally falls into the category of complete, attached coprocessors rather than just additional instructions. This tactic has already been taken by many microprocessors whose floating-point instructions are handled by what could be viewed as attached coprocessors. The specific categories of important attached coprocessors include pipelined unifiers, associative-memory subsystems, multiprocessor communication packet switchers, and special signal-processing chips for vision and speech.

Studies of a custom instruction set for the FAIM-1 machine indicate that not only can a single processor be designed that is memory-bound by DRAM (dynamic random-access read/write memory) access delays but that this is the case even when a large cache is employed. This is an important fact. It means that parallel machines sharing a single large common memory are a bad idea because there isn't enough memory bandwidth to go around.

PARALLELISM: THE GREAT HOPE

Traditional views cite concurrency as a great method of obtaining increased computational power. In practice, however, designers continue to concentrate on making faster and faster single-processor machines. Now that hard technological limits have been reached for serial processors, parallelism has become recognized as perhaps the only hope for further performance increases. Unfortunately, concurrency is not free—it brings new systems organization problems to the fore.

The first conceptual problem with parallelism is the confusion between multi*processing* and multi*processors*. There are algorithms that very elegantly express a set of cooperating processes

(continued)

ARCHITECTURES

(e.g., writers and readers), but these same algorithms have little or no inherent parallelism that can be exploited by parallel computers. Just because an algorithm can be expressed in concurrent terms is no guarantee that, when run on many parallel processors, it will run significantly faster than as separate processes on a single sequential machine.

The true measure of parallelism is how much faster a given program will run on *n* simple parallel processors compared to how fast it would run on a single simple processor and for what ranges of *n* this is valid. The best you can hope for in principle is a factor of *n* speedup, but in practice this is rarely reached (due to overhead and communication contention). The maximum amount of speedup attained for a given program using any number of parallel processors indicates the inherent parallelism of that program. Unfortunately, for most existing programs written in traditional computer languages, the maximum parallelism seems to be about a four-times speedup (reference 10). This surprisingly low number is due to the style of programming enforced by the traditional languages. There are special-purpose exceptions to this rule and the hope is that nontraditional parallel languages will encourage more concurrent algorithms. Compilers for parallel machines can take advantage of techniques such as and, or, and stream parallelism if AI languages support the concurrent control structures that give rise to them. But the jury is still out as to the amount of speedup such techniques can deliver.

Another problem in parallelism is failure to take the entire systems context into account. Before building a parallel machine, you must not only simulate the machine but determine how to write large programs for it. This reveals potential flaws in the machine before commencing with time-consuming hardware development. The simulation must properly take scheduling and technologically realistic hardware-communication overhead into account or the timings produced will have little or no connection to reality.

Good examples of software systems that have not taken realistic hardware considerations into account are some of the parallel LISPs that have been proposed (reference 9). These proposals point out places in LISP-like processing where multiple processors could be exploited, but they do not analyze the overheads incurred. They usually assume that multiple processors share a single large main memory where CONS cells and other LISP objects are being stored. This is the equivalent of assuming that memory is infinitely fast, which is just as unrealistic as assuming that processors are infinitely fast. The problem is that with current technology a *single* well-designed LISP processor could run faster than current mass-memory technology could service it. Adding processors would thus not result in any increase in throughput.

There are several reasons why designers of parallel LISPs may have missed this fact. Perhaps one is that current 68000 LISPs are not memory-bound. Another is the potential use of caches to reduce the required memory bandwidth to each processor. However, even with caching, the number of processors that can be added is not unlimited; a 90 percent hit-rate cache would accommodate only 10 processors.

What about the thousand-processor architectures envisioned? Experimental data shows that a single processor can run significantly faster than memory can service it: You must employ a cache just to keep a single processor running full tilt. The lesson is that processors are still much faster than memories, and any sharing of data between multiple processors (beyond a few) must be done with special communication channels. In other words, MIMD (multiple instruction, multiple data) machines with a single shared memory are a bad parallel architecture. This has important implications for some AI paradigms, such as Blackboard sys-

tems and Production systems that (in their current form) rely on memory for communication between tasks.

This is not to say that there are no opportunities for spreading LISP-like processing across hundreds of processors. There are many techniques other than a single shared-memory system for connecting processors. More realistic areas of research include the spreading of parallel inference computation via techniques of and, or, and stream parallelism. The point is that all of these techniques incur some overhead and you cannot simply solve the parallel-computation problem by saying that arguments to functions should be evaluated in parallel. You must first study hardware technology to determine at what grain sizes parallelism is feasible and then figure out how to make AI-language compilers decompose programs into the appropriate-size pieces.

CUSTOM VLSI

One of the principal hopes for more efficient future computation is the use of custom VLSI hardware to accelerate particular functions. The ideal functions for silicon implementation should be current bottlenecks in AI systems and generic to many AI tasks. Four of the most important classes of operations that fit this description are symbolic matching of abstract objects, semantic associative memory, parallel-processor communication, and signal-to-symbol processing.

MATCHING AND FETCHING

Matching two objects is a general and pervasive operation. Most AI languages define one or more *match* functions on their structured data types (such as frames). Some of these match functions are very ad hoc (thus supposedly flexible), but others are subsets or supersets of unification. If significant support for matching is to be provided in hardware, the match function must have well-defined semantics.

AI-language objects can be complexly structured and used to represent semantic knowledge. The objects can contain embedded pattern-matching variables that are given bindings as a side effect of the match operation. Thus the matching of these objects is complex. To give the flavor of the matching process, I'll present a short description of the unification matching function. (For a more exact description, see any good description of the Prolog language.) Matching is best described by recursively defining the semantics of the match operation:

1. If the two objects to be matched are structured (nonscalar) objects, recursively match their subcomponents (or "slots"). The two objects are said to match if and only if all pairs of slots match. Otherwise, the objects do not match, and any side effects of the matching process must be undone.
2. If the two objects to be matched are scalar objects (integers, floating-point numbers, atoms, symbols, characters, etc.), then the match function reduces to simple equality.
3. If one of the two objects to be matched is a pattern-matching variable, the match operation must check the variable's binding state. If the variable already has been bound to a value, the match operation continues using the value in place of the variable. If the variable has no current binding, it is bound to the value of the object against which it was being matched, and the match succeeds.
4. If both of the objects to be matched are unbound pattern-matching variables, then one is bound to the other as a placeholder for possible future bindings. If either variable is later bound to a "real" value, then both variables will be bound to this value.

(continued)

The match operation produces a binary result: Did the two objects match successfully or not? Successful matches produce the bindings of pattern-matching variables necessary to make the two objects identical in as general a way as possible.

Many AI languages augment this match operation with checks for circularity in the list structure (the "occure check"), segment matches (similar to Snobol's), and the matching of sets and bags.

When a match function is applied to a database of objects, the operation is called *fetching*. In this case matching becomes the inner loop operation, and this is a context in which matching should be optimized. An ideal solution would integrate matching circuitry with memory circuitry so that fetching would become a memory access of a content-addressable memory (CAM). The choice of match function is critical. To obtain reasonable memory densities, the relative silicon area of match circuitry cannot overwhelm that of the memory circuitry. Unfortunately, full unification and more complex match functions require too much circuitry to be built into memory cells. But if a formal subset of unification could be built in, then the CAM could act as a prefilter function for unification.

The primary source of unification complexity is the maintenance of the binding environment. The match function of *mock unification* resembles full unification except that all variables are treated as "don't cares" and no bind-

(continued)

FAIM-1 Project Overview

Our goal is to produce a *high-performance symbolic multiprocessor*, 100 or more times faster than current machines in common use (e.g., the DEC VAX-11/780) to meet the voracious computational demands of future artificial-intelligence applications.

The FAIM-1 (Fairchild Artificial Intelligence Machine) is a multiprocessor system consisting of a number of identical processing elements called *hectagons* interconnected by a communication network. Each hectagon is a complete computer capable of sequentially executing a compiled program that is stored in its local memory. Hectagons communicate with each other via messages that are sent through communication ports. A hectagon has six ports that may be active concurrently.

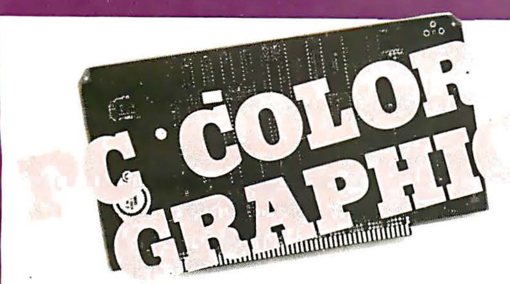
The FAIM-1 architecture permits the connection of arbitrary numbers of hectagon processing elements in a hexagonal-mesh topology. The ensemble of hectagons is capable of exploiting very large levels of concurrent multiprocessing and as such should provide an extremely attractive target machine for future concurrent AI applications due to its performance. Moreover, each individual hectagon is itself a concurrent processor composed of six modular sybsystems, each of which provides an important level of support for symbolic computation.

A hectagon is composed of six self-timed subsystems named FRISC, SRAM, ISM, CxAM, SPUN, and Post Office. Three of these subsystems (ISM, CxAM, and SRAM) are specialized memory systems that provide "intelligent" storage, while the other systems support inter-hectagon communication (Post Office), processing (FRISC), and unification (SPUN).

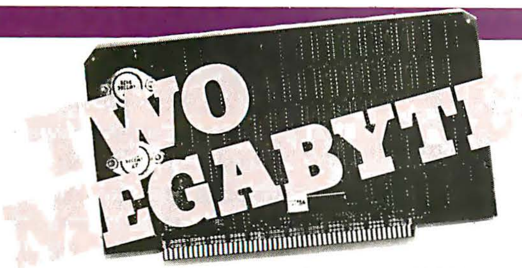
FRISC: The "fanatically reduced instruction set computer" component of the hectagon corresponds to the central processing unit in a conventional computer. It is a stack-oriented machine with a 20-bit word composed of a 16-bit data field and 4-bit tag field. Tag bits and associated tag-handling hardware support generic operations.
SRAM: The FRISC views most data structures as objects; a conventional memory with a small finite-state machine attached to it (collectively called the SRAM) provides an object-oriented memory system for the FRISC. For example, using the data tag bits the SRAM can chase a pointer chain to retrieve an object requested by the FRISC.
ISM: The "instruction stream memory" subsystem delivers instructions to the processor at high speed. Thus, the normal address calculation activities that have traditionally been the processor's responsibility are the ISM's job.
CxAM: The "context-addressable memory" subsystem provides direct hardware support for important pattern-matching functions inherent in symbolic programs. The structure of both entries and queries in the CxAM is an S-expression. Therefore, each slot can either be a structure or an atom. Atoms can be symbols, numbers, variables, or *don't cares*. The CxAM responds to four commands: Find Match, Give Match, Delete Structure, and Add Structure. The CxAM manages its own free space and removes garbage automatically.
SPUN: The "streamed pipeline unifier" supplies direct hardware support for logic programming. The CxAM finds the next rule or set of rules to be tried but does not perform full unification since its match function does not consider variable bindings. The SPUN unit takes the query and the streamed set of matched structures, detects which variables still need to be matched, fetches the binding in the current context from the SRAM, and completes the unification. This may entail binding a variable, in which case the SPUN unit must post this binding back in the SRAM. More complex structure manipulation requires the SPUN to interrupt the FRISC for services.
Post Office: Hectagons communicate by sending messages to each other; it is the duty of the Post Office to provide autonomous communication support for its hectagon. If a message's destination is not one of the sender's six neighboring hectagons, the Post Office will route the message to its destination by sending the message to a neighbor that is *generally* in the direction of the destination.

Conceptually, messages may be of arbitrary length. In fact, each message is broken up and sent as a sequence of fixed-length packets.

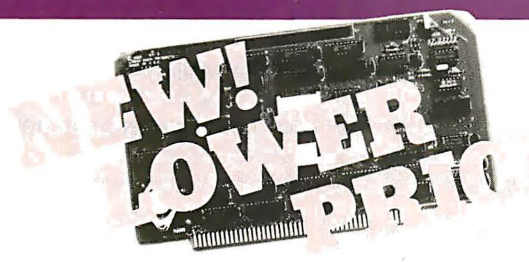
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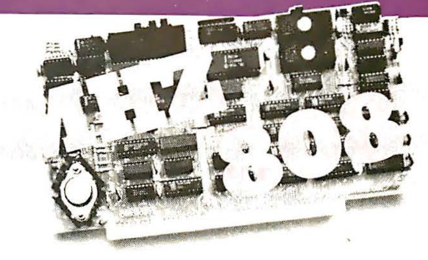


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ing list is formed. In terms of the definition given above, steps 3 and 4 would be replaced with null operations—variables are just treated as "always match" objects. Mock unification is the most powerful subset of unification that is state-free. Therefore, mock unification is a suitable candidate for integration into VLSI memory. Associative-memory systems that utilize mock unification as their match function are called CxAMs: context-addressable memories.

From a hardware point of view, designing associative-memory architectures involves a resource trade-off between processing and memory: The more hardware devoted to "matching," the more data that can be examined in parallel, leading to faster search time per bit of storage. But conversely, the more matching hardware there is, the smaller the amount of hardware that can be devoted to data memory and the lower the density of the associative memory. The data-path bandwidth of the match hardware is also a factor in making these trade-offs. Therefore, associative memories can be rated by their storage density (bits stored per unit of silicon area) and search throughput (bits searched per unit of time per unit of silicon area).

I examined two classes of associative memory in which the match function is mock unification. One integrated the matching circuitry with memory circuitry, the other was hash-based. Hashing was considered because in many applications in the past software hashing has dominated CAM technology (reference 7). In more detail the two classes are

1. Brute-force search: The contents of a memory are exhaustively searched by some number of parallel match units. For this class of search a custom VLSI mock-unification-memory architecture was designed.
2. Hashing: Objects to be fetched are hashed, and then the collision list is serially searched by a match unit. A proposed VLSI implementation of PEARL's hashing scheme (called the HCP, or hash coprocessor) served as an embodiment of hash-based searching. In this system the bit storage is conventional DRAM.

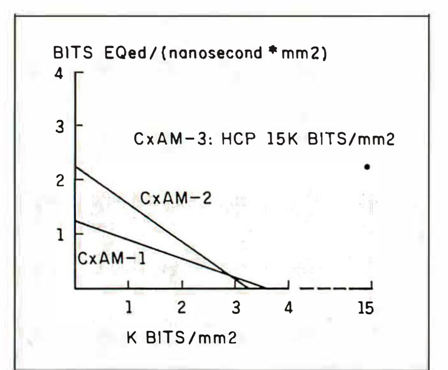


Figure 1: *A graph of the range of bit and search-power densities for a CxAM design.*

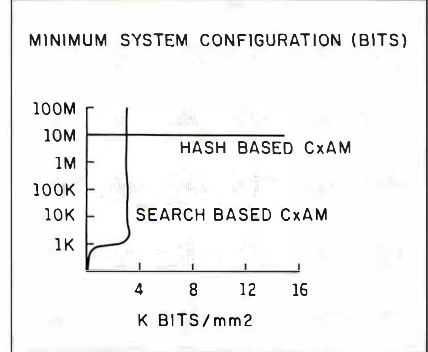


Figure 2: *The minimum-usable-size system for use with the hashing CxAM. Note that the minimum is too large for some applications.*

Table 2: *A list of AI-language match operations and data types arranged in order of complexity.*

Match Hierarchy

Match Operation	Object Type
Compare Instructions	32-bit data object
LISP EQ Function	Atomic LISP objects
LISP EQUAL Function	S-Expressions
Mock Unification	S-Expression with don't cares
Unification	S-Expression with matching variables
Unification & Predicates	S-Expression with variables/predicates
Arbitrary User Code	arbitrary user representation objects

Figures 1 and 2 present graphs of CxAM design-space trade-offs. Figure 1 displays the range of bit and search-power densities. The hash-based CxAM has a single operating point because the fetch time is essentially independent of memory size, as is the density. The search-based CxAM has a variable range because one can vary the relative proportions of storage and processing in such architectures. The two lines represent two different search-based architectures. One has inherently better bit density, but over most of the design space this advantage is negated by an inherently worse search throughput. However, neither design completely dominates the other—a choice between the two will depend on the relative storage-density/match-throughput balance desired. Figure 2 displays the defect of the hashing CxAM. The minimum-usable-size system is too large for some applications.

Thus the trade-offs between these two schemes turn out to be in density and minimum usable size. As a representative data point, both techniques could perform a mock unification of their entire local memory contents for an average query (an S-expression of length 16) in 5 microseconds. The density of the search-based CxAM was about eight times worse than that of conventional single-transistor DRAM. The hashing

scheme used conventional DRAMs and so had high density. But the minimum configuration of a hash-based CxAM memory system using standard 256K-byte DRAMs is 10 megabits, whereas the search-based CxAM can be configured for much smaller system storage sizes.

This extremely high speed of 5 microseconds portends greatly increased efficiency for systems bottlenecked by database fetch time. But which technique to use is very dependent upon grain size. If you are constructing a large nonparallel machine, a bank of HCPs and conventional DRAMs works well. But for an array of small-grain processors with on-chip memories, the search-based CxAM approach is more tractable.

Combining a CxAM with software-based routines provides a range of tailored matching services with sliding power/price/throughput trade-offs. The FAIM-1 machine provides an example of this design. For each of thousands of processors, there is parallel CxAM hardware for mock unification, a single, hard-wired, serial pipelined full unifier, and software support for post-unification matching features (attached predicates and demons). With such a hardware/software hierarchy, simple matches (like LISP's equal) run fast, whereas more complex matching services (such as KRL's—see reference 1) cost more in time due to the software component.

In summary, matching is a common operation ripe for VLSI implementation, but the complexity of match functions varies. Table 2 arranges a simple list of match operations and data types in order of complexity. Successful high-performance AI machines will have to carefully decompose these functions into hardware and software components.

PARALLEL-PROCESSOR COMMUNICATIONS

As already mentioned, processors working in parallel cannot communicate objects and messages by sharing a large common memory. Some sort of special message-passing (and forwarding) hardware is essential for efficient handling of the traffic. In many general-purpose parallel processors, interprocessor communication is *the* computational bottleneck.

SIGNAL-TO-SYMBOL PROCESSING

Despite all the attention given to speeding up high-level symbolic computation, within some AI applications the main processing bottleneck has been in the very-low-level processing of raw sensory data. Within many vision systems, 90 percent or more of the run time may be incurred in the initial segmentation of the visual scene from pixels to low-level symbolic constructs (reference 16). Moreover, limitations of the higher-level vision processing can usually be traced to an inadequate initial segmentation (reference 4). Similar problems arise in many speech systems. In such cases, you should look to special-purpose VLSI processors to directly attack the problem. Examples include special image-processing chips (reference 14), and speech chips (reference 2). As array processors have shown, for these special processors to be usable by programmers they need to be very well integrated with the other hardware and software components of the system and as transparent as possible. Since most AI programmers are not good microcode hackers, you are in trouble if this is the only interface with a special device.

CONCLUSION

Opportunities for increased efficiency abound at all levels of AI systems if we only look, but to obtain the desired throughput increases all the potential improvements outlined here must be made. We must make hard trade-offs between traditional AI programming practices and the discipline necessary to construct algorithms that can make effective use of large multiprocessors. We must compile our AI languages, and these compilers must influence instruction-set design. Key computational bottlenecks in AI processing must be attacked with custom silicon. There is a real need to use

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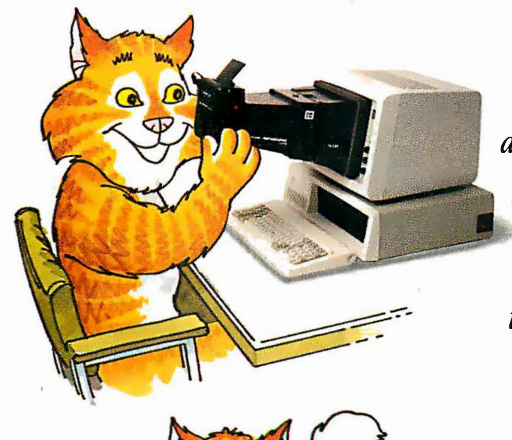
concurrency at all levels where it makes sense, but the overhead must be analyzed realistically. ■

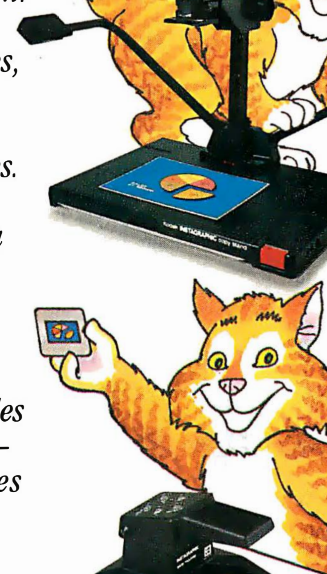
ACKNOWLEDGMENTS
The author would like to acknowledge the contributions of members of the FAIM-1 project: Ken Olum for his collaboration on the instruction-set benchmarks, Ian Robinson and Erik Brunvand for their VLSI CxAM designs, and Al Davis for overall architectural discussions.

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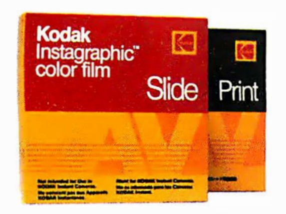
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"Despite the recent press notices, multiuser microcomputers aren't anything new!"

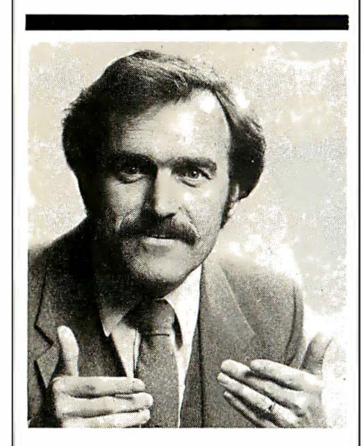
This is the first in a series of discussions with Rod Coleman, President of Stride Micro (formerly Sage Computer) on the 68000 multiuser market and its current environment.

Q: Why do you say that?

RC: "The technology to build a high performance multiuser system has been around for five years. And while some of the leaders in this industry have been pretending that micro multiuser didn't exist, we've been shipping complete systems for nearly three years. The benefits of multiuser are undeniable; it is more cost effective, and offers greater flexibility and utility. But until just recently, the marketing pressure to be compatible instead of being better, has blinded the industry."

Q: What do you mean?

RC: "Well, for example, the Motorola 68000 processor introduced 16/32-bit technology to the personal computer world a long time ago. It was fully capable of meeting high performance and multiuser design requirements in 1980. Instead of this trend taking off, most energy was spent promoting 8088/8086 products that were clearly inferior from a technical point of view. This phenomenon leads me to believe that they will soon rewrite the old proverb: 'Build a better mousetrap and the world will beat a path to your door,' but only if they can find the way through the marketing fog."



"A surprising feature is compatibility. Everybody talks about it, but nobody does anything about it."

Q: Are things changing now?

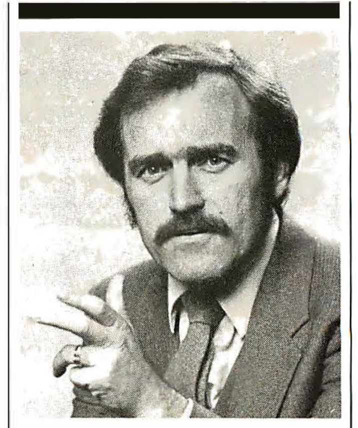
RC: "Yes and no. With the business world starting to take more and more interest in microcomputer solutions, the advantages of a solid multiuser system couldn't be kept hidden forever; companies like ours and a few others were beginning to make a dent. Instead of taking a fresh approach, some of the newest multiuser offerings will probably only give the technology an undeserved black eye! Multiuser is far more than the ability to plug in more terminals. It involves things like machine compatibility, fast processors, adequate memory, large storage capacities, backup features, networking, and operating system flexibility."

Q: Is this what makes the new Stride 400 Series different?

RC: "Exactly. That sounds self-serving, but it's true. Today a number of companies are introducing their first multiuser system. We've been building and shipping multiuser machines for almost three years. We know the pitfalls, we've fallen into some of them. But we have learned from our mistakes."

Q: Give me some examples.

RC: A hard disk is almost mandatory for any large multiuser installation. Yet, backing up a hard disk can be a nightmare if you only have floppies to work with. That's why we've added a tape backup option to all the larger Stride 400 Series machines. It's irresponsible for a manufacturer to market a multiuser system without such backup. Another good lesson was bus design. We started with one of our own designs, but learned that it's important not only to find a bus that is powerful, but also one that has good support and a strong future to serve tomorrow's needs. We think the VMEbus is the only design that meets both criteria and thus have made it a standard feature of every Stride 400 Series machine."



"The marketing pressure to be compatible instead of being better, has blinded the industry."

Q: What are some of the other unique features of the 400 Series?

RC: "A surprising feature is compatibility. Everybody talks about it, but nobody does anything about it. Our systems are completely compatible with each other from the 420 model starting at $2900, through the 440, on to the powerful 460 which tops out near $60,000. Each system can talk to the others via the standard built-in local area network. Go ahead and compare this with others in the industry. You'll find their little machines don't talk to their big ones, or that the networking and multiuser are incompatible, or that they have different processors or operating systems, and so on."

Q: When you were still known as Sage Computer, you had a reputation for performance, is that still the case with the new Stride 400 Series?

RC: "Certainly, that's our calling card: 'Performance By Design.' Our new systems are actually faster; our standard processor is a 10 MHz 68000 running with no wait states. That gives us a 25% increase over the Sage models. And, we have a 12 MHz processor as an option. Let me add that speed isn't the only way to judge performance. I think it is also measured in our flexibility. We support a dozen different operating systems, not just one. And our systems service a wide variety of applications from the garage software developer to the corporate consumer running high volume business applications."

Q: Isn't that the same thing all manufacturers say in their ads?

RC: "Sure it is. But to use another over used-term, 'shop around'. We like to think of our systems as 'full service 68000 supermicrocomputers.' Take a look at everyone else's literature and then compare. When you examine cost, performance, flexibility, and utility, we don't think there's anyone else in the race. Maybe that's why we've shipped and installed more multiuser 68000 systems than anyone else."





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THE LISP REVOLUTION

BY PATRICK H. WINSTON

LISP is no longer limited to a lucky few

A LITTLE MORE than five years ago, a friend from a major computer corporation came into my office to talk about developing artificial-intelligence (AI) packages. "How should we get started?" he asked. My answer was gloomy:

> First, get together a million dollars or so and buy one of Digital Equipment Corporation's (DEC's) big mainframe computers. Next, decide what dialect of LISP to run, choosing from MacLISP, InterLISP, Portable Standard LISP, Franz LISP, and many others. Then try to get a tape from somewhere and find someone who can install it. You'll probably find that the documentation is not particularly complete, and software maintenance will be a problem. And if you bet on the wrong dialect now, changing to another will certainly take a lot of work.

Today, by contrast, I wrote this article using an editor written in LISP. The editor is part of a $500 LISP system that I use on a $4000 personal computer. I wrote and tested a program in the $500 LISP that I will be able to run without change on a supersophisticated, superpowerful Symbolics 3670. Two things have made this progress possible. First, the recent availability of personal computers with 512K bytes of memory, which is enough to learn LISP and to start experiencing the excitement of its applications in AI. Second, Common LISP emerged as the heir apparent to all previous LISP dialects. The same Common LISP program you write on a personal computer can be transferred later to a heftier machine, as needs and resources permit.

Data General, DEC, Hewlett-Packard, LISP Machine, Symbolics Inc., Texas Instruments, and Xerox all sell versions of Common LISP for their own machines, and Common LISP is available for personal computers as well. Suddenly, serious LISP programming is no longer limited to a lucky few.

LISP MEANS SYMBOL MANIPULATION

The reason that LISP is different from most other languages is that LISP focuses on symbol manipulation rather than on numbers. To highlight the difference, I'll lay out some examples of symbol manipulation taken from the Mover program, one that moves toy blocks like those shown in figure 1. Specialized problem-solving procedures inside the Mover program enable it to get rid of obstacles that are in the way. These problem-solving procedures use and maintain information about what each object supports. For example, B3 supports B1 and B4. The Mover program knows this because the symbols B1 and B4 are found in a list obtained from B3 by the get instruction:

```
(get 'B3 'things-supported)
—> (B1 B4)
```

Now suppose we have attached the list of things that B3 supports to a variable called obstacles. LISP's symbol-manipulation primitives allow for quick answers to basic questions:

How many obstacles are there?
```
(length obstacles) —> 2
```

(continued)

Patrick Henry Winston (MIT Artificial Intelligence Laboratory, 545 Technology Square, Cambridge, MA 02139) has a B.S., M.S., and Ph.D. from MIT. He does research on computer learning and directs the Artificial Intelligence Laboratory at MIT.

What's the first obstacle?
(first obstacles) —> B1
Is B1 an obstacle?
(member 'B1 obstacles) —> t
Is B4 the first obstacle?
(eq 'B4 (first obstacles)) —> nil

Note that t is LISP notation for true, and nil is LISP notation for false. Other symbol-manipulation primitives facilitate changes to the list and test to see if it is empty:

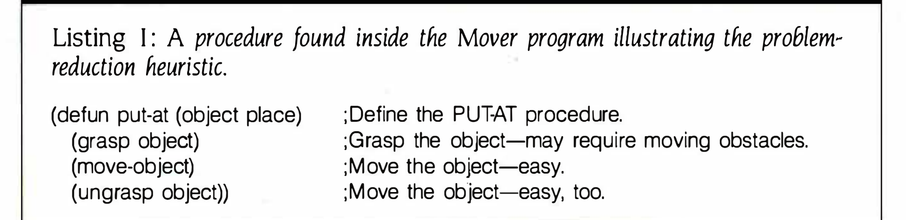
Remove B4 from the list:
(setf obstacles
   (remove 'B4 obstacles)) —> (B1)
Add B7 to the list:
(setf obstacles
   (cons 'B7 obstacles)) —> (B7 B1)
Is the obstacle list empty?
(endp obstacles) — NIL

Once changed, the obstacle list can be reattached to the symbol B3 from which it came:

(setf (get 'B3 'things-supported)
   obstacles)

All these questions and changes are simple, low-level examples of the symbol manipulation for which LISP is famous. Similar symbol-manipulation feats enable the Mover program to keep track of what is done. Mover's history-maintaining procedures contain instructions that examine and change symbolic expressions describing every move. Those symbolic descriptions make it possible to answer questions like: Did you move block B7? How did you move block B7? Why did you move block B7? When did you move block B7?

Thus symbol manipulation enables Mover to exhibit a humanlike, introspective ability to explain itself. Symbol manipulation is so intimately associated with AI, it's no wonder that LISP is the key language used in AI applications.


Listing 1: *A procedure found inside the Mover program illustrating the problem-reduction heuristic.*

```
(defun put-at (object place)   ;Define the PUT-AT procedure.
  (grasp object)               ;Grasp the object—may require moving obstacles.
  (move-object)                ;Move the object—easy.
  (ungrasp object))            ;Move the object—easy, too.
```

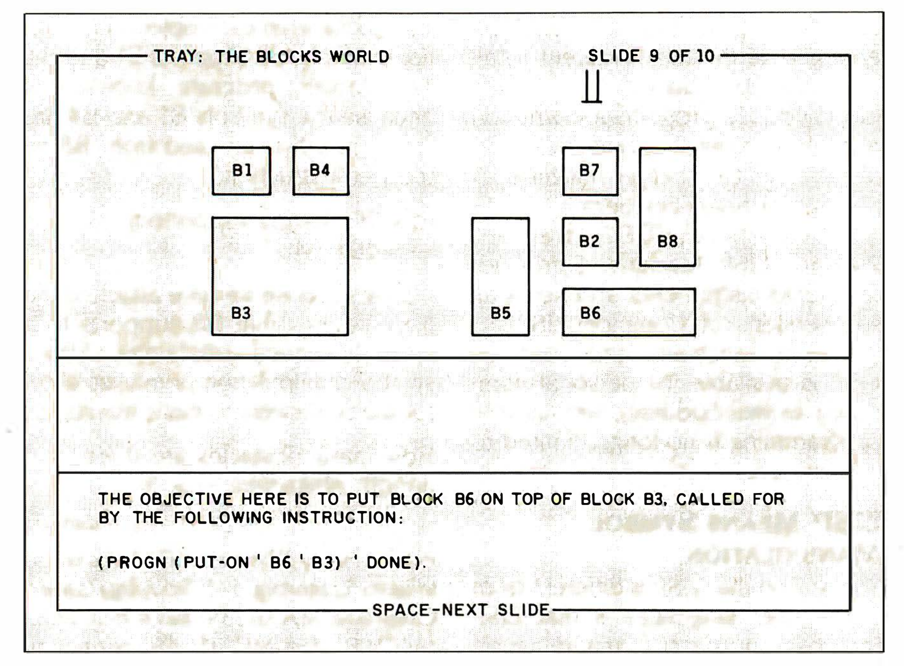


Figure 1: *A picture of the blocks world in which the Mover program operates.*

Computer Professionals Should Know LISP

LISP experts argue endlessly about why LISP remains the primary language for AI and about why it is becoming a language for general-purpose programming as well. Some say LISP's primitives and features explain all. Others claim LISP owes its power to its tradition of interactive programming and powerful debugging tools. Still others cite its simple hierarchy-encouraging procedure-definition mechanism. [*Editor's note: for a short introduction to* LISP, *see* "LISP *for the* IBM *Personal Computer" by Jordan Bortz and John Diamant, July 1984* BYTE, *page* 281.]

Increasingly, LISP is becoming a more generally used language, not strictly limited to applications in AI. Because many of the systems of AI are large, LISP has become a language suited to large-system implementation. For example, it has been used with outstanding success in building the entire operating systems of the LISP machines now offered by a growing number of major companies.

Such successes are one reason why many computer-science educators believe that an understanding of LISP is de rigueur for computer science majors. Another is that LISP has been proven an excellent language for illustrating computing concepts. At MIT, for example, a dialect of LISP called Scheme has been used for years as the primary language in the basic introductory subject on programming languages.

LISP Is Both Old and New

Before you learn any computer language, you should ask if the language is too old to be modern or too new to be mature. What about LISP? Is it too old or too new? Many people are surprised to learn that the history of LISP goes back to the late 1950s, making LISP nearly as old as FOR-

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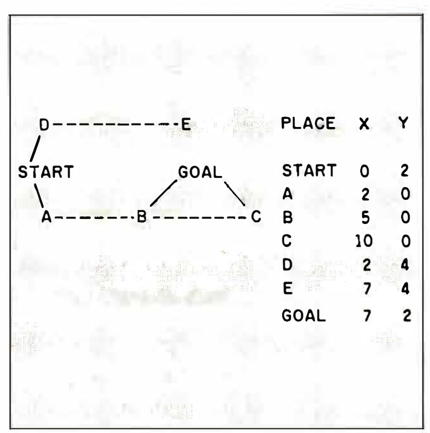
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TRAN. Unlike FORTRAN, however, the LISP of today is much different from the LISP of 25 or even 5 years ago. Why did FORTRAN calcify while LISP continued to evolve vigorously? The principal reason is that FORTRAN was suited to commercial applications early on, whereas LISP was not. LISP requires a lot of memory, and in the days when memory was expensive, there was no commercial purpose served by early standardization of LISP. Consequently, LISP dialects proliferated, LISP innovations thrived, and cross-fertilizations from one dialect of LISP to another kept each about as powerful as any other. Now, however, memory is relatively cheap, which is attracting many commercial users to LISP, thus increasing the need for a standardized LISP for applications and instruction. Fortunately, the 25 years LISP has had to mature means that many new features have been incorporated into the Common LISP standard. Here are some of my favorites:

- a powerful structure-defining primitive that automatically generates procedures for accessing record fields
- a generalized assignment primitive that works for values, properties, arrays, and structures
- a flexible template-filling mechanism that enables complicated expressions to be constructed easily and transparently
- a strong macrocomputer capability that enables users to dream up their own syntax
- a rich variety of argument-passing options, including optional arguments with specifiable defaults as well as arguments associated with parameters by way of key words
- a modern, stream-oriented input/output (I/O) system

PUT-ON
GET-SPACE
MAKE-SPACE
FIND-SPACE
GET-RID-OF
PUT-AT
CLEAR-TOP
GRASP
MOVE-HAND
MOVE-OBJECT
UNGRASP

Figure 2: *Graphical description of how all the procedures in Mover work together.*



PLACE	X	Y
START	0	2
A	2	0
B	5	0
C	10	0
D	2	4
E	7	4
GOAL	7	2

Figure 3: *An example of a maplike net.*

```
(make-rule identify16
  if     ((> animal) is a (> type))
         ((< animal) is a parent of (> child))
  then   ((< child) is a (< type)))
```

Figure 4: *A rule ready for inclusion in a LISP-based animal-recognition system.*

```
Rule IDENTIFY1 asserts  (ROBBIE IS A MAMMAL)
     because  (ROBBIE HAS HAIR)
Rule IDENTIFY5 asserts  (ROBBIE IS A CARNIVORE)
     because  (ROBBIE EATS MEAT)
Rule IDENTIFY9 asserts  (ROBBIE IS A CHEETAH)
     because  (ROBBIE HAS DARK SPOTS)
              (ROBBIE HAS TAWNY COLOR)
              (ROBBIE IS A CARNIVORE)
              (ROBBIE IS A MAMMAL)
Rule IDENTIFY16 asserts  (BOZO IS A MAMMAL)
     because  (ROBBIE IS A PARENT OF BOZO)
              (ROBBIE IS A MAMMAL)
Rule IDENTIFY16 asserts  (BOZO IS A CARNIVORE)
     because  (ROBBIE IS A PARENT OF BOZO)
              (ROBBIE IS A CARNIVORE)
Rule IDENTIFY16 asserts  (BOZO IS A CHEETAH)
     because  (ROBBIE IS A PARENT OF BOZO)
              (ROBBIE IS A CHEETAH)
```

Figure 5: *Output fragment showing how a forward-chaining rule moves from facts to conclusion.*

How to Learn LISP

I think the best way to learn LISP is interactively. There are quite a number of reasons why such interactive learning is good. For instance: It's fun to do on-line puzzles; it's boring to do exercises in a book. It's easy to demystify difficult points by trying things out immediately. It's motivating to watch interesting programs work.

In any case, one factor stands undisputed: LISP programming is fun. Let's look at a few taken from an on-line, interactive instruction package known as the San Marco LISP Explorer. [*Author's note: The San Marco LISP Explorer package is sold by Gold Hill Computers Inc., 163 Harvard St., Cambridge, MA 02139.*] We will examine the Mover blocks-manipulation program, the search program, the rule-based ex-

(continued)

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Compile Time (secs.)	**8.5**	–	–	3.9	108

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Listing 2: A *search program that finds paths through maplike nets such as the one in figure 3.*

```
(defun start-depth (start goal)
  (depth (list (list start))          ;Make a one-partial-path queue.
         goal))                       ;Pass along name of goal place.

(defun depth (queue goal)
  ;;If no other partial paths, quit:
  (if (null queue)
      nil
      ;;Otherwise, if goal found, quit:
      (if (equal goal (first (last (first queue))))
          (first queue)
          ;;Otherwise, expand first partial path
          ;;and add to FRONT of queue:
          (depth (append (expand (first queue))
                         (rest queue))
                 goal)))))

(defun expand (path)
  (let ((reversed-path (reverse path)))
    ;;Turn the new partial paths right way around:
    (mapcar 'reverse
      ;;Get rid of partial paths that close on themselves:
      (remove-if '(lambda (new-path)
                    (member (first new-path) (rest new-path)))
        ;;Make one new partial path for each neighbor:
        (mapcar '(lambda (neighbor) (cons neighbor reversed-path))
                ;;Get neighbors:
                (get (first reversed-path) 'neighbors))))))
```

Listing 3: *The expression-matching procedure in any rule-based expert system must compare expressions and produce a list of pattern-match pairs.*

```
* (match '((> animal) is a (> type))   ;First argument is a pattern.
         '(Robbie is a Cheetah)        ;Second argument is an assertion.
         nil)                          ;Third is a list of prior pattern-match
                                       ; pairs, none in this example.
((animal robbie) (type cheetah))       ;The answer—a list of pattern-matches.
```

Listing 4: A *matcher program for a rule-based expert system.*

```
(defun match (p d matches)
  (cond ((and (endp p) (endp d))          ;Succeed.
         (cond ((endp matches) t)
               (t matches)))
        ((or (endp p) (endp d)) nil)      ;Fail.
        ((equal (first p) (first d))      ;Identical first elements.
         (match (rest p) (rest d) matches)) ;Match the rest.
        ((atom (first p)) nil)            ;Losing atom.
        ((equal (first (first p)) '>)     ;Match > variable.
         (match (rest p) (rest d)
                (shove-value (second (first p))
                             (first d)
                             matches)))
        ((equal (first (first p)) '<)     ;Substitute variable.
```

(continued)

pert system, and the natural-language interface.

Planning in the Blocks World

LISP programs are generally examples of the problem-reduction heuristic; that is, to solve a hard problem you must break it up into simpler subproblems. The problem-reduction heuristic can be seen in the simple Mover program. Listing 1 is a procedure found inside the Mover program that breaks the problem of putting an object somewhere into three subproblems: grasp it, move it, and ungrasp it. Figure 2 is a graphical description of how all of the procedures in Mover work together. LISP encourages the creation of layered programs, like Mover, wherein big problems are broken down successively into smaller and smaller problems.

Searching in the Map World

Search techniques are commonly used in AI to solve problems. Here are some examples:

- finding a route through a highway net
- finding a way to put together a motor
- understanding a written database request
- learning to recognize a plant disease

Abstractly, search problems all amount to finding a way through some sort of maplike net. Figure 3 is a sample of such a net. The goal is close to place E, but there is no direct connection; E is a dead end. There are two ways to go from B to the goal: directly, and indirectly, through C. Listing 2 shows a page of LISP defining a search program that finds paths through these maplike nets. Although you won't understand much of the program if you don't know LISP yet, you may enjoy looking at its overall structure and simplicity. With a little more effort, you can define a search

(continued)



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```
        (match (cons (pull-value (second (first p) matches)
                     (rest p))
               d
               matches)))))
```

This matcher happens to use two auxiliary procedures:

```
(defun pull-value (variable a-list)
  (second (assoc variable a-list)))

(defun shove-value (variable item a-list)
  (append a-list (list (list variable item))))
```

Listing 5: *A program that matches sentences against a suitable representation of semantic grammars and activates the appropriate search procedure.*

```
(record question
      ((branch ((parse present)
                (branch (THE (parse attributes) OF (parse tools)
                  (parse-result-if-end
                    (report-attributes attributes tools)))
                ((parse tools) S (parse attributes)
                  (parse-result-if-end
                    (report-attributes attributes tools)))))
      (HOW MANY METERS IS (parse tool1) FROM (parse tool2)
        (parse-result-if-end
          (report-distance tool1 tool2)))
      (IDENTIFY (parse tools)
                (parse-result-if-end
                       (report-identity tools)))
      (COUNT (parse tools)
             (parse-result-if-end
                    (report-number tools))))))
```

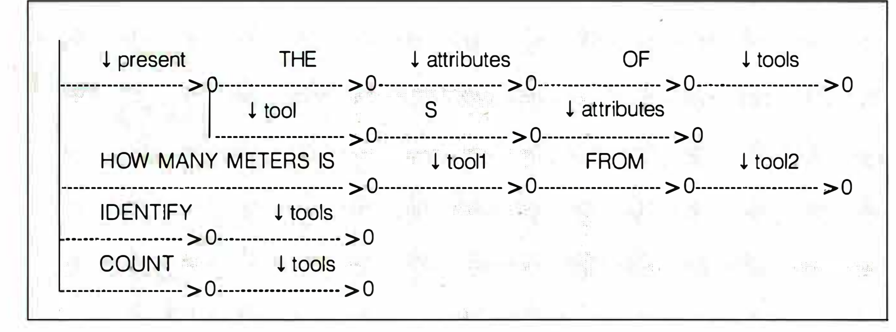


Figure 6: *The top level of a semantic grammar capable of handling queries about the color, weight, length, and position of some tools.*

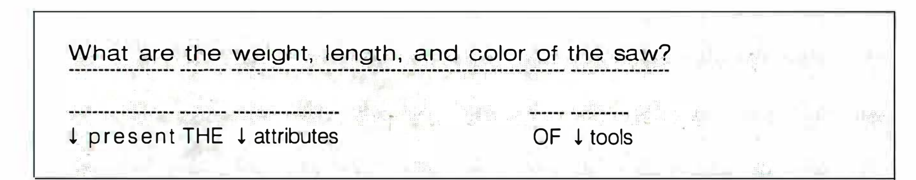


Figure 7: *An example of a question that matches the top level of the semantic grammar in figure 6.*

procedure that finds the guaranteed-shortest path.

ANALYSIS IN THE ZOO WORLD

Rule-based expert systems are the hottest thing in the commercialization of AI. All of them are built on the idea that some kinds of knowledge can be reduced to simple rules. Figure 4 shows one rule that is ready for inclusion in a LISP-based animal-recognition system, which expresses the fact that an animal's children are animals of the same kind. LISP does not have any built-in primitives that handle such rules, but it is a splendid language in which to embed a rule-exploiting program. LISP's symbol-manipulating power is well suited to the task of examining the symbols that make up a rule, comparing them to the symbols that make up the existing facts, and reacting accordingly. One kind of rule-exploiting program is a forward-chaining rule interpreter, which is a program that uses rules to move forward from facts to conclusions. Figure 5 is an output fragment showing what such a program does with facts about Robbie, knowledge about the relationship between Robbie and Bozo, and a few rules. There is always an expression-matching procedure buried inside any rule-based expert system like the animal-identification procedure. While the entire system is too lengthy to show, the matcher is short and straightforward. Its task is to compare expressions and to produce a list of pattern-match pairs, as shown in listing 3. Listing 4 is the matcher program.

INTERACTION IN THE TOOL WORLD

The pattern matcher shown previously is not just an important part of a rule-based system. It is also just about all you need to make the famous Doctor program, the one that pretends it is a psychiatrist responding with apparent sympathy as you pour your heart out over family traumas. More importantly, the pattern matcher has a family resemblance to natural-lan-

(continued)



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guage interface programs built on what is called a semantic grammar. Basically, a semantic grammar is a model of what can be said in tightly constrained conversations about a narrow database. Suppose that you are interested in the color, weight, length, number, and position of some tools. The natural queries are:

- Identify the hammers.
- Count the red screwdrivers.
- Show me the color of the wrenches.
- Present the small red screwdriver's weight.
- What is the length and weight of the large saw?
- How many meters is the small red screwdriver from the big blue screwdriver from the big blue one?

The top level of a semantic grammar capable of handling all these queries is shown in figure 6. A semantic-grammar interpreter finds paths through such a net using input sentences as a guide. Each branch marked with a > symbol requires traversal of a subnet. Each complete path from the entry to an exit is associated with its own data-searching procedure. For example, the sentence in figure 7 matches the topmost path in the top-level net. Three subnets are traversed in addition to the top-level net. Once again, LISP's symbol-manipulating power makes it easy to write a program that both matches sentences against a suitable representation of semantic grammars and activates the appropriate search procedures. Listing 5 shows what such a representation looks like when it is rendered in LISP-oriented notation.

CONCLUSION

We really don't need any new examples to demonstrate why professionals need to know about LISP. The examples presented are all elementary, but they indicate the sorts of things done by their bigger brothers. LISP is the foundation for expert systems of all kinds, many of which have progressed far beyond the simple rule-based paradigm. LISP is the language for most natural-language development efforts. Indeed, LISP is the language of choice for most people working in AI—supporting work that includes learning, instruction, speech, vision, robotics, and all sorts of reasoning. ■

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8085	199.50	500.00	199.50	199.50	199.50
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68020	399.50	750.00	399.50	399.50	399.50
68000,08,10	299.50	750.00	299.50	299.50	299.50
6800,02,08	199.50	500.00	199.50	199.50	199.50
6801,03	199.50	500.00	199.50	199.50	199.50
6804	199.50	500.00	199.50	199.50	199.50
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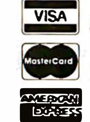
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Inquiry 4

THE CHALLENGE OF OPEN SYSTEMS

BY CARL HEWITT

Current logic programming methods may be insufficient for developing the intelligent systems of the future

SYSTEMS OF INTERCONNECTED and interdependent computers are qualitatively different from the relatively isolated computers of the past. Such "open systems" uncover important limitations in current approaches to artificial intelligence (AI). They require a new approach that is more like organizational design and management than current approaches. In this article we'll take a look at some of the implications and constraints imposed by open systems.

Open systems are always subject to communications and constraints from outside. They are characterized by the following properties:

• *Continuous change and evolution.* Distributed systems are always adding new computers, users, and software. As a result, systems must be able to change as the components and demands placed upon them change. Moreover, they must be able to evolve new internal components in order to accommodate the shifting work they perform. Without this capability, every system must reach the point where it can no longer expand to accommodate new users and uses.

• *Arm's-length relationships and decentralized decision making.* In general, the computers, people, and agencies that make up open systems do not have direct access to one another's internal information. Arm's-length relationships imply that the architecture must accommodate multiple computers at different physical sites that do not have access to the internal components of others. This leads to decentralized decision making.

• *Perpetual inconsistency among knowledge bases.* Because of privacy and discretionary concerns, different knowledge bases will contain different perspectives and conflicting beliefs. Thus, all the knowledge bases of a distributed AI system taken together will be perpetually inconsistent. Decentralization makes it impossible to update all knowledge bases simultaneously. This implies that it is not even possible to know what kinds of information are contained in all the local knowledge bases in the system at any one time. Systems must be able to operate in the presence of inconsistent and incomplete knowledge bases.

• *Need for negotiation among system components.* In a highly distributed system, no system component directly controls the resources of another. The various components of the system must persuade one another to provide capabilities. Consequently, a distributed AI system's architecture must support a mechanism for negotiation among components.

• *Inadequacy of the closed-world assumption.* The closed-world assumption is that the information about the world being modeled is complete in the sense that exactly those relationships that hold among objects can be derived from the local information possessed by the system. Systems that depend on the closed-world assumption make use of the principle that they can find

(continued)

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all existing instances of a concept by searching their local storage. At first glance it might seem that the closed-world assumption, almost universal in the AI literature, is smart because it provides a ready default answer for any query. Unfortunately, the default answers provided become less realistic as open systems increase in size and less of the information is available locally.

Continuous growth and evolution, arm's-length relationships, inconsistency among knowledge bases, decentralized decision making, and the need for negotiation are interdependent and necessary properties of open systems.

Parallel Computation in Open Systems

The theory of recursive functions (e.g., Turing machines) is based on a batch-processing model of computation. Output is obtained from a recursive function when it finally halts. Open systems require a theory of computation in which processing might never halt, may be required to provide output while still in operation, and can accept input from sources not anticipated when the computation began.

Asynchronous parallel computer systems make use of a two-input, two-output computing element called an *arbiter*. Arbiters are the fundamental hardware primitives that make parallel asynchronous computing different from sequential synchronous computing. Arbiters make decisions for which there is no logical justification (proof) because the decision cannot be predicted from knowledge of the structure of the computing system and its input. In a very fundamental sense, arbiters are not equivalent to Turing machines (see reference 3). Figure 1 shows an arbiter with inputs x and y and outputs x' and y'.

An arbiter decides the order in which it receives requests. Thus, if inputs x and y are asserted at about the same time, the result will eventually be one of the possibilities shown in figure 2.

The output of an arbiter is *not* a logical function of its input, in the sense that it is not a simple Boolean function, because the dimension of time enters into the semantics of arbiter modules in a fundamental way. However, the *feasible* sets of outputs can be described in logic using the *subsequently* relation (see reference 1):

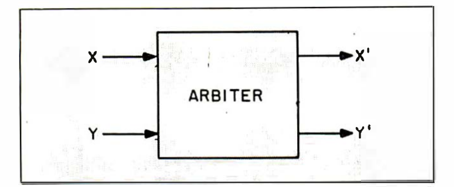


Figure 1: *An arbiter, with inputs x and y and outputs x' and y'.*

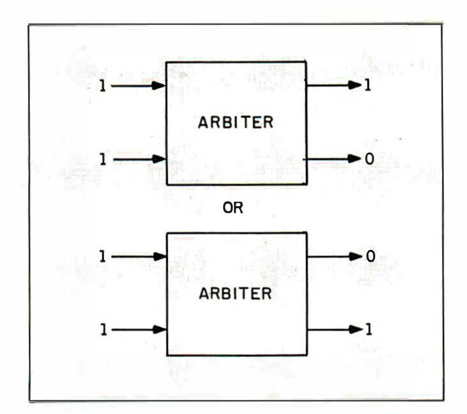


Figure 2: *Given that the inputs to the arbiter are asserted almost simultaneously, the resulting output will be one of the above two cases.*

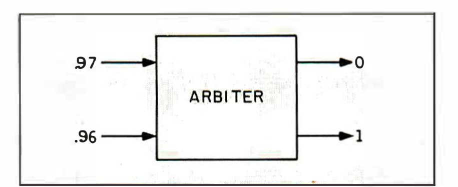


Figure 3: *In practice, the inputs to an arbiter are analog signals varying between 1 and 0.*

(x=1 and y=1) *subsequently*
(or
(x'=0 and y'=1)
(x'=1 and y'=0))

Logic cannot be used to determine which particular eventuality will occur. Systems with arbiters are not equivalent to a nondeterministic Turing machine, since an arbiter can require an unbounded amount of time to make a decision (possibly while other computations are taking place). If a nondeterministic Turing machine is required to make a decision, there is a bound on the amount of time it can take, and this bound is determined before it starts. Each individual choice of a nondeterministic Turing machine takes one step.

In practice, the inputs to an arbiter are analog signals that vary continuously between 0 and 1. For example, if the actual inputs to an arbiter were .97 and .96, then the output might be as shown in figure 3.

The arbiter has only digital outputs (0s or 1s) even though the input is analog. It makes a definite digital choice out of the analog quantities of time and its two inputs. Because of the continuous nature of time and the analog nature of the input, an arbiter cannot be strictly modeled as a nondeterministic-state machine.

In a parallel computation, arbiters are used repeatedly so that the number of possibile outcomes grows exponentially with time. Thus, the actual operation of a parallel computer system cannot be determined logically by the inputs to the system. The indeterminacy of the arbiters used in open computer systems results in their making decisions that cannot be proved from knowledge of structure of the computing system and its input.

Decisions Justified by Agreements

The electronic-banking system is a good example of an open system. You're probably familiar with it through the use of automated teller machines that enable you to withdraw cash thousands of miles from where you opened an account. Teller machines are continually being added to the system.

Decisions about which transactions to honor are justified on the basis of an agreement between the bank and its depositors. Often an agreement will provide that the bank does not have to honor a withdrawal if there are insufficient funds present in the

account when the withdrawal is requested. The withdrawal would be refused even though it might be covered by subsequent deposits.

The decisions of which withdrawals not to honor cannot be deduced from complete information about the structure of the bank's computers and the input from the teller machines. Thus, the decision whether or not to honor a withdrawal is not subject to logical proof. For example, suppose Account 1 has a balance of $1000, Account 2 has a balance of $2000, and they share a common reserve account with a credit limit of $3000. If two electronic withdrawals of $4000 each are attempted at about the same time from both Account 1 and Account 2, then one of the attempts will be refused and the other one will be honored, though it is impossible to deduce which one will be honored and which one refused.

The above example shows how a decision of an open system can be justified even though it does not follow from any proof. Instead, the decision is justified by an agreement to act in certain ways. We see a divergence between the theories used in the construction of open systems and their operation. Theory informs practice; e.g., the design of the banking mechanism is based on a financial theory. However, the financial theory does not determine the actual operations of the bank accounting system. The operation of the bank accounts is determined by the order in which asynchronous events occur inside the system. Each performance of a complicated open system is unique.

This illustrates the divergence between classic recursive-function theory and theories needed to model open systems. (For a further discussion of the mathematical semantics needed to model the behavior of open systems, see references 1 and 3.)

Exploration vs. Search

Searching in problem spaces is the traditional AI framework. Problem spaces and problems have been defined as follows (see reference 16):

Problem Space: A problem space consists of a set of symbolic structures (the *states* of the space) and a set of *operators* over the space. Each operator takes a state as input and produces a state as output, although there may be other inputs and outputs as well. The operators may be partial, i.e., not defined for all states. Sequences of operators define *paths* that thread their way through sequences of states.

Problem: A problem in a problem space consists of a set of *initial* states, a set of *goal* states, and a set of *path constraints*. The problem is to find a path through the space that starts at any initial state, passes only along paths that satisfy the path constraints, and ends at any goal state.

A good example of a problem space is that of the game of chess:

1. *Initial state*: chess pieces in starting position
2. *Operations*: legal moves
3. *Goal states*: checkmate, stalemate, etc.

I claim that searching through problem-solving spaces provides a narrow foundation for the analysis and synthesis of intelligent systems. The perspective must be broadened to include *exploration* that goes beyond search. An excellent perspective on some of the differences between search and exploration is provided by the means used to explore and develop the North American continent.

1. *Initial state*: There was no well-defined initial global state of the

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North American continent in the middle 1600s. Leif Ericson and Christopher Columbus had led some early probes, but the information was fragmentary, dispersed, and self-contradictory.

2. *Operations*: The set of operations used to explore the continent was not defined in advance. Instead, it was improvised dynamically and interactively in the course of initial probes. Furthermore, the explorers operated *in parallel* so that there is no path of states of the continent that adequately explains how it was explored. That is, the continent was not explored by finding a single path through a space of states. Exploration of the North American continent can be better modeled as a partial order of causally linked historical events than as a problem space.

3. *Goal states*: There was no set of immutable global goal states for the continent that the explorers set out to achieve. Rather, the explorers' goals evolved with the exploration methods as the exploration proceeded.

Searching problem spaces is limited mainly in its applicability to artificial domains like chess and mathematical theorem proving. It is not very adaptable to the hurly-burly of solving problems involving interaction with the physical world. Problem spaces do not provide sufficient flexibility to represent the problem-solving processes of communities because of the attempt to represent the problem solving of individual actors as a single global state. This limitation of problem spaces is closely related to the inadequacies of the Turing machine as a model of asynchronous distributed systems. Problem solving in open systems is more analogous to the exploration of North America than the playing of games like chess.

PLANNER

Planner was one of the first AI programming languages to support goal-oriented problem solving without an externally specified problem space. It was based on the following principles (see reference 6):

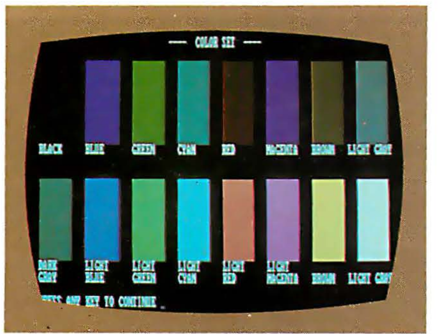
- *Accessibility*: Planner aims for a maximum of flexibility so that whatever knowledge is available can be incorporated into the problem-solving process even if it is fragmentary and heuristic.
- *Pattern-directed invocation*: Procedures in Planner can be invoked by patterns of what they are supposed to accomplish. Suppose that we have a stopped sink. One way we could try to solve the problem would be to know the name of a plumber whom we could call. An alternative that is more analogous to pattern-directed invocation is to advertise the fact that we have a stopped sink and the qualifications needed to fix it. In Planner this is accomplished by making the advertisement (i.e., the pattern that represents what is desired) into a goal.
- *Procedural interpretation of logical statements*: One basic idea behind Planner is to exploit the duality that we find between certain imperative and declarative sentences. Consider the statement (implies A B). The statement is a perfectly good declarative. In addition, it can also have certain imperative uses for Planner. It can say that we might set up a procedure that will note whether A is ever asserted and if so to consider the wisdom of asserting B in turn. Furthermore, Planner permits us to set up a procedure that will watch to see if it is ever our goal to try to deduce B and if so whether A should be made a subgoal. Exactly the same observation can be made about the contrapositive of the statement (implies A B). Statements with universal quantifiers, conjunctions, disjunctions, etc., can also have both declarative and imperative uses. Planner theorems are used as imperatives when executed and as

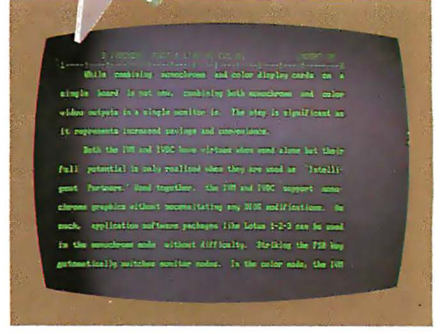
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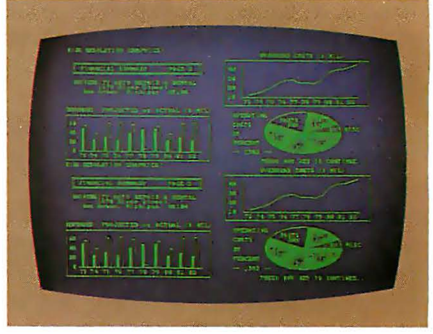
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declaratives when used as data.

Planner represented an advance over the "uniform proof procedures" of resolution theorem-proving systems then current. The design for Planner was implemented by Sussman, Winograd, and Charniak (see references 5, 23). Winograd used it to implement his interactive natural-language program, SHRDLU, for a world with simulated toy blocks (see reference 27).

In order to understand how procedural interpretation works, consider this logical statement:

(For All *x* ((man *x*) implies (mortal *x*)))

The implication has two parts: the antecedent (man *x*) and the consequent (mortal *x*). It says: For every *x*, if *x* is a man, then *x* is mortal. Logical rules of inference permit certain deductions from the above statement. For instance, that Socrates is mortal can be derived from the premise that Socrates is a man as follows:

(Man Socrates)

(Mortal Socrates)

I proposed that logical implications like "all men are mortal" could be interpreted as procedures in a programming language. One interpretation, the *belief-invoked* interpretation (called the "antecedent interpretation" in Planner), provides that when the belief that *x* is a man is held, then the belief that *x* is mortal can be logically derived. We can express this as follows:

```
(when (belief (man x)) do
      (believe (mortal x)))
```

Another interpretation, the *goal-invoked* interpretation (called the "consequent interpretation" in Planner), provides that from the goal that *x* is mortal, the subgoal that *x* is a man can be logically derived:

```
(when (goal (mortal x)) do
      (show (man x)))
```

The ideas in Planner have been generalized and perfected in subsequent artificial-intelligence programming languages. However, by themselves they do not address the needs of open systems.

Logic Programming

Logic programming has been proposed by some as the programming paradigm for the future (see reference 12). Let's focus on limitations that are inherent in the enterprise of attempting to use logic as a programming language for dealing reliably with empirical knowledge and interacting with the physical world. The remarks in this section continue a debate that begins with the genesis of AI. I recommend that interested readers consult the appendix to Marvin Minsky's frames paper (see reference 15) and the subsequent analysis of David Israel (see reference 8).

Logic programming must be based on logic. But what is logic? First-order logic, with its well-defined semantics and syntax, is the basis claimed by most of those who call themselves logic programmers. In part, the confidence of logic programmers is based on the fact that first-order logic augmented with set theory has proved to be a good foundation for mathematical semantics.

Omega-order logic is an extension to first-order logic that allows quantification over predicates and functions. It has advantages over first-order logic in that it includes the full lambda calculus as a sublanguage and has arbitrary powers of abstraction. When certain technical problems having to do with Russell's Paradox have been dealt with, omega-order logic may be the preferred logical language (see reference 19). Therefore, we should consider it to be in the mainstream of logic programming. Experts have argued that the merits of other logics can be found in first-

(continued)

order logic (see references 14 and 26), so the analysis in this article is confined to first-order logic without loss of generality.

The Inconsistency Problem

I make the following claim, which I call the Conjecture of Inconsistency: The axiomatizations of the human knowledge of all physical systems are uniformly inconsistent in practice.

I've used the term *conjecture* because the above claim is in principle impossible to prove rigorously, easy to disprove by counterexample, and has a preponderance of evidence in its favor. The reasons for the inconsistency have to do with the dispersed asynchronous nature of human knowledge, including the following factors:

- *Environmental context*: The physical system being axiomatized is related to various other physical systems. For example, a diseased kidney is often related to a diseased heart. Knowledge of the kidney cannot be separated from knowledge of the heart.
- *Spatiotemporal context*: A physical system is situated in space and time. Knowledge of the physical system comprises knowledge of its history and mode of production.
- *Terminological context*: The predicates used in the axiomatization of the properties of a physical object are always somewhat problematic in practice. For example, specifying in practice what it means for a physical table to be flat raised many problematic issues.
- *Evidential context*: It is impossible to separate what we know about a physical object from how we came to know it. Axiomatization of the methods by which the axiomatized knowledge came to be known further enlarges the axiomatization.

The DEC System-20 is a good case in point. In the first place, observe that the DEC System-20 is an extremely simple system in comparison with, say, the human kidney. Furthermore, the DEC System-20 is an artificial human construct that was designed to be consistent with some simple requirements. Nevertheless, despite the best efforts of software engineers, the formal description (axiomatization of documentation and code) of the DEC System-20 remains inconsistent. There are inconsistencies in the documentation as well as inconsistencies between the documentation and the code. Although inconsistencies are continually being removed from the system, the experience is that more inconsistencies are always found immediately.

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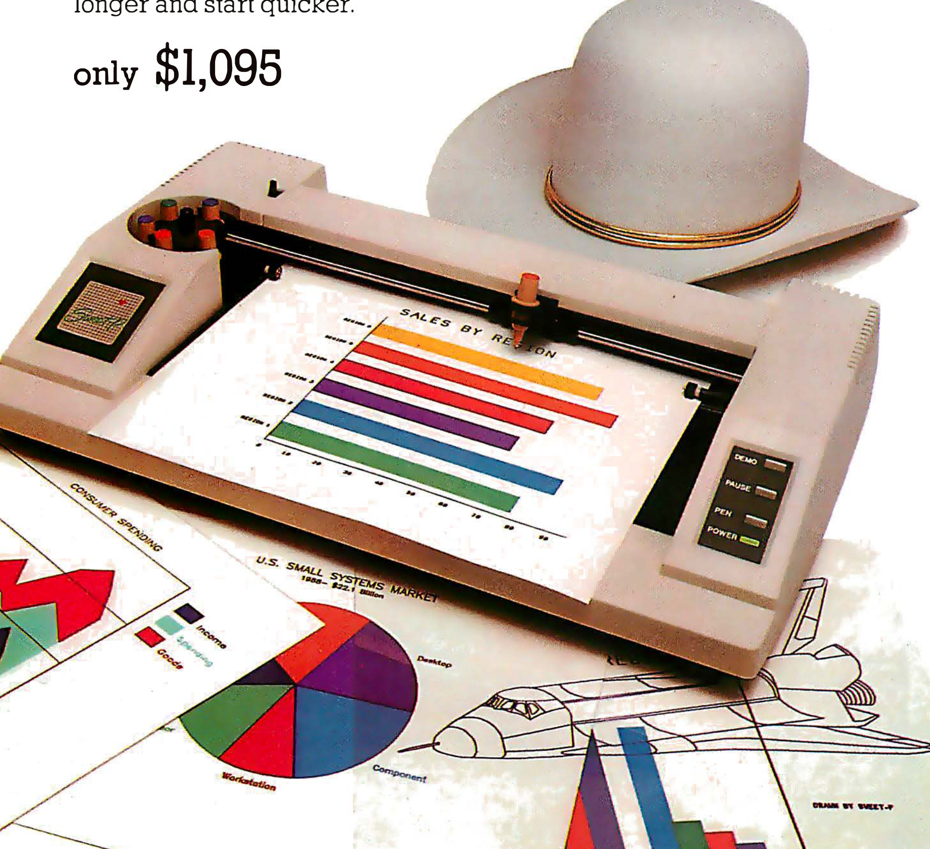
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of making the description of the DEC System-20 consistent. We would have to control the process by which the system grows and evolves. In particular, we would have to handle all changes to the documentation and code in face of the following external requirements:

- Bugs in both the code and documentation must be fixed
- New functions must be incorporated to meet the customers' changing needs
- The system must accept changing interfaces to other systems such as peripherals and networks

There is no way to prove that the process by which the DEC System-20 evolves will result in new releases with consistent formal descriptions. An axiomatization of the code and documentation of even a system as simple as the DEC System-20 is, in practice, inconsistent despite enormous efforts made to achieve consistency.

A second claim I make is that the axiomatizations of the human knowledge about any physical systems will forever be inconsistent. I call it the Conjecture of Perpetual Inconsistency: Removing some inconsistencies from an axiomatization of the human knowledge about a physical system leaves an axiomatization which is nevertheless inconsistent.

MESSAGE-PASSING SEMANTICS

Consideration of the previous claim suggests that we need to examine how logic treats inconsistency. Inconsistencies have some important implications of the utility of logic programming as a foundation for intelligent systems. The logical view of inconsistent theories is clear: They are meaningless because they correspond to no possible world. The logical account of meaning is too stringent for nontrivial empirical systems because inconsistent beliefs and descriptions are not meaningless. Inconsistency is inherent in the enterprise of expressing the human knowledge of physical systems. A theory of meaning that maintains that inconsistent descriptions are meaningless is not directly applicable to problems of empirical knowledge.

In model theory, the meaning of a sentence is determined by the models that make it true (see reference 24). For example, the conjunction of two sentences is true exactly when both of its conjuncts are true. Truth-theoretic semantics assumes that it is possible to give an account of truth in itself, free of interactional issues, and that the theory of meaning can be based on such a theory of truth.

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Message-passing semantics takes a different perspective on the meaning of a sentence: It takes the meaning of a message to be the effect it has on the subsequent behavior of the system. In other words, the meaning of a message is determined by how it affects the recipients. Each partial meaning of a message is constructed by a recipient in terms of how it is processed (see reference 12). At a deep level, understanding always involves categorization, which is a function of interactional (rather than inherent) properties using the perspective of individual viewpoints (see reference 13). Meaning is thus fundamentally interactional. The meaning of a message is open-ended and unfolds indefinitely far into the future as other recipients process the message. According to message-passing semantics, meaning is communication-based, not logic-based.

Need for Due-Process Reasoning

In the presence of conflicting information and contradictory beliefs, logical proof is inadequate as a reasoning mechanism. Instead we need *due-process reasoning* that investigates different sides of beliefs, goals, and hypotheses that arise.

Consider the following hypothesis to illustrate due-process reasoning: "Nixon was guilty of destruction of evidence in the Watergate case by erasing a portion of a tape recording." One possible approach in logic programming is to gather evidence in favor of the hypothesis and attempt to fashion the evidence into a logic proof (perhaps augmented with "certainty factors" or "default assumptions"). The other approach is to use "negation as failure" to conclude that the hypothesis is false because it cannot be proved from the available knowledge. Both of the approaches are inadequate in this case. No matter how much evidence is produced and analyzed, logical proof (either for or against Nixon's guilt) is unbalanced because it presents only one side of the case in the form of a proof. Using "negation as failure" to draw conclusions from the inability to construct such a proof is equally limited. A balanced approach requires debate between differing positions and weighing presented evidence. Debates are not structured in the same way as logical proofs.

Due-process reasoning is the process of collecting and analyzing the evidence and arguments presented by all interested parties. *Advocates* collect evidence and organize arguments in favor of the hypothesis. In parallel, *skeptics* collect evidence and organize arguments against the hypothesis. Then a debate is conducted on grounds for deciding the case in terms of *motive* and *ability*. The ques-

tion of motive is whether Nixon thought that he would benefit by erasing the tape. The question of ability is whether he could have erased the tape. Both advocates and skeptics *recursively* make use of due-process reasoning while investigating, organizing, and presenting their cases. The advocates and skeptics operate interdependently in collecting evidence (through discovery processes and disclosure requirements) as well as interacting by debating each others' cases in a decision-making process that is fundamentally different from logical proof.

PROLOG

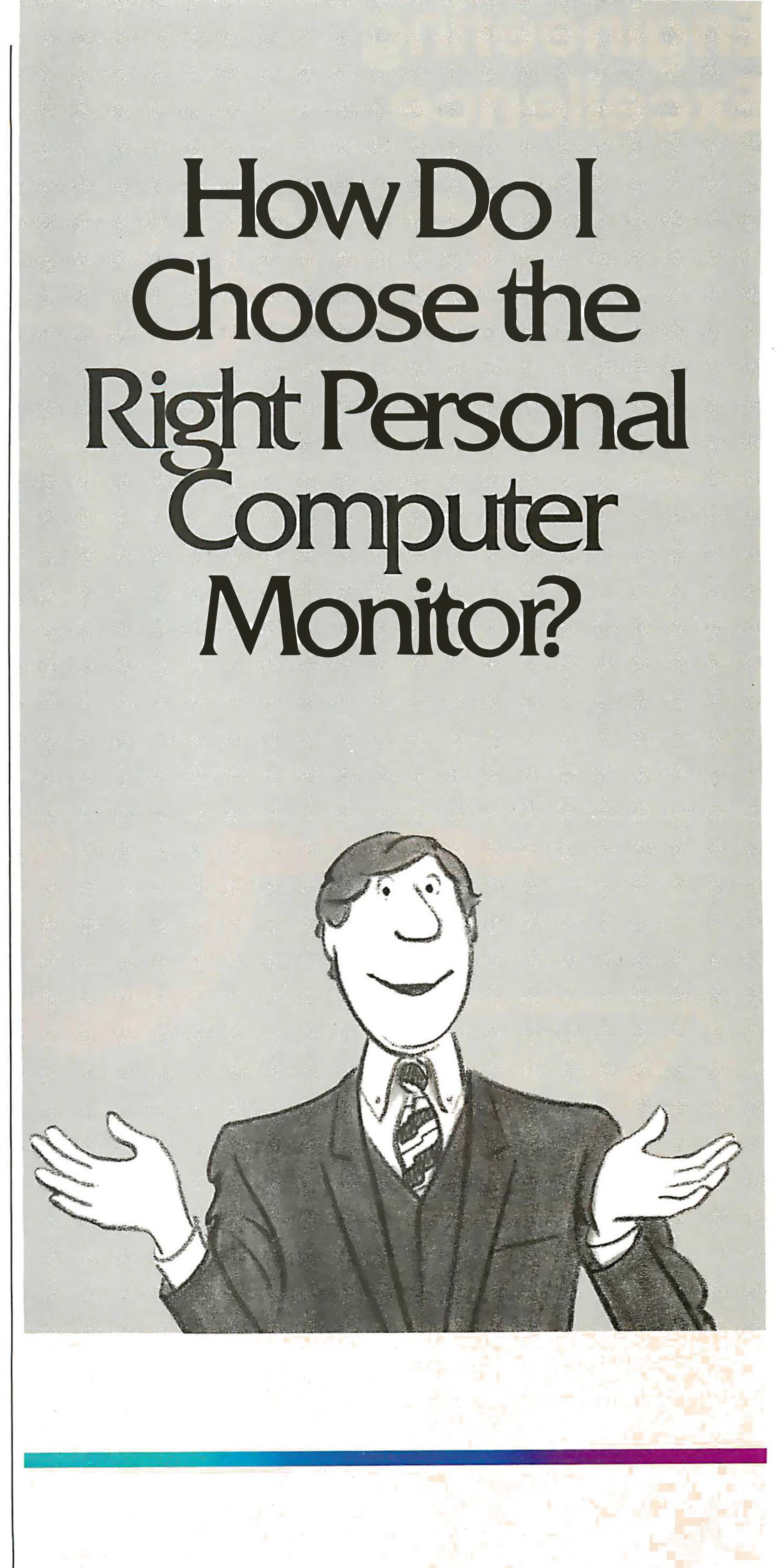
Advocates of logic programming initially developed a programming language called Prolog that was based on the goal-invoked procedural interpretation of implication discussed earlier in the section on Planner (see reference 11). The example discussed earlier to the effect that "In order to show that *x* is mortal, establish a subgoal to show that *x* is a man" is written in Prolog as:

mortal (*x*) :– man (*x*)

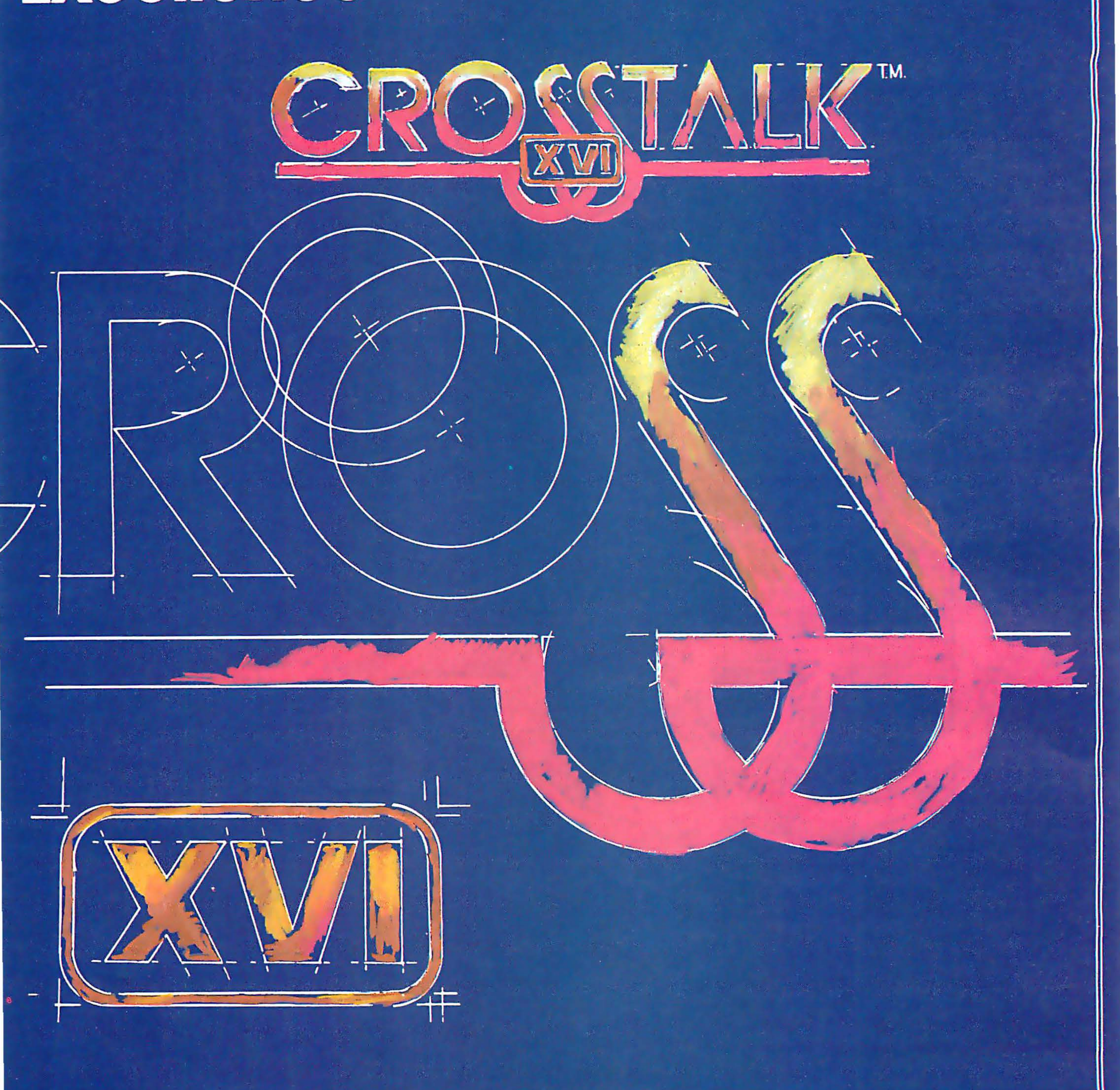
The original Prolog was a much simpler language than Planner, which was a considerable advantage in terms of pedagogy and ease of implementation. But now Prolog, like the Planner-like languages before it, has fissioned into incompatible dialects based on the procedural interpretation of logic, pattern-directed invocation, message-passing theory, and description systems (see references 4, 9, and 12).

In addition to the general limitations of logic programming discussed earlier, Prolog has some idiosyncratic weaknesses all its own. The closed-world assumption is the hypothesis that the locally available knowledge is complete; i.e., if a proposition does not follow from the local knowledge base, then it is assumed to be false (see reference 18). Planner could make use of the closed-world assumption using its ability to conditionalize a plan (theorem) on the exhaustive

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failure to establish a goal. In fact, Winograd made strong use of the capability in SHRDLU. Influenced by Planner, Prolog went much further and adopted a very strong form of the closed-world assumption as a basic postulate of the programming language in incorporating *negation as failure*. (Relational database systems make use of a similar strong hypothesis: If an entry is not found in a relational table, then the relationship is false.) The strong use of the closed-world assumption in Prolog is incompatible with the need in open systems to allow for the open-ended incremental introduction of new beliefs and objects.

INFORMATION-PROCESSING PRINCIPLES FOR THE FUTURE

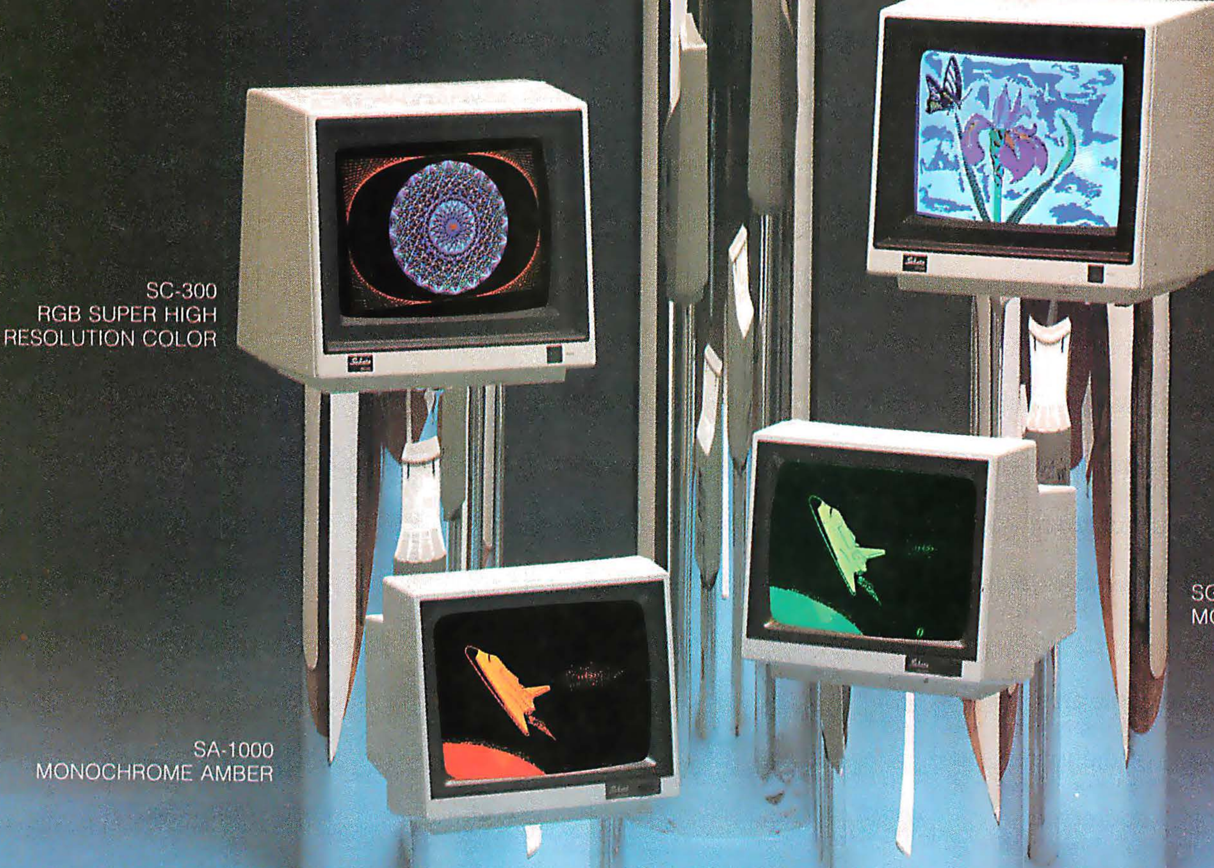
The term *reflection* has been much discussed in the current AI literature (see references 2, 4, 7, 22, and 26). It is universally conjectured that reflective problem capabilities will be important to improving machine problem-solving capabilities. However, a danger is developing that the important problems will be neglected unless reflective problem solving is taken to encompass the following *minimum* capabilities:

- *History of its own behavior*: What did you do then?
- *Representation of its own information-processing procedures*: How do you make decisions?
- *Knowledge of the relationship between its previous behavior and current procedures*: What would you do differently and why?
- *Representation of its procedures for interacting with the external world*: How do you control things?

The current state of the art in implementing reflective systems is extremely primitive. Many of the issues and questions itemized above have not yet been properly addressed.

Besides reflective problem solving, other principles should be adopted in constructing reliable systems that meet the needs of open systems.

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SC-100
COLOR COMPOSITE
SC-200
RGB HIGH
RESOLUTION COL
SC-300
RGB SUPER HIGH
RESOLUTION COLOR
SG-1000
MONOCHROME GREEN
SA-1000
MONOCHROME AMBER

• *Serendipity*: It is not critical whether the system learns of a result before it can be used in a problem-solving task or after work has commenced on the task.
• *Pluralism*: There is no central arbiter of truth in the system.
• *Accessibility*: All knowledge of the system (including its own procedures) should be able to be applied to any problem.
• *Parallelism*: The system should be able to mobilize its full resources in parallel instantiations for different aspects of large-scale problems.
• *Due-process reasoning*: The system collects and debates alternatives to decide among beliefs and goals.
• *Reflection in practice*: Knowledge (including self-knowledge) should inform practice, and practice should modify hypotheses, beliefs, and goals.
• *Reasonableness*: The system should perform efficiently in the face of conflicting information and inconsistent beliefs.

CONCLUSIONS

In practice, the human knowledge of a physical system cannot be consistently axiomatized. Every physical system is open in the sense that it is embedded in a larger physical environment with which it interacts asynchronously. In general, open systems are not totally in control of their fate. In contrast, closed systems (like Peano arithmetic and point-set topology) are exactly characterized by rules and laws.

Proponents of logic programming have maintained that it is a suitable basis for all programming and is the programming paradigm for the future. Logic programming has some fundamental limitations that preclude its becoming a satisfactory programming methodology. It is inadequate for the needs of open systems because it is based on logical operations instead of communication primitives and logical reasoning instead of due-process reasoning. Decisions in open systems are justified by agreements to act in certain ways. Justification by agreement stands in contrast to justi-

(continued)

Inquiry 385 for Dealers. Inquiry 386 for End Users.

fication by logical proof; interaction with the physical world involves dealing with conflicting and contradictory information in a way that does not fall within the scope of decision making by logical proof. Prolog also suffers from the limitation of "negation as failure," restricting it to a closed-world assumption that is incompatible with the nature of open systems.

We need foundations for intelligent systems based on principles of commutativity, pluralism, accessibility, reflection in practice, and due-process reasoning. Logical reasoning is a useful module in the repertoire of an intelligent system, but it is not the whole show. ■

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Suchman at the AAAS session. Allen Newell took the time to give me an overview of some of the aspects of his recent work on foundations in July 1984.

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VISION

BY DANA H. BALLARD AND CHRISTOPHER M. BROWN

Biology challenges technology

VISION AND MOTOR CONTROL are such common capabilities in the animal kingdom that we do not usually associate them with intelligence. Yet vision has always been a paradigm problem for artificial intelligence (AI), since it is mysteriously difficult. Technology has mounted many responses to the biological challenge of reliable, versatile, real-time vision systems, but so far the resulting industrial systems only work in specialized settings (or domains). These systems are routinely used to inspect integrated circuits and manipulate parts but cannot be used outside of these limited contexts. For example, the systems' image input is binary (black and white), not the full gray-scale range provided by an input device such as a TV camera. Attaining such an image calls for carefully engineered lighting and imaging conditions. Also, to attain the necessary speed, the systems have simple algorithms that will not tolerate events such as parts obscuring one another or lying propped up at odd angles. A seemingly simple but elusive industrial vision task, beyond the capability of all current systems, is the "bin-picking" problem, one regularly surmounted by humans: It involves simply grasping and removing parts jumbled together in a bin, not laid out flat on a special surface.

Thus, fast, reliable computer vision is so hard that we can presently achieve it only in highly constrained and simplified domains. This makes the fast and reliable vision performed by biological systems all the more marvelous and mysterious. Somehow, humans perform recognition, description, manipulation, and locomotion in a highly complex world of moving solid objects, both rigid and nonrigid, with complex (textured, transparent, glossy, etc.) surfaces and highly variable illumination conditions.

General-purpose vision systems, which can build descriptions of their environment in general situations, remain a research goal. Today, a consensus is emerging that such systems will be designed around two central ideas, originating in biology and rediscovered by researchers in technology. The embodiment of these ideas in vision systems is a topic of much current concern and an area of rapidly expanding technological achievement and biological insight.

The first idea is that vision systems use a hierarchy of representations that develops visual information in many intermediate stages to span the gap from input signal to cognitive symbols. Computer-vision researchers found the hierarchy to be a solution to several technical problems of computing and storage efficiency. Currently, researchers in the neurosciences are studying the extent of such a functional and physiological hierarchy in biological systems, and many signs point to biological versions of the computer-vision hierarchy.

The second idea is parallel computation. Researchers have known for a long time that nervous systems compute in parallel, and they have made many attempts to model such computations. Recent work has provided new tools in these areas (see the articles in this issue "Learning in Parallel Networks" by Geoffrey E. Hinton on page 265 and "Connections" by Jerome A. Feldman on page 277) and powerful parallel computing engines are now realizable. In the remainder

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of this article, we will explore the two themes of representational hierarchy and parallelism in computational and biological vision.

History and Background

The digital analysis of visual input has been a research issue since the late 1950s when computers became large enough to accommodate such data. After about a quarter of a century of development, computer vision is a large subfield of AI. Like robotic control and computer-speech analysis, computer vision often uses "real" data—that is, the raw output of sensors—as its input. However, computer vision also uses more symbolic or processed data. Thus, one vision program can have, for example, an array of gray-level intensities from a television image as input, while another program may take a symbolic description of a line drawing as input.

The *goals* of computer vision are also diverse but may be characterized as seeking answers to "what," "where," and "why" questions. "What" questions concern the identification of objects in a scene; "where" questions involve the perception of the environment in time and space; and "why" questions address causal relationships between objects.

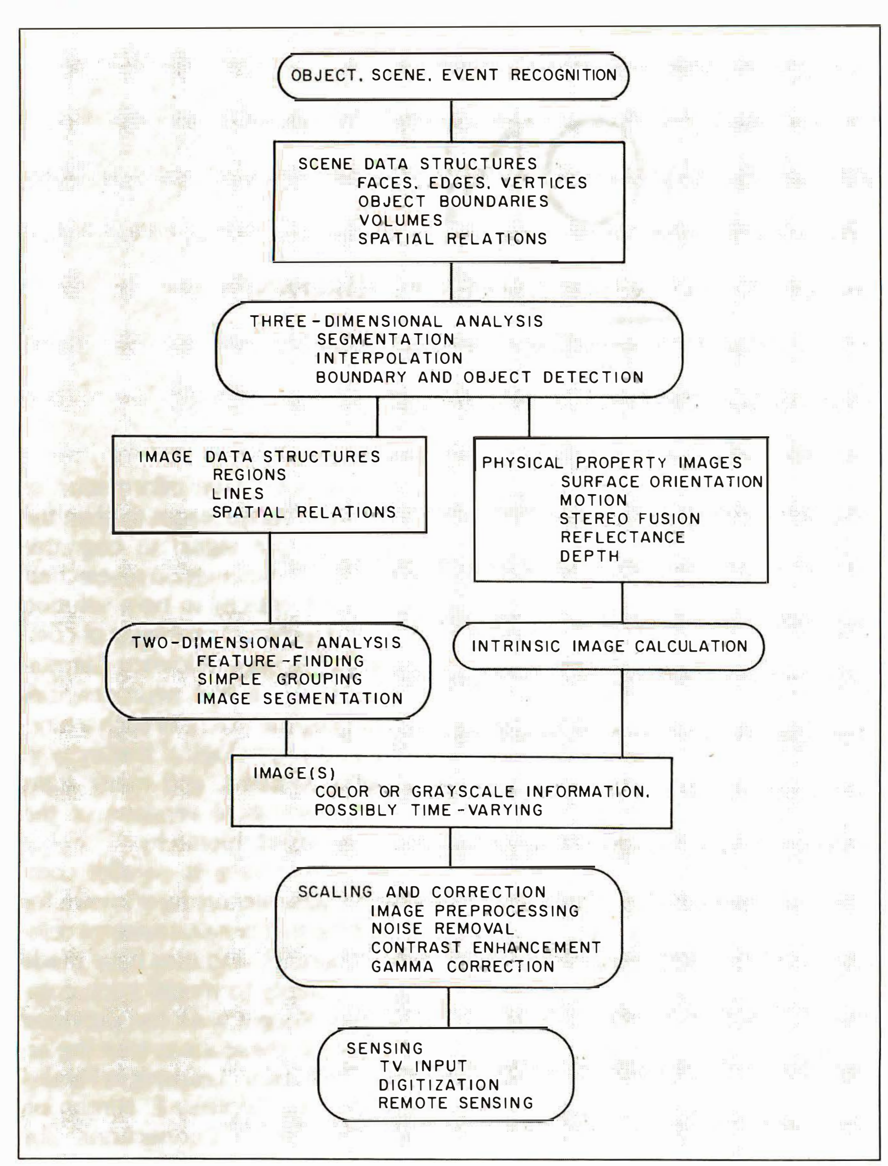


Figure 1: *The processes (ellipses) and data representations (rectangles) of a general computer-vision system. Processing can proceed from input data to symbolic description (a normal data-driven scheme) or in the reverse direction (where expectations guide processing). Control is most often thought to flow in both directions. Each stage of processing includes assumptions about how the image information is related to the phenomena of interest in the world. In natural systems these assumptions may be innate or learned.*

True computer vision, with the goal of understanding images of complex three-dimensional scenes, was first attempted in the early 1960s by Larry Roberts at MIT (see reference 1). His goal was to "understand" a scene made up of polyhedral blocks, in the sense of being able to produce a line drawing of the scene from any viewpoint. Roberts's system pioneered many fundamental techniques still in use today, not just in computer vision, but also in computer graphics. In particular, the system analyzed digitized input images by identifying "edge elements" that might line up along the polyhedral edges (see figure 3b for an illustration of this technique in another application). The system then fused these edge elements to produce longer lines that corresponded to the polyhedral edges (figure 3c again is similar) and matched the resulting line and polygon data structures against three-dimensional models of primitive blocks. This process derived the scaling, rotation, and translation of the models needed to explain the image data, and this information allowed the system to produce the final line drawings, using basic computer-graphics techniques—also first attempted by Roberts—such as hidden-line removal.

Roberts's goal was ambitious even by today's standards: No computer vision system will perform the task of reliably identifying blocks on a table in the presence of occlusion and noise. However, such early work

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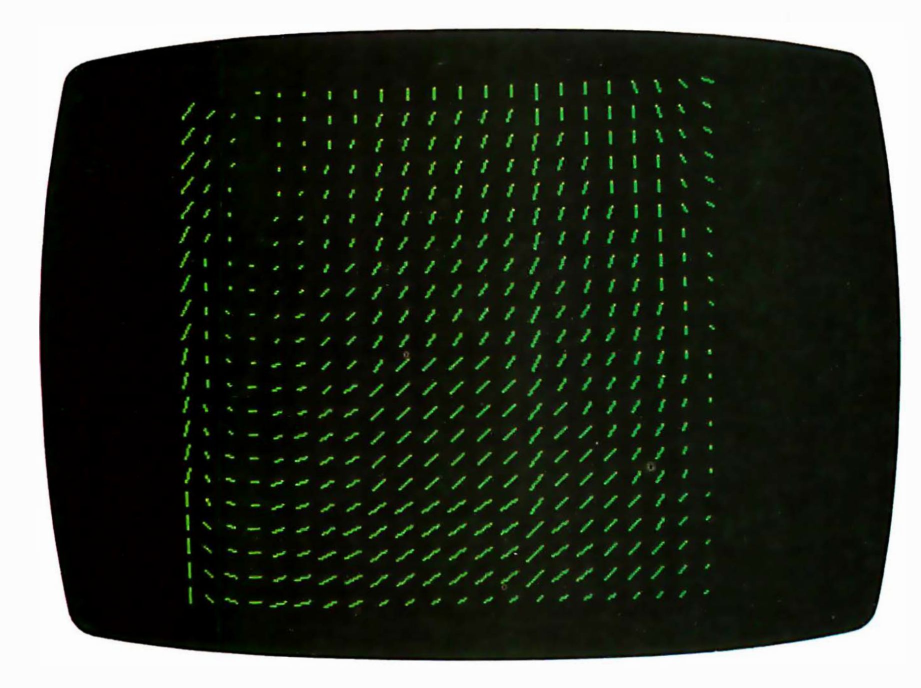
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revealed the immense computational complexity of vision and the unreliability and inadequacy of sequential control structures to allocate processing power.

Such a task requires an extraordinary amount of computation, which includes extracting physical information from an image, labeling image regions that correspond to significant objects, and symbolically describing objects in the image.



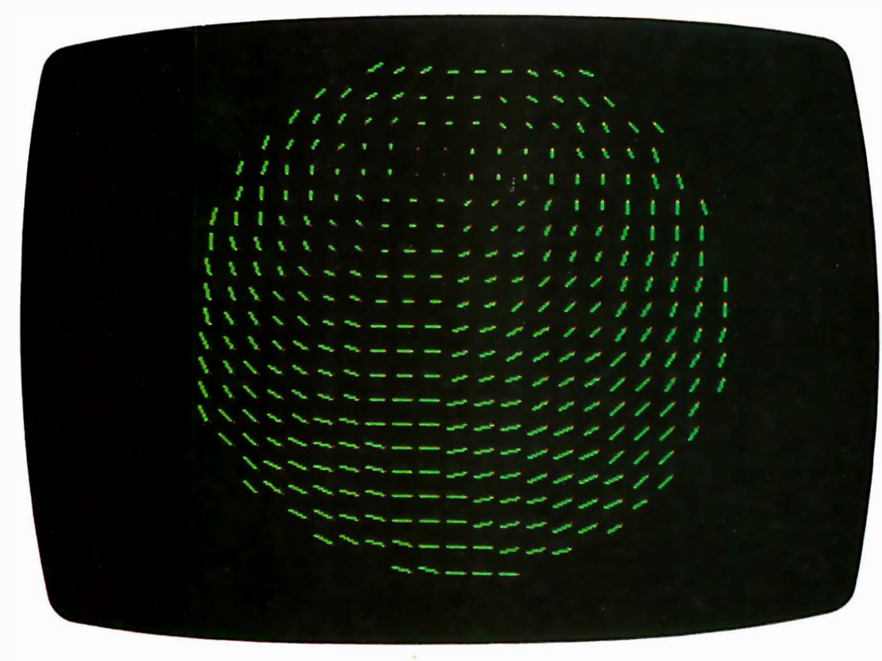


Figure 2a: *Optic flow images (retinal pattern velocities caused by scene motion) from a rotating sphere and cylinder.*

Thus the field of computer vision is quite large. It includes the aforementioned industrial inspection systems, as well as academic research efforts whose competence (what we must know to solve a problem) is often of more interest than their performance (how we actually solve the problem in real time). See the bibliography at the end of this article for more material on the field of computer vision.

In the 1970s a cognitive approach to computer vision arose, which conveniently minimized image-level computation and emphasized the symbolic manipulations to which computers are well adapted. In such "knowledge-directed" vision, processing uses facts about such phenomena as gravity, support, occlusion, or the likely spatial relations between objects in the scene. Research turned toward representing and manipulating facts about a particular setting (or *domain*, such as a grouping of polyhedral blocks or an office scene) and exploiting the domain-specific knowledge in vision.

However, the representation and application of knowledge is a very difficult branch of AI, and the available techniques proved inadequate to bridge the gap between the input image and the desired symbolic descriptions of it. Thus in 1974, starting with Marr at MIT and Barrow and Tenenbaum at Stanford Research Institute, attention was directed toward a collection of intermediate representations, termed *intrinsic* images, that would span the representation gap.

Today, the consensus of the computer-vision community is that this gap is bridged by a set of visual data representations that are arranged in a hierarchy of increasing abstraction.

Vision and the Abstraction Hierarchy

Our vision is quite reliable—that is, there is a good correlation between our perceptions and things in the world. Otherwise, we would not have survived as a species. How do we ignore irrelevant variations and concentrate on those that mean something?

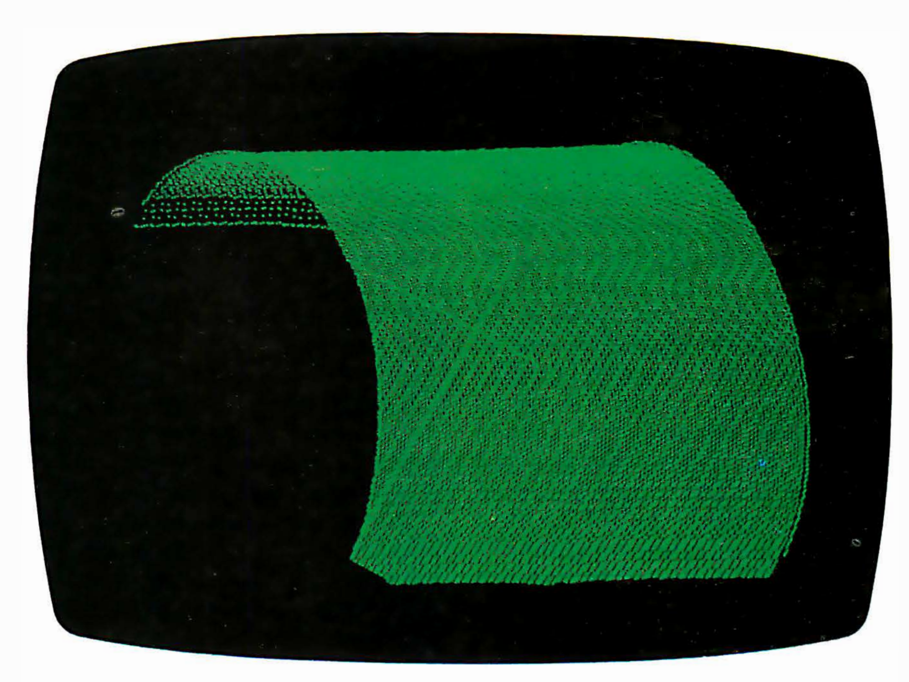
How do we achieve the constancies whereby we recognize objects under varying illumination, or faces at different ages? How do we perform so fast and reliably? A partial answer to these questions is that of abstraction hierarchies.

Modern computer vision spans the gap between input image and object perception with a hierarchy of representations (the aforementioned intrinsic images) operated on by powerful computational processes (as shown in figure 1). These processes create representations that pass from image-like representations of physical parameters to symbolic descriptions. Constructing these intermediate descriptions is feasible and probably necessary, but it involves complex computations for a general vision system (as opposed to a highly specialized system, such as an industrial system).

At the earliest level (the input level), a general vision system derives a representation of image brightness changes that it uses for stereo disparity calculations (the difference between two views of the same setting), detecting changes in surface composition, orientation, distance, reflectance, and so forth. Perceptual phenomena (e.g., subjective contours, the ability to discern colinearity of dissimilar shapes) suggest components for the earliest image representations (e.g., locations, orientations, and endpoints of features). Feature detectors that derive these components may then be designed by humans.

Much current research is centered around the production of physical property images, which are intermediate representations that the system forms before attempting object recognition. These image-like representations are registered with the input image and contain values of physical parameters of scene points such as the distance from a sensor to the point, the albedo (reflective power) of surfaces, the objects' direction of motion, the location of shadows and light sources, and so forth. Researchers generally assume that the processes producing physical property images are part of "early vision." That is, they are not dependent on the context of the scene being viewed, much less on conscious reasoning, but are robust general processes that produce reliable output in a broad range of natural circumstances. However, these processes cannot be *completely* general and reliable, since the two-dimensional input image does not capture three-

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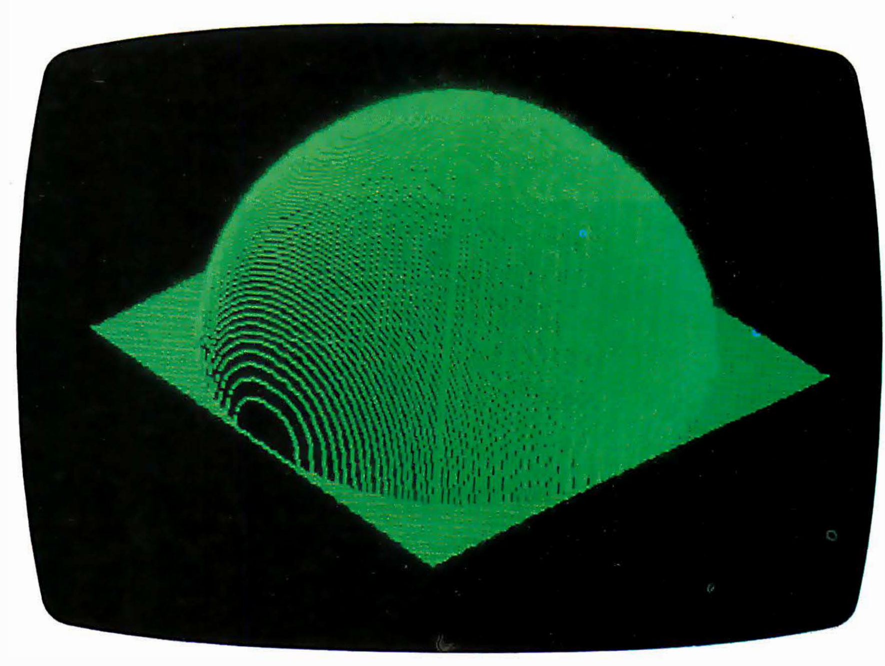


Figure 2b: *Shapes causing the images as derived by a computational vision process. Such processes use mathematical models of physical laws and assumptions about nature to recover physical information about scenes from input images. (Courtesy of John Aloimonis, University of Rochester.)*

dimensional information directly (it can only imply it). But the usual reliability of these processes in animal vision implies that they rely on natural constraints or assumptions about the world to derive unambiguous output. Identifying and using such constraints are important goals of modern computer-vision research. This, in turn, calls for seeking out properties of the physical work that could help a visual process do useful work, making mathematical models of their interaction with visual phenomena, and implementing the mathematics in computer programs. One such result that illustrates the kind of computations at this level is the computation of relative depth from optic flow (see figure 2).

The step beyond intrinsic images is a large one; although they contain physical information, they are still image-like entities not yet described in terms of objects. Two of the most important visual phenomena are motion and texture, which transmit much information about the objects and surfaces in a scene. One of the most active areas of computer-vision research is the extraction of information from motion or from optic flow of the visual field on our retina as an object or the viewer moves. It is also a particularly good illustration of the symbiosis that can take place between psychology and computer vision.

Researchers basically agree that the higher abstraction levels in a general computer-vision system must contain data structures representing aspects of the domain from which the scene originates. The resulting problems in knowledge representation are interesting in a wide variety of AI applications. For example, computer modeling of three-dimensional rigid solids is by no means a solved problem except for certain manufactured objects. Also, representing naturally occurring shapes and volumes so that they can be matched to their geometric counterparts in intrinsic images is still an open question.

High abstraction levels pose several other difficulties. Perception goes on through time, and yet representing processes through time is an area of advanced AI research.

The contribution of high-level knowledge and inferential procedures to the vision process is still a mystery. It seems certain that information does not simply flow "bottoms up" (that is, sequentially, from low-level to high-level) through the visual system, as it did in Roberts's first system. Nor is vision merely controlled hallucination, with the abstract representations dictating our perceptions as they do in dreams, subject to minor corrections from incoming data. The upper levels of abstraction hierarchy must support information flow in both directions, and a bottleneck in current computer-vision research is achieving useful interaction between the lower, image-like representations and the higher, symbolic ones.

State-of-the-Art Examples

Two examples will illustrate the operation of computer vision in the sort of abstraction hierarchy introduced in the last section. The three-dimensional MOSAIC system at Carnegie-Mellon University, developed by Marty Herman and Takeo Kanade, can reconstruct three-dimensional representations of buildings from two aerial views—using stereo to provide depth information—or from a single view—using advance knowledge about the nature of the input scene to provide depth information. Figures 3a through 3d show the operation of the monocular version of the algorithm.

The MOSAIC system uses an edge operator to find intensity discontinuities, which contain much image information in a single input image (see figure 3a). Because the image has a baffling number of such "edge elements," the system sends the output to a post-processing routine that identifies edges that are likely to con-

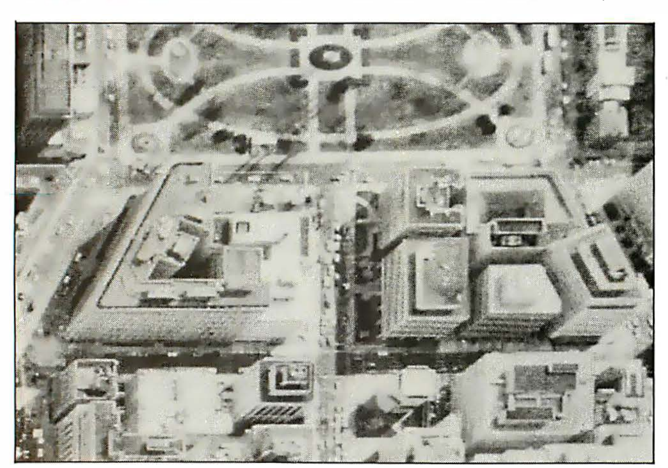


Figure 3a: *Aerial view of a city park and buildings provided as a single input image to the* MOSAIC *(see text) system.*

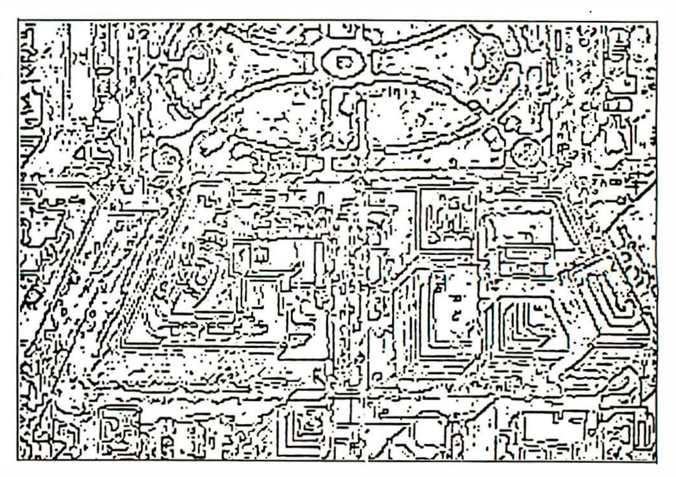


Figure 3b: *Output of an edge-finding algorithm applied to the image of figure 3a.*

tribute to interesting structures in the image (see figure 3b). Several stages of processing then link the edges into two-dimensional structures using standard edge-linking technology and information about the way lines meet to form vertices in polyhedral scenes. And then the edges are linked into three-dimensional structures—using information about gravity, support, the perspective imaging process, and other facts describing the physical scene domain and the optics of image formation. Figure 3c shows the result of this processing: a perspective view of a three-dimensional "wireframe" representation of edges in the scene.

The next stage of processing relates the wireframes to stored representations of three-dimensional solid models. In a sense, the solid models are the final output of the program, with two important additions. First, the system can relate new image information to its existing model data structures, which it can refine as it acquires the new images. Second, the system can, using standard computer-graphics technology, map the flat image onto the surfaces of the stored three-dimensional models. The system can then display three "painted" models from another angle, as shown in figure 3d.

Work continues on the extraction and identification of meaningful parts of an image. This process is called *segmentation*, which is typified in the VISIONS (Visual Integration by Semantic Interpretation of Natural Scenes) system at the University of Massachusetts. The VISIONS system's sophisticated programs use models of a specific domain (rural, outdoor scenes of houses, trees, etc.) and knowledge about that domain.

In this work, the goal is to segment a color image (as in figure 4a) into regions that correspond to meaningful objects or substances in the image. The process involves extracting straight lines (see figure 4b), and regions of related color characteristics (see figure 4c). The VISIONS system uses interpretation rules that incorporate knowledge about the scene domain (for example, that a driveway is not found silhouetted against the sky, or that a house's roof is above its walls) in cooperation with the image-guided segmentation processes. These interpretations make the segmentation process more reliable, by indicating, for example, when regions may be merged or should be split. For example, in figure 4c the system has colored regions that it has hypothesized, using interpretation rules, to be shutters. Foliage is an important component of these scenes, and VISIONS has a set of feature extractors and recognizers to allow reliable identification of foliage, despite its many different appearances.

Figure 5 shows the final labeling of another input scene, with regions identified as sky, foliage, grass, wall, shutters, roof, and regions (in black) that are uninterpreted due to the lack of a symbolic model in the current system or deviation of the scene's appearance from that predicted by the model. VISIONS currently models some 20 major objects and object collections such as "house" and "house scene," and a larger number of object parts such as "roof" and "shutters."

The two examples of current systems show the beginning of understanding the competence issues in vision: We know what kinds of entities need to be computed. However, each of these examples requires huge amounts of computer time. Most researchers believe that the performance problem in vision will only be solved through parallel computation.

Challenges from Animal Vision

One of the most promising directions for the study of parallel processing has centered around studies of

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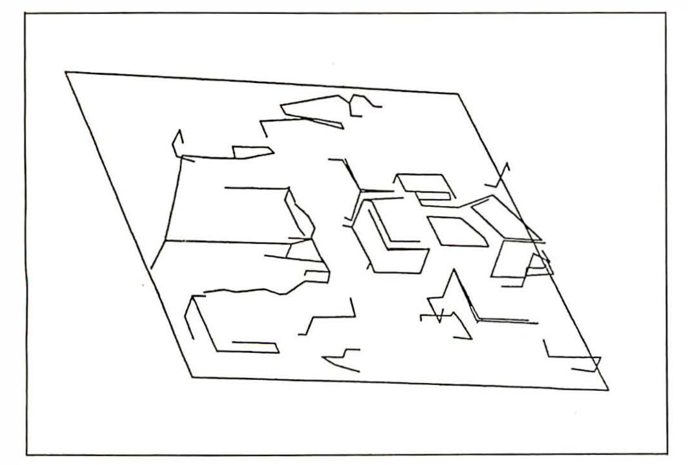


Figure 3c: *A "wireframe" of linked line segments in three dimensions resulting from several sorts of processing applied to the data of figure 3b.*

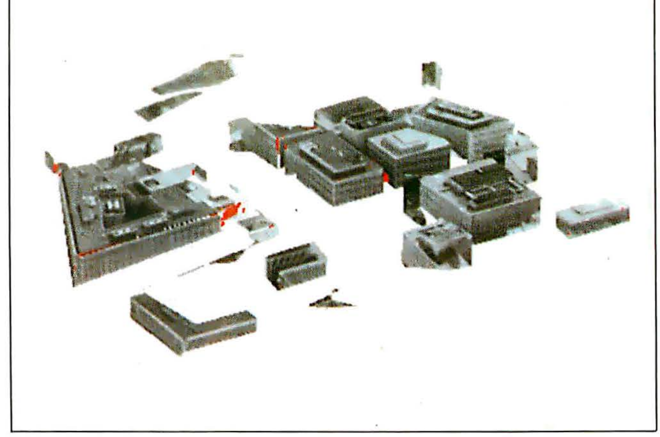


Figure 3d: *Computer-graphics techniques use the original photo and the three-dimensional models extracted by further processing of the wireframe data of figure 3c, resulting in a convincing reconstruction of the scene. (Courtesy of Marty Herman and Takeo Kanade at Carnegie-Mellon University.)*

human and animal vision. Unlike robot vision, where many of the complexities of sensing the environment can be manipulated by tailoring the environment and using special imaging techniques, animal vision must somehow analyze time-varying photometric data in its full complexity in real time. Furthermore, biological systems use neural-processing elements that are six orders of magnitude slower than silicon components.

Despite all these apparent disadvantages, animal systems succeed admirably. Experiments with human subjects show that they can make a variety of behavioral responses to visual stimuli in a few hundred milliseconds. Thus, the biological system, somewhat embarrassingly, embodies solutions to problems that still plague vision researchers. This situation has lured researchers to tackle the problem of modeling the human visual system head-on, in the hopes of discovering its secrets. Such researchers typically have a wide range of cross-disciplinary interests and are joining to make progress in the separate fields of psychology, neuroscience, and computer science. We shall describe some of the more interesting of the many new results from these disciplines.

Since humans are very good at visual tasks, researchers were surprised to find that, for some tasks, information can be processed in parallel, but for rather modest increases in complexity, the processing became sequential (see reference 2). Treisman describes visual displays of letters about which subjects were asked questions of the form "Does the display contain a T?" (See figure 6.) Most subjects can answer this question in a few hundred milliseconds, independent of the number of letters displayed (see the lowest dashed lines of figure 6). However, if we change the question to "Does the display contain a *red* T?" the time taken to answer becomes linearly dependent on the number of letters displayed. From this we conclude that the brain processes certain primitive features in parallel but processes conjunctions of these features serially.

We still lack a detailed explanation for this result, but one hypothesis is as follows. It may be uneconomical for the visual system to check stored prototypes against spatial positions. A faster way would be for the brain to build an abstract representation that is independent of the precise point in space where the feature is located. Thus, we hypothesize that the brain builds a representation for a T if there is one or more Ts anywhere in the visual field. In a similar process, the brain builds a representation for perceived color values, such as "red." Thus, the brain could answer questions concerning these features directly. In contrast, questions about conjunctions of features cannot be handled by this scheme, since information about spatial location is not present in the abstract representation. One idea, termed the *searchlight hypothesis* (see reference 3), is that the brain

(continued)



(4a)



(4b)



(4c)

Figure 4: *(a) An outdoor scene to be analyzed by the* VISIONS *computer-vision system. (b) Straight lines extracted from the data of 4a. (c) Regions extracted from the data of 4a.*

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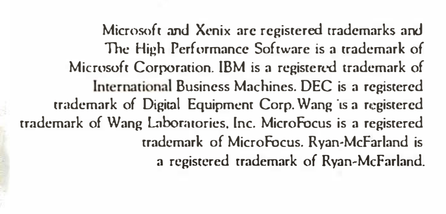

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Figure 5: *Regions extracted and labeled by* VISIONS *for another house scene.* |*Figures 4 and 5 courtesy of Allen Hanson, Edward Riseman, and the* VISIONS *project at the* University *of* Massachusetts.|

sequentially focuses on spatial locations from which the features are derived. In this manner, if the "T" feature and the "red" feature occur together, then the question can be answered affirmatively. The separation of data into two different levels of abstraction (spatially organized and nonspatially organized) seems to be a fundamental design decision that allows the brain to do its job quickly.

Mishkin and colleagues performed another experiment that points to this organization (see reference 4). They made selective lesions in different parts of a monkey's cortex. Monkeys with lesions in one area of the brain performed a feature-recognition experiment at chance levels (in a statistically random manner) but had no trouble with a spatial-location experiment. In contrast, monkeys with lesions in another area performed a spatial-location task at chance levels but had no trouble with a feature-recognition experiment. This startling result shows that an important psychophysical property may have a distinct locus in animal brains.

CODING PHYSICAL CONSTRAINTS AS HARDWARE

Concurrent with these biological and psychological results, researchers in computer vision have been exploring parallel models of computation that handle features in similar ways. In addition, these models have to grapple with many difficulties of noise and missing information: A shape outline or a feature like a straight line is only represented in an image by partial and conflicting evidence mixed with confusing noise.

To overcome this problem, we use the Hough transform (see reference 5). The Hough transform includes a

(continued)

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wide variety of clustering histogram analysis and estimation strategies, all of which transform data so that phenomena of interest form clusters.

Consider an example using the Hough transform for line detection. To detect lines in an image we must first detect local intensity differences or *edges*. Figure 7a shows the Hough transform applied to the image of a Rubik's cube, in which intensity differences could be caused by an actual edge of the cube, a shadow, a label, and so on. If we call the image $f(x,y)$ and the horizontal and vertical intensity differences $h(x,y)$ and $v(x,y)$, then one way to compute the intensity differences uses the values of neighboring picture elements in the

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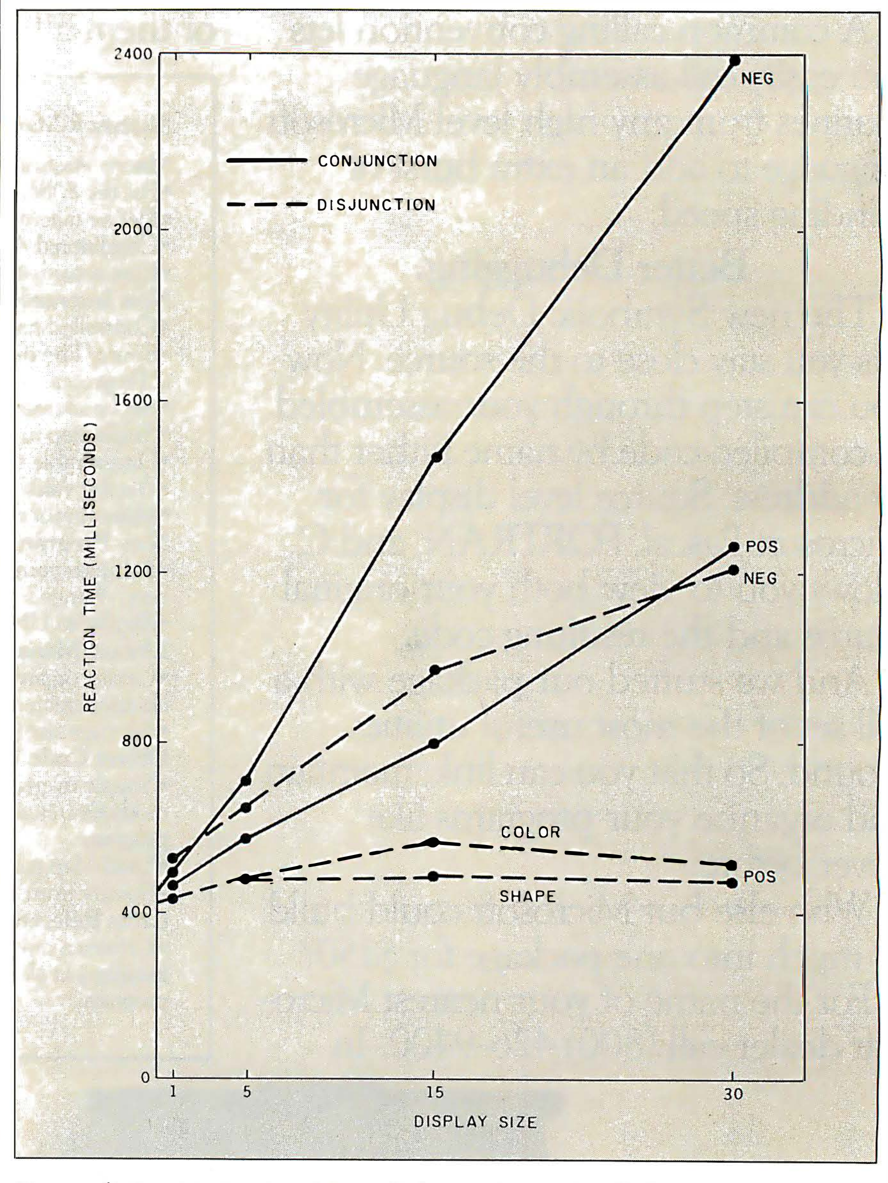


Figure 6: *Reaction time in milliseconds for experiments described in text. In recognizing a single feature such as "red" or the letter "T", a subject's reaction time is constant if the feature is in the display* (POS). *If it is absent or, more importantly, if the stimulus is a conjunction (i.e., red T, depicted by a solid line), the response time increases linearly with the size of the display.* |*Figure taken from Treisman (see reference 2).*|

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following manner:

$$h(x,y) = f(x+1, y-1) - f(x-1, y-1) + 2\times f(x+1, y) - 2\times f(x-1, y) + f(x+1, y+1) - f(x-1, y+1)$$

$$v(x,y) = f(x-1, y+1) - f(x-1, y-1) + 2\times f(x, y+1) - 2\times f(x, y-1) + f(x+1, y+1) - f(x+1, y-1)$$

The edge finder reports an edge if the magnitude of the intensity differences ($m=\sqrt{(h^2+v^2)}$) is greater than a given threshold value. We will give the orientation of the edge as θ, where $\theta=\arctan(h/v)$.

Next, we accumulate the local edges into straight lines. This accumulation is essentially a voting process, in which each edge element "votes" for the lines that could have caused it. Thus, in figure 7b, the edge element centered at the point (x_0,y_0), with the orientation θ, votes for a line that we can describe as (ϱ,θ), where $\varrho=x \cos \theta+y \sin \theta$.

After each edge element votes for the lines that could have caused it, the line with the most votes is presumed to be an actual line of the image, rather than an artifact or noise.

To facilitate this accumulation process, place all the values of (ϱ,θ) into another two-dimensional array, with ϱ and θ as coordinate axes (see figure 7c). The brightness of each cell in figure 7c is proportional to the number of edge elements voting for a line at that particular value of (ϱ,θ). That is, the brighter the cell, the more likely the image actually has a line with those values of (ϱ,θ).

To sum up, suppose the feature detector applied to a point (x,y) of the image responds with a local edge orientation θ and a measure of edge contrast. Then one version of the algorithm is as follows.

For each point (x,y) in the image, do the following two steps:

1) Apply the detector to get θ at (x,y)
2) If edge contrast exceeds some threshold:
   compute $\varrho=x \cos \theta+y \sin \theta'$
   increment LineParams $[\varrho,\theta]$

Several implementations of the Hough transform are possible (see reference 6). We have just described a straightforward sequential computer implementation that represents parameter space in an array. This representation is costly for transforms with multiple parameters, since it demands space exponential to the number of parameters—although researchers have made progress in implementations of the accumulating parameter space (described above) using hash tables or content-addressable memories, which use less space.

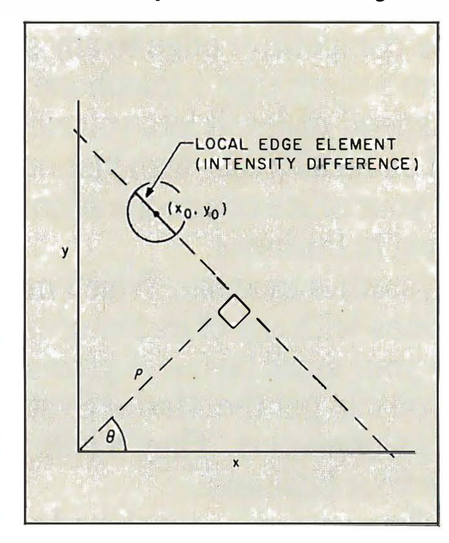
Finally, the Hough transform can be implemented in massively parallel computing networks in which prewiring accomplishes all the voting in one time step.

The general notion of capturing functionality in terms of connection patterns is known as *connectionism* and is sparking a great deal of interest in different disciplines. One issue raised is computational. How is the computation carried out in very large networks with complex constraints? Recently, progress has been made by several groups headed by Kirkpatrick, Hopfield, Hinton, Sejnowski, Geman, and Geman (see references 7 through 10 and Geoffrey E. Hinton's article "Learning in Parallel Networks" on page 265). The thrust of this work is that constraints can be cast as local changes in "energy" and that the computing units can be turned on or off to minimize energy.

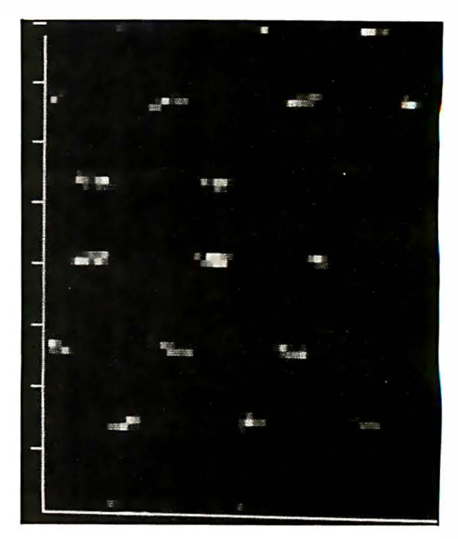
The neural network also shows a general way of representing informa-

(continued)

(7a)



(7b)



(7c)

Figure 7: *(a) Results of applying a computer-vision edge operator to the image of a Rubik's cube. (b) The geometrical constraint that relates a local edge element (x_0,y_0,θ), shown by a circle, to a line, denoted by ϱ and θ. For every edge element in an image, a unique line can be determined. (c) Each edge element "votes" for the lines that may have caused it, as shown in this plot of ϱ and θ values. The brightest accumulations of values for ϱ and θ indicate the most likely lines in the actual image.*

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tion known as *value encoding*. On a sequential computer, a variable can have only one value at a time. A parallel computer, however, may need to simultaneously access many values of a variable. In value encoding, we represent the different possible values of a variable as discrete cells or "intervals." The number of cells used determines the accuracy in the representation.

For example, we can represent the parameters for the edge element of figure 7b as discrete intervals centered at (x_i, y_i), with a width of $(\Delta x, \Delta y)$ (see figure 8a). We can also represent the line parameters of figure 7c as discrete intervals centered at (ϱ_i, θ_i), with a width of $(\Delta\varrho, \Delta\theta)$ (see figure 8b). This idea was suggested by Horace Barlow at Cambridge and is being pursued by D. H. Ballard and Jerome Feldman at the University of Rochester. We can then hard-wire the accumulation (or voting) process from figure 7 directly into hardware. Thus, in figure 8a we assign a distinct processor for all the values of (x,y) that fall within the boundaries $(\Delta x, \Delta y)$ and a specified range of θ. In figure 8b, we assign a distinct processor for all the values of (ϱ,θ) that fall within the boundaries $(\Delta\varrho, \Delta\theta)$. Each processor can either be on or off, based on a modification of the algorithm we described earlier:

For each edge unit, turn it on if its input exceeds some threshold. For each line unit (ϱ,θ), turn it on if its input exceeds some threshold. That is, if enough colinear edge units are "turned on" (figure 8a), the line that encompasses all of those edges will be turned on (see figure 8b); that is, the system will draw a line with those parameters.

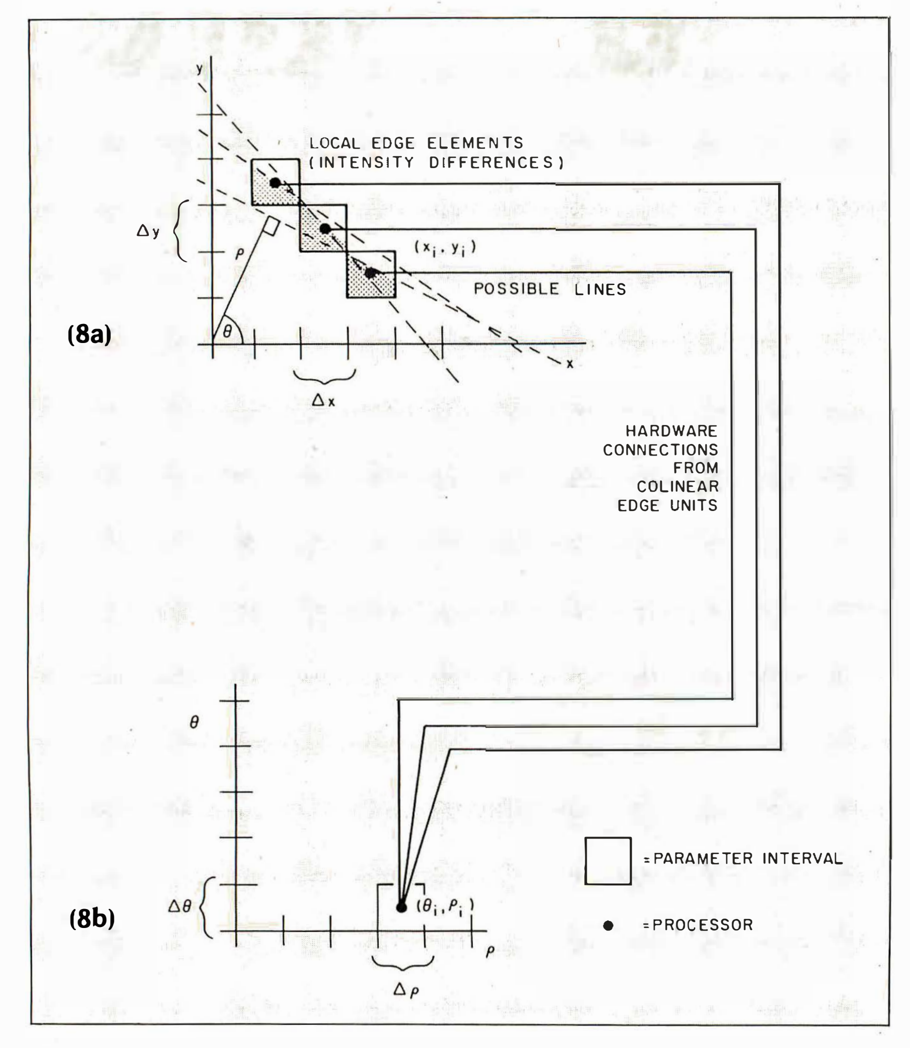


Figure 8: *The "voting process" of figure 7 can be directly encoded in hardware using interval encodings. (a) For each of a discrete number of (x,y) values with bounds $(\Delta x, \Delta y)$, we assign a specific processor. (b) For each of a discrete number of (ϱ,θ) values with bounds $(\Delta\varrho, \Delta\theta)$, we assign a specific processor. If enough colinear edge units are "turned on," the line that encompasses all of those edges will be turned on. This strategy may be impractical for* VLSI *(very-large-scale integration) designs, but it is realizable in the brain, which has approximately* 10^{10} *neurons and approximately* 10^4 *connections per neuron.*

This realization of the Hough transformation shows how complex wiring carrying simple excitation can replace the complex information flow of voting. Nets of fairly simple computing units with highly structured connections carrying simple excitatory and inhibitory levels can provide a uniform architecture for computation at many levels of abstraction, from early vision to symbolic and cognitive levels.

We have tried to highlight some of the various issues that arise in these kinds of parallel models. However, at this point the reader may still be wondering how applicable this kind of computation is to a general vision system. The first-order answer is that generality is achieved through hierarchies. The line computation can serve as a subnetwork in a much larger network that spans the vision abstraction hierarchy (see figure 1). Hierarchies may be a ubiquitous strategy for organizing information in animals. Figure 9 shows Kiel's ontological ("related to or based upon being or existence") hierarchy of children's preferences (see reference 11). Kiel's hierarchy is also evident in eye-movement experiments, during which adult subjects showed the same kind of attentional preferences. Hierarchical organization may also be traceable to brain anatomy, although data is only

available for the visual areas (see reference 12). Hierarchies may be a global organization feature of the cortex.

CONCLUSION

The most important breakthrough in computer vision in the past decade has been a broad understanding of what has to be computed and how the computations are organized. Current research is shaped by the discovery that vision primitives (intermediate images) form a natural hierarchy and that the amount of computation required to build this hierarchy is enormous. Now that we have an understanding of what to compute, the crucial issue is that of computing it in real time. Throughout the decade, there has been a close relationship between "pure" vision research, which ignores biological constraints, and that which directly attempts to explain how the animal vision system works. The underlying intent of this article has been to show that ideas connected with animal vision, contrary to many earlier expectations, are playing an increasingly compelling role in shaping computer-vision research. The current notion of hierarchy of representations was developed without direct connections to animal research, but concurrent research shows that animal brains already incorporate hierarchical representations as a fundamental design principle. Furthermore, it seems likely that the biological system has also solved the parallel-computation problem that is emerging as the issue for formal vision studies. Thus we can anticipate a profusion of cross-disciplinary research efforts in the decade ahead, in the drive to realize practical, real-time visual perception. ■

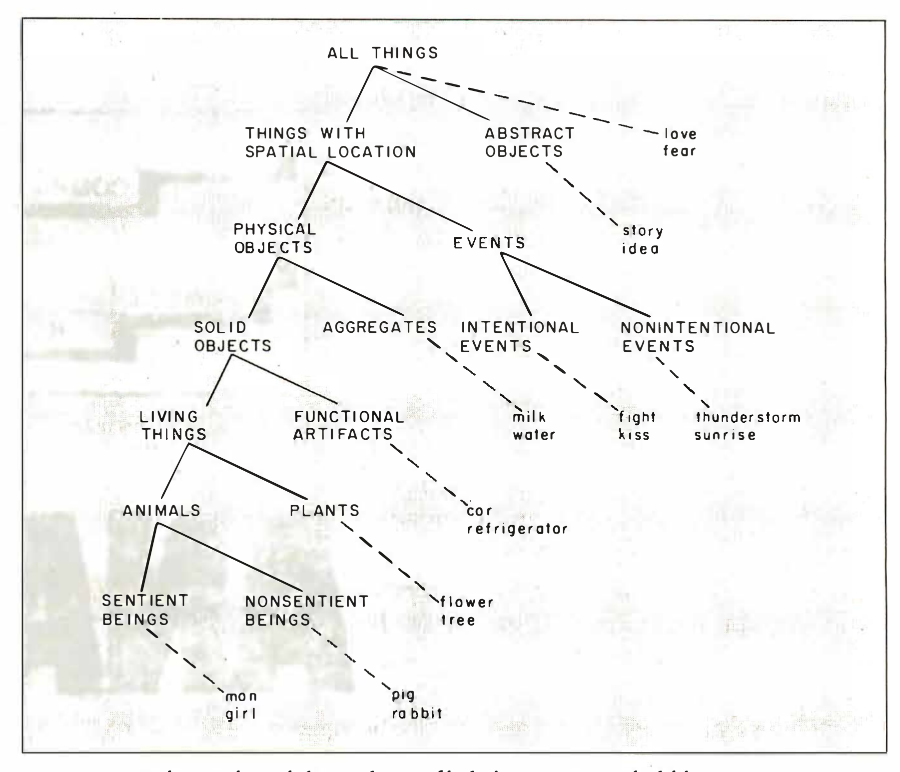


Figure 9: *Kiel's ontological hierarchy established via testing of children.*

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ACKNOWLEDGMENTS

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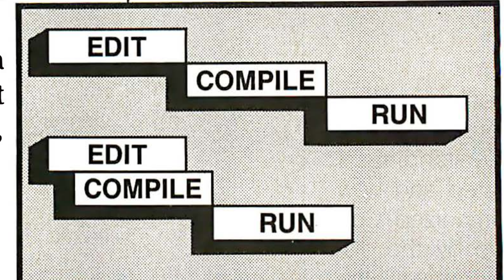
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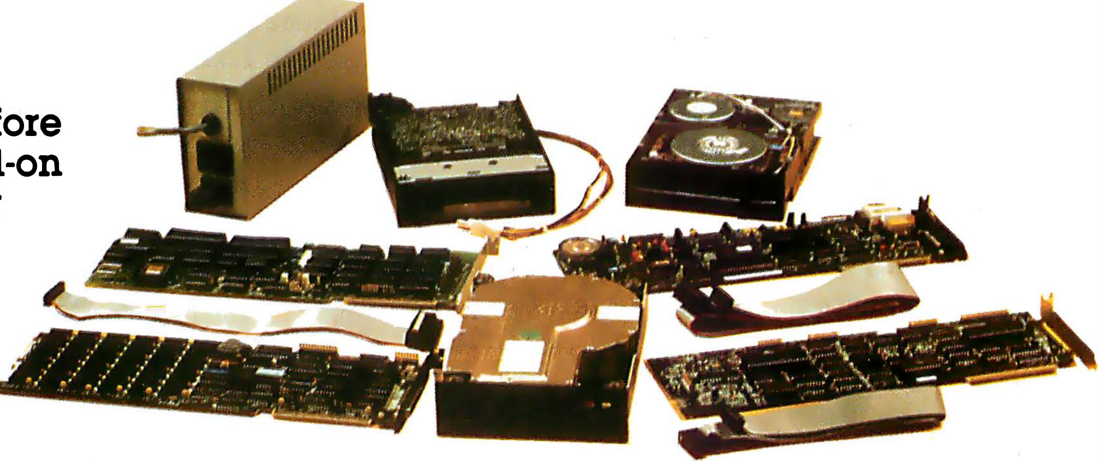
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LEARNING IN PARALLEL NETWORKS

BY GEOFFREY E. HINTON

Simulating learning in a probabilistic system

THE BRAIN is an incredibly powerful computer. The cortex alone contains over 10^{10} neurons, each connected to thousands of others. All of your knowledge is probably stored in the strengths of these connections, which somehow give you the effortless ability to understand English, to make sensible plans, to recall relevant facts from fragmentary cues, and to interpret the patterns of light and dark on the back of your eyeballs as real three-dimensional scenes. By comparison, modern computers do these things very slowly, if at all. They appear very smart when multiplying long numbers or storing millions of arbitrary facts, but they are remarkably bad at doing what any five-year-old can.

One possible explanation is that we don't program computers suitably. We are just so ignorant about what it takes to understand English or interpret visual images that we don't know the appropriate data structures and procedures to put into the machine. This is what most people who study artificial intelligence (AI) believe, and over the last 20 years they have made a great deal of progress in reducing our ignorance in these areas.

Another possible explanation is that brains and computers work differently. Perhaps brains have evolved to be very good at a particular style of computation that is necessary in everyday life but hard to program on a conventional computer. Perhaps the fact that brains store knowledge as connection strengths makes them particularly adept at weighing many conflicting and cooperating considerations very rapidly to arrive at a common-sense judgment or interpretation. Of course, any style of computation whatsoever can be *simulated* by a digital computer, but when one kind of machine simulates a very different kind it can be very slow. To simulate all the neurons in a human brain in real time would take thousands of large computers. To simulate all the arithmetic operations occurring in a Cray would take billions of people.

It is easy to speculate that the brain uses quite different computational principles, but it is hard to discover what those principles are. Empirical studies of the behavior of single neurons and their patterns of connectivity have revealed many interesting facts, but the underlying computational principles are still unclear. We don't know, for example, how the brain represents complex ideas, how it searches for good matches between stored models of objects and the incoming sensory data, or how it learns. In this issue, Jerome A. Feldman describes some current ideas about how parallel networks could recognize objects (see "Connections" on page 277). I will describe one old and one new theory of how learning could occur in these brain-like networks. Please remember that these theories are extreme idealizations; the real brain is much more complicated.

ASSOCIATING INPUTS WITH OUTPUTS

Imagine a black box that has a set of input terminals and a set of output

(continued)

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Ideally, the black box will capture some neat regularity in its connection strengths.

terminals. Each terminal can be clamped into either of two states, active or inactive (1 or 0). We can show the black box what we would like it to do by repeatedly clamping a combination of 1s and 0s on the input terminals and another combination of 1s and 0s on the output terminals (each combination is called a *vector*). When we have done this for many I/O (input/output) pairs, we would like the black box to automatically set its output terminals into the correct state when we clamp a vector on the input terminals. Ideally, if there is some neat regularity in the mapping from input vectors to output vectors, we would like the black box to "capture" this regularity in its internal connection strengths in order to give the "correct" output vector for input vectors it has never seen before. This kind of black box would be a very useful module to have within an intelligent system.

If the black box contains only direct connections from input terminals to output terminals, there is a beautifully simple learning procedure that adjusts the weights on these connections until every input vector causes the appropriate output vector. The learning procedure has two phases that keep alternating. In phase 1, we clamp an input vector on the input terminals and an output vector on the output terminals. Then we increment by a small amount, δ, the weights of all connections that have both their input and output terminals active. In phase 2, we clamp the same input vector, but we let the black box decide for itself what output vector to produce, using the rule that an output terminal turns on if the sum of the weights on its connections from active input terminals is positive. We then

decrement by δ all the connections that have both their input and output terminals active. If the network produces exactly the right output, these decrements will exactly undo all the increments we made in phase 1, because exactly the same pairs of input and output terminals will be active in the two phases. If, however, the network produces the wrong output in phase 2, some of the weights that were incremented will not be decremented or vice versa, so some weights will change.

The learning procedure I have described is a version of the Widrow-Hoff or "perception convergence" procedure. It has a remarkable property: If we keep cycling through all the pairs of input and output vectors using this two-phase procedure for each pair, we will converge on a set of weights that causes the right output vector for every input vector *if any such set of weights exists*. The big disappointment (which led people in AI to abandon this kind of model) is that for most interesting problems there is *no* suitable set of weights. The relationship between the input and output vectors is just too complicated to be captured by a system that has direct connections between input and output terminals. At the very least, there must be intermediate layers within the black box, and units in these layers must learn to extract a hierarchy of "features" of the input vector that can eventually cause the right output.

Here is an example of a relatively simple task that requires intermediate units. The input consists of two 8-bit vectors, one of which is a shifted version of the other. Only shifts one place to the left or one place to the right are allowed. There are two output terminals, one for each possible shift, and the black box must turn on the correct output terminal for any appropriately related pair of input vectors. The task sounds easy until you consider that any one of the input bits, considered in isolation, provides *no* information about what the output should be. Moreover, simply adding up evidence from all the separate in-

(continued)

put bits is useless. The task can be done only if you consider combinations of bits in one vector with bits in the other, which requires intermediate units that extract informative combinations. Figures 1a and 1b show a collection of useful intermediate feature detectors that work well together for performing this task.

When we try to extend the simple learning procedure to networks containing intermediate units, more complications arise because we do not know in advance how we want the intermediate units to behave. So instead of just fixing some weights that will make the output terminals behave in the way that we specify, the learning algorithm must also decide under what circumstances each of the intermediate units should be active. This amounts to *creating* intermediate representations. Several more recent learning procedures can do this. I shall describe one that Terry Sejnowski and I discovered. It is only guaranteed to work in networks of a rather special kind, which I will now describe.

Networks That Minimize Their Energy

The kind of network we have been considering so far consists of layers of units in which units in one layer are connected to units only in contiguous layers. More complex networks have cross-talk within a layer and feedback from later layers to earlier ones. It is generally very hard to analyze the behavior of such networks, but John Hopfield at Cal Tech (reference 1) has shown that there is an interesting special case that behaves in a very useful way. In a Hopfield net, the units make their decisions asynchronously, the communication between units is instantaneous, and all the connections are symmetrical; the effect of unit i on unit j is the same as the effect of unit j on unit i. Given these restrictions, the various possible states of the whole network form a space like a bumpy surface and the current state of the network behaves like a ball bearing placed on this surface—it moves downhill into the nearest *local minimum*. Each point in the surface corresponds to a pattern of active and inactive units in the network, and the height of the surface at that point represents the "energy" of that pattern of activity, where the energy of a pattern is defined as minus the sum of all the weights on connections between pairs of active units. Therefore, if two units have a big positive weight between them, patterns in which they are both active will have low energy; it is patterns like this into which the network will settle. Conversely, a negative weight between two units will make a big positive contribution to the energy when they are both on, so the network will tend to avoid such states.

Figure 2 shows a small network whose lowest energy state is -8. Can you figure out which units are on and which are off in this state? You will always end up at an energy minimum if you start with a random state and then apply the following rule to each unit in turn (in any order): If the sum of the weights on the connections to other currently active units is positive, turn it on; otherwise, turn it off. If you apply this procedure a few times, you will discover that there is another minimum with an energy of -3 and that once the network has settled into this state it will just stay there.

Networks of this type can be used to associate input vectors with output vectors. To provide the input, we clamp a subset of the units into their

Figure 1a: *A network with 16 input terminals, 12 intermediate units, and 2 output terminals. The boldface units show which bits are on in a typical pair of input and output vectors. The 8-bit vector at the bottom has been shifted one place to the left (with wraparound) to produce the 8-bit vector immediately above it. With these two vectors as the input, the correct output vector (shown at the top of the figure) has the left unit active to represent a left shift. Each of the 12 intermediate units is connected to all the input and output units, but only one set of connections is shown. The intermediate units also have a fixed threshold, which is subtracted from their net input before the decision is made to turn them on or off.*

on or off states, and, once the rest of the network has settled into an energy minimum with this input vector clamped, we treat the states of another subset of the units as the output. In figure 2, for example, we could clamp the three bottom units into the active state to represent the input vector (1, 1, 1); we would get the output vector (1, 0) by letting the network settle and then reading the states of the top two units.

To teach the network a particular set of I/O pairs, we would need to create an appropriate energy landscape—we would need to choose weights so that for each clamped input vector the system had an energy minimum that yielded the correct output vector. Choosing such weights is not an easy task, and to make matters worse, we might end up with an energy landscape in which there were many different local minima for each clamped input; each input vector might give many different outputs depending on the energy minimum into which the system happened to settle. In figure 2, for example, the input vector (0, 0, 0) can generate two different output vectors depending on the initial states of the middle units and the order in which decisions get made.

A Probabilistic Network

If the same input is going to produce different outputs on different occasions, we would at least like to have some control over the probabilities. It would be nice, for example, if we could guarantee that deeper minima would be found more often than shallower ones. It would be even better if we could guarantee that the relative probability of ending up in two different minima depended *only* on their relative depths. We could then control the probabilities of getting particular outputs by manipulating the energy landscape (i.e., by changing the weights).

Once again, a physical analogy is helpful: If we have a ball bearing on a bumpy surface and we shake the whole system up and down, the ball bearing will be able to jump over the

(continued)



Figure 1b: *The weights that are learned by the 12 intermediate units. The black and white rectangles in the bottom two rows of a unit represent the weights on its connections to the input terminals. The sizes of the rectangles indicate the magnitudes of the weights. Black indicates a negative weight. The two weights at the top of each unit show how it affects the two output terminals. The weights all start at 0 and change by very small steps. Notice that all 12 units detect different combinations of active input terminals and that these combinations are generally sensible predictors of the global shift for which the unit "votes."*

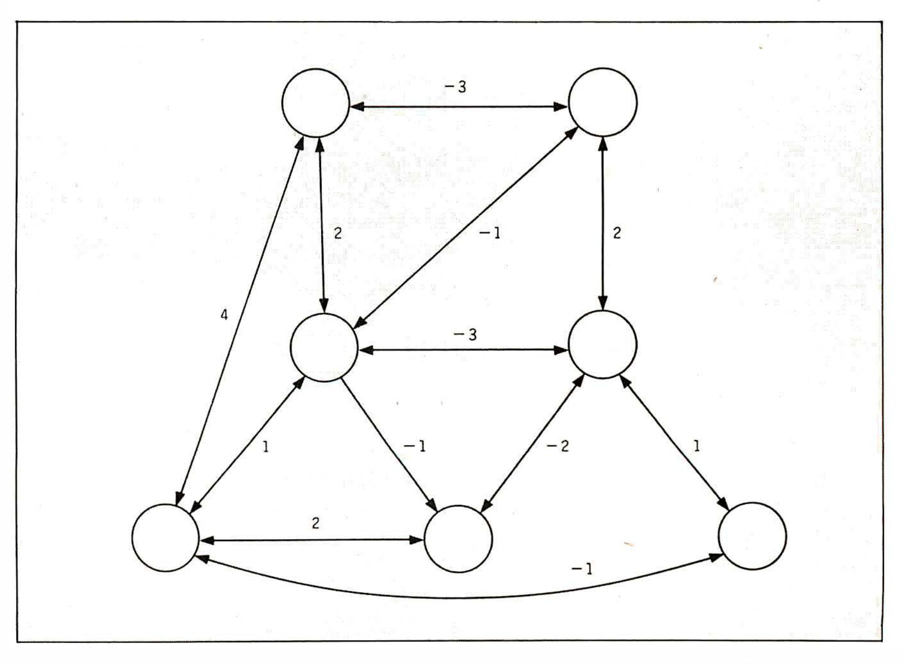


Figure 2: *A simple network with three input units at the bottom, two intermediate units in the middle, and two output units at the top. All the connections are symmetrical.*

barriers that separate shallow minima from deep ones; the ball bearing will spend most of its time in the deeper minima, even though it will occasionally sample higher energy states. If we shake for a while in just the right way, a useful simplification occurs: We approach a condition called "thermal equilibrium" in which the ball bearing is still moving from place to place, but the *probability* of finding it at any one place on the surface is stable and depends only on the height of the surface at that point—it doesn't depend on where the ball bearing started or on the shape of the energy landscape. More precisely, the log of the probability ratio of finding the ball bearing in two different states is proportional to the energy difference of those two states. Scott Kirkpatrick at IBM introduced the idea of using "thermal noise" to escape from local minima and to increase the chances of finding the deeper minima (see reference 2). He has shown that for large problems in which the cost of a solution is the analog of energy, an effective method for finding low-cost solutions is to start with a lot of thermal noise and gradually reduce it—a process that he calls "simulated annealing."

In our parallel networks it is easy to introduce the analog of thermal noise. We just modify the decision rule that is used by the individual units. They still compute the sum of the weights on the connections coming from other active units, but instead of always turning on when this sum is positive and off when it is negative (which always reduces the energy of the network), they behave probabilistically, as shown in figure 3.

Using this probabilistic decision rule, we can run networks in the following way: Clamp an input vector, let the remaining units turn on and off probabilistically until the network has reached thermal equilibrium, and then read the output vector. At equilibrium the output units will continue to change states, but each output vector will have a fixed probability that does not vary with time.

Research teams in fields as diverse as statistics (Stuart and Donald Geman), neuroscience (Terry Sejnowski), psychology (Paul Smolensky), and artificial intelligence are now investigating networks of this kind. Statisticians call them Markov Random Fields. At Carnegie-Mellon University we call our particular version the Boltzmann Machine, in honor of Ludwig Boltzmann, one of the founders of statistical mechanics.

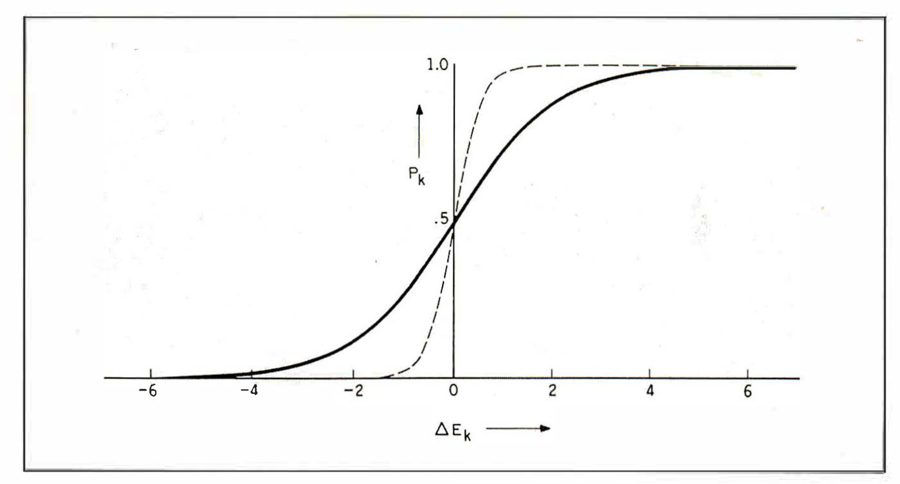


Figure 3: *This shows the probability p_k with which the kth unit is active. The quantity ΔE_k is the sum of the weights on connections between the kth unit and other currently active units. The equation is*

$$p_k = \frac{1}{1+e^{-\Delta E_k/T}}$$

T is the level of thermal noise in the network. The solid curve is for T = 1 and the dotted curve is for T = 0.25. If the value of T is decreased, the unit becomes less probabilistic. When T = 0, the curve becomes a deterministic step function.

Learning Again

We can now return to the issue of learning. First, we redefine the learning task in probabilistic terms. For each possible input vector, we want to produce each possible output vector with a certain probability. (Generally, most of these probabilities will be close to 0 and a few will be close to 1.) We can then train the network to behave in this way by alternating between two phases that are very similar to those used in the earlier learning rule.

In phase 1 we tell the network about the desired probabilities by clamping pairs of input vectors and output vectors with the corresponding frequencies. Each time a pair of input and output vectors is clamped, we run the network until it is close to thermal equilibrium; we then run the network for a little extra time, modifying the weights in the following way: For each unit of time during which two units are both active, we increment the weight between them by δ.

In phase 2 we clamp input vectors and let the network decide for itself what output vector to give. Once it has approached equilibrium, we run a little longer, as before, and now *decrement* by δ the weights between pairs of active units. If we keep alternating between phase 1 and phase 2, showing the network all the various pairs of input and output vectors, the net change in the weight between any two units will be proportional to the difference between the probability that the two units are both active in phase 1 and the probability that they are both active in phase 2 (averaged over all I/O pairs). It is remarkable that when these probabilities are measured at thermal equilibrium, their dif-

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ference is exactly the right quantity to use for changing the weights to make the behavior of the network in phase 2 (when it is deciding for itself) mimic the behavior in phase 1 (when it is being forced to behave in the desired way). To prove this it is necessary to define a measure of the difference between the probability distribution that is forced on the network in phase 1 and the probability distribution that it exhibits in phase 2. Once the correct measure has been defined, it can be shown that the measure is decreased by changing each weight according to the above procedure. The proof can be found in reference 3.

Figure 1 shows what the learning procedure can do when the task is to "recognize" the shift that was applied to one 8-bit vector to produce a second 8-bit vector. If you think this is an easy problem, remember that the network starts off with no preconceptions. It has no idea that neighboring input bits will have anything to do with each other, and it is not expecting this task any more than it is expecting any other. If the very same network is presented with a completely different combination of input and output vectors, it will create a different set of feature detectors that are appropriate for the different task.

Making It Faster

The first learning algorithm I described just changes weights to make units behave in prespecified ways. It cannot figure out what to do with internal units whose required behavior is not specified from outside. The second learning algorithm is potentially much more powerful because it is able to decide how to use the internal units to help achieve the required I/O mapping. It actually constructs simple internal representations. Unfortunately, there is a heavy price to pay for this added power. The algorithm is currently extremely slow; the example in figure 1 requires hours of computer time.

To speed things up, Blake Ward, a graduate student at Carnegie-Mellon, has built a parallel machine containing six Omnibyte 68000 boards, each of which has a copy of the entire network. Each board runs with a different input vector, and then all the boards agree on how to change the weights. This helps, but ultimately we would like to implement networks of these probabilistic units directly in silicon. Unlike current computers, these networks are rather tolerant of localized hardware failures or fabrication errors; Carver Mead has pointed out that an analog implementation of the processing elements would positively thrive on the kind of thermal noise that comes from running transistors at very low power. This might make it possible to build much larger chips than is currently feasible. However, developments like this are still a long way off, and they do not remove the need for more theoretical progress. Our current simulations are slow for three reasons: It is inefficient to simulate parallel networks with serial machines, it takes many decisions by each unit before a big network approaches equilibrium, and it takes an inordinate number of examples of I/O pairs before a network can figure out what to represent with its internal units. Better hardware might solve the first problem, but more theoretical progress is needed on the other two. Only then will we be able to apply this kind of learning network to more realistic problems. ■

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BY JEROME A. FELDMAN

Massive parallelism in natural and artificial intelligence

A FUNDAMENTAL PREMISE of artificial intelligence (AI) is that intelligent behavior can be simulated on digital computers. Great progress has been made in AI, with far-reaching practical and scientific consequences. Despite successes with quite specific problems, however, many researchers feel that the general questions of intelligence have barely been touched. The field of AI is nowhere near possessing the ability to simulate the natural intelligence of a small child or even a simple animal. Yet the basic computing speed of modern computers is about a million times faster than the firing rate of a neuron, which is in the millisecond range.

The situation becomes even more striking when we consider the speed of human responses on simple tasks. When asked to carry out a wide range of tasks, such as naming a picture or deciding if some sound is an English noun, people can respond correctly in about half a second. This means that the brain, a device composed of neural elements with a basic computing speed of a few milliseconds, can solve difficult problems of vision and language in a few hundred milliseconds (0.5 second = 500 milliseconds), or about 100 steps. The best AI programs for these tasks are not nearly as general and require millions of computational time steps. Of course, the brain is a parallel device, while essentially all of our existing machines are sequential, executing one instruction at a time. But what are the algorithms used in this massively parallel natural computer?

The exploration of possible algorithms for this radically different architecture forms the cornerstone of a promising new branch of artificial intelligence. Workers in the field use an abstract computer that is as similar as possible to the brain in structure and performance. This approach permits AI researchers to collaborate closely with colleagues in the brain and behavioral sciences; a good algorithm for some task on a computational model can also serve as a prototype theory for the mechanisms the brain uses on the same problem. Some psychologists have found that constructing massively parallel computational models to fit their data is far easier than constructing models based on sequential machines. The cycle is complete when AI researchers use experimental results to guide the construction of parallel algorithms for various problems.

In addition to the 100-step restriction, using the brain as a model has other computational consequences. For one thing, the timing constraints limit to a few bits the information that can be sent from one neuron to another. This means that units cannot pass the large symbolic structures common in AI and that the computational richness must lie in the connections among units; this has led to the use of the term "connectionist" to characterize these models.

Using the brain as a model does allow for quite a lot of connections, up to about 10,000 per unit. The total number of neurons (about 100 billion) seems large but is actually a major limitation. Since vision has a million parallel inputs, any algorithm requiring n^2 units would not fit. Also, the brain grows no new units and essen-

(continued)

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tially no new connections, placing severe constraints on models of learning. Even with all these constraints, connectionist models are increasingly popular in AI research.

A VISUAL MODEL

A simple example can capture some of the flavor of connectionist computation. The cube shown in figure 1 is a famous optical illusion attributed to the Swiss naturalist L. A. Necker (1832). Most people initially see the cube with the corner G closer to them, but you can also see it as a cube with vertex A closest to you. If you focus on vertex A and imagine it coming out of the paper toward you, the picture will flip to the A-closer cube. Notice that the flip takes less than a second. The Necker cube is interesting to psychologists because it will flip spontaneously between the two views if you keep looking at it. It is interesting to artificial-intelligence researchers because of what it tells us about parallel computation.

You have observed how quickly the Necker cube flips, and you know how slow the underlying human computing elements are. A sequential program running on such a slow device could probably not perform this task. But the situation is much more complex. Both human and computer vision require several levels of processing (see "Vision" by Dana H. Ballard and Christopher M. Brown on page 245). Typical levels include edge segments, lines, vertices, faces, and object descriptions. The edges and lines are the same for both the A-closer and G-closer cubes, but many other visual features are seen differently in the two views. A few of these are given in figure 2. Remarkably, our visual system simultaneously flips all these perceptual decisions from one mutually consistent reading of the cube to the other. This illustrates the key cooperative property of massively parallel computation and why it is conceptually different from von Neumann computation on standard machines.

The Necker cube also illustrates some of the details of the connectionist paradigm, as shown in figure 2. In our models each item of interest is represented as a computational unit, with connections to many other units. Each unit has a level of activity (say between −10 and +10) and automatically sends the value of this activity along all its outgoing connections. In the network of figure 2, units that are mutually consistent (for example, "H closer than G" and "G hidden") have connections to each other. Units that are mutually exclusive, such as "G hidden" and "G showing" are connected with circle-tipped links denoting negative connections. The only other information needed for a complete model is the rule by which a unit computes its new activity from its inputs and its old activity. We can assume that the units compute the average of their positive and negative inputs. Networks like figure 2 are not very sensitive to the exact choice of unit computation rules; this is one of the reasons for their attractiveness. Units that are all mutually connected by negative links are said to comprise a "winner-take-all" network. Such networks are one of the main decision mechanisms in connectionist models and have known neurophysiological analogs.

Much of the effort in massively parallel AI is dedicated to using computational frameworks like that in figure 2 to build models of intelligent activity. Advantages of this approach include its link to natural intelligence, increased noise resistance, and ease of implementation on parallel hardware. But the main advantage of the connectionist approach is that it provides a much better way of specifying some computations. I know of no other way to describe the Necker-cube phenomenon that is as clear and concise as the model in figure 2.

A NATURAL-LANGUAGE APPLICATION

Researchers in AI and related areas of cognitive science are using connectionist models to study a variety of tasks. Vision is an area where massive parallelism fits naturally. Ballard and Brown's article describes some of the success in that area. The methodology is also effective in natural-language research. Although it is a less obvious application, researchers have had some very nice results in that domain.

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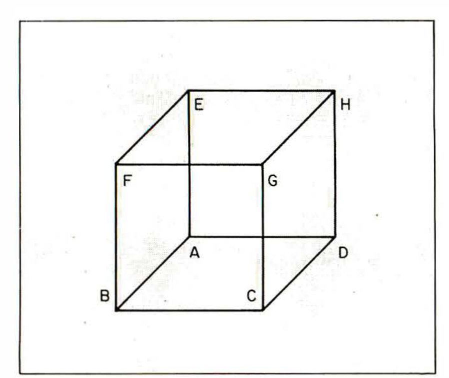


Figure 1: *The optically illusive Necker cube. Is point A closer to you than point G, or vice versa?*

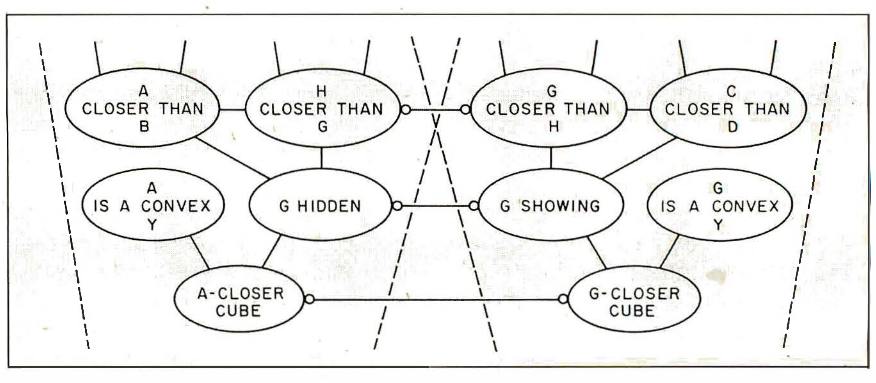
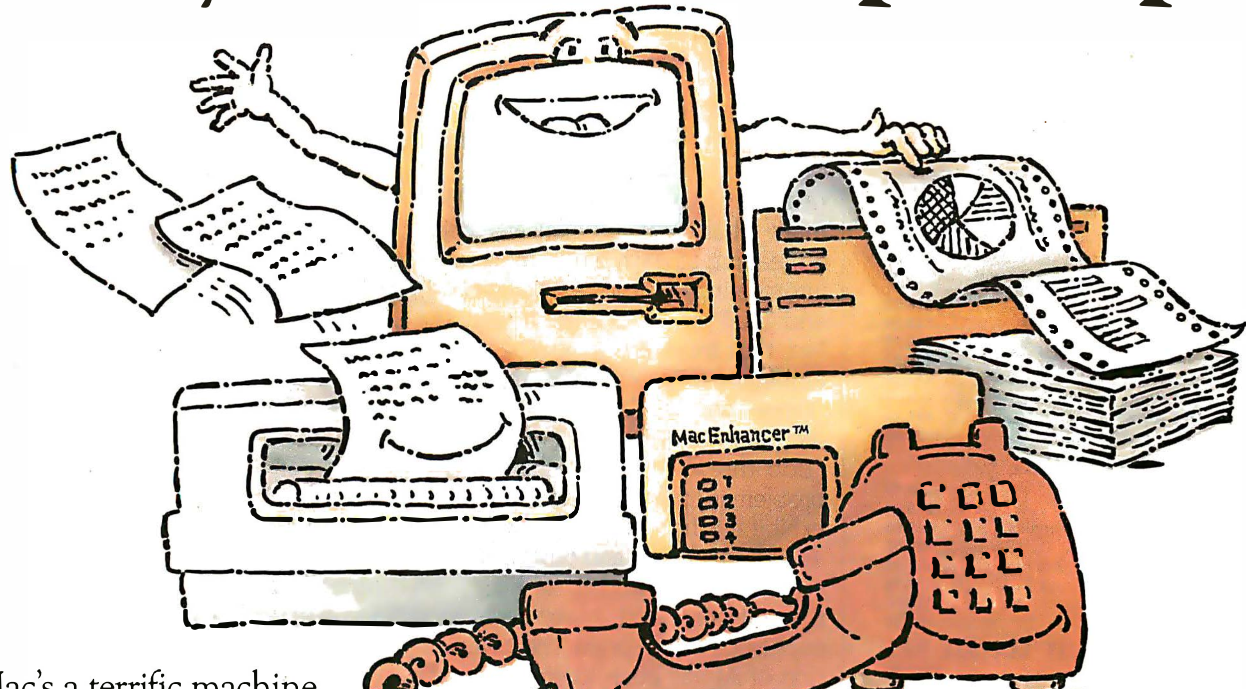


Figure 2: *A connectionist model illustrating the process of understanding the cube in figure 1.*

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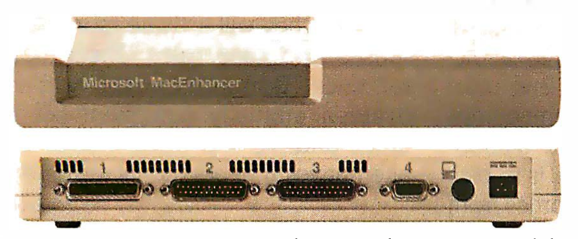


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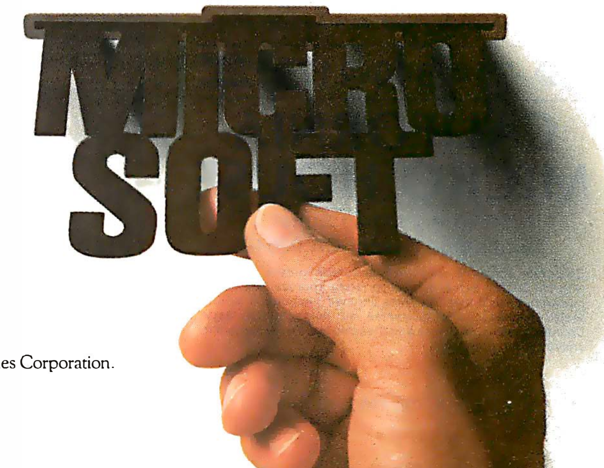
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One problem that has worked out particularly well is disambiguation. Consider what happens when you hear or read a sentence such as: "Bob threw a ball." You automatically assign a meaning to each word, most likely interpreting "threw" as "propelled" and "ball" as "a sphere," despite the fact that most words in English are ambiguous. For example, the words "threw" and "ball" both suggest quite different meanings in the sentence "Bob threw a ball for charity." The problem is to develop algorithms that exhibit this behavior and help explain its basis. Linguists and other cognitive scientists have worked at length on these issues and have developed sophisticated theories. The contribution of AI has been to encode these theories in programs so that they can be tested and, if correct, used in applications. As with the Necker-cube example, massively parallel models appear to constitute the best way to carry out the encoding.

In language, as in vision, the theory calls for several distinct levels of representation and processing. Figure 3 shows three of these levels. The *lexical level* comes after the individual sounds or letters have been formed into words; this level corresponds to what you would look up in a dictionary. The *word-sense level* corresponds to the various meanings listed under a word in the dictionary—the problem, of course, is to pick the right one. The *case level* comes from linguistic theory and conveys the idea of the different roles that words can play in a sentence. The cases used here are

- agent: the person or thing carrying out an action
- object: the thing acted upon
- recipient: beneficiary of the action

The key linguistic insight is that there are constraints on the possible word senses that can fill various case roles. For example, you cannot throw (propel) a ball (dance), so these are incompatible. Nor can you throw (sponsor) a ball (sphere). The only other fact used in the model is that some word senses are more frequent than others.

We can now see how figure 3 presents a connectionist computational model of disambiguation. As with the Necker cube, compatible units have positive links and incompatible units have negative, winner-take-all, links. The model assumes that as each word reaches the lexical level it spreads activity to the various word senses to which it is connected. Since the more frequent sense has a greater weight, it will tend to dominate less frequent senses. As additional words come in, they will activate more word senses and case roles. The simple sentence "Bob threw a ball" will activate a mutually consistent set of units, and we will never notice the alternatives. The additional words "for

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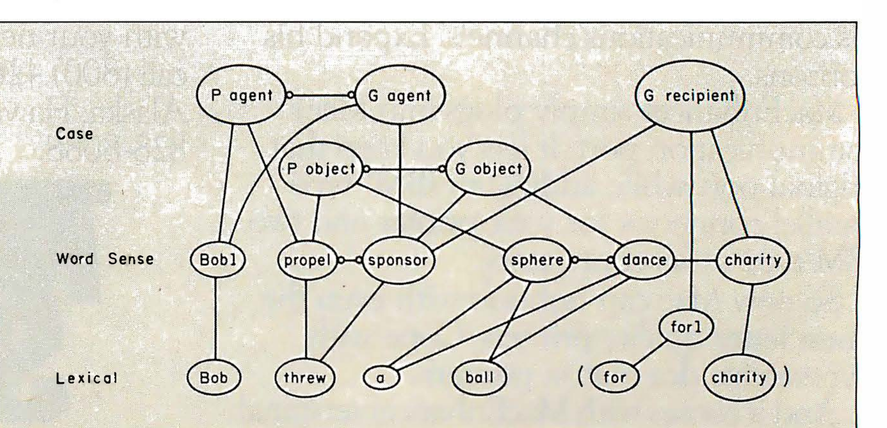


Figure 3: *A connectionist model for understanding the sentence "Bob threw a ball (for charity)." The model uses three levels of representation and processing.*


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charity" will activate the "dance" meaning of ball. This will weaken the "sphere" meaning, which will in turn reduce the activity of "propel" because the sentence no longer has a suitable object. Thus, an alternative stable coalition develops and suppresses the original interpretation. The two alternative coalitions are quite similar to the two readings of the Necker cube. This is no accident—the idea of a cooperative-competitive network pervades parallel models. Work on language problems such as disambiguation is quite advanced and offers simple explanations of many phenomena. For example, a context that biased us toward the "dance" sense of ball would be modeled as providing that meaning with a head start in its competition with "sphere." Again, the massively parallel paradigm is the simplest way to express this idea.

KNOWLEDGE REPRESENTATION

The Necker-cube and disambiguation examples are both instances of what AI researchers call recognition problems. Several other problems are like this, but many are not. Can we apply massively parallel models to other traditional AI issues such as knowledge representation and inference? Researchers have completed much less work along these lines but have made some promising starts. The example in figure 4 should convey the flavor of this work.

The standard way to explore the issue of knowledge representation and inference is in terms of programs that can answer questions. AI approaches to the development of question-answering systems are numerous (Roger Schank and Larry Hunter present one in "The Quest to Understand Thinking" on page 143), but the approaches all have the same basic requirements: You need a way to store the knowledge, to pose questions, and to compute and register the answers. In a connectionist model, all of these aspects must be expressed in terms of activity spreading among simple units like those in the previous examples.

It is easiest to start with the recording of answers. In figure 4, the possible tastes of foods form a winner-take-all network, where each unit inhibits the others so only one answer will be active. The answer network is assumed to be part of a routine that also poses the questions and acts upon the answer. The units that make up the routine are assumed to be activated in sequence from left to right just like a standard program. The routine sends a question to the knowledge network by activating the appropriate units; figure 4 shows this as links, for example, from the hexagonal node to the nodes for "has-taste" and "ham." The key to the operation of this network is the operation of the triangular-shaped nodes, such as "b1." We define such a triangular unit to become active when two of its inputs are simultaneously active. In this case "ham" and "has-taste" are both on, so "b1" becomes active and activates "salty." Now the "salty" node in the knowledge network spreads activation to the response "r-salty" back in the routine and the question is answered. The same network can answer questions such as "Name a salty meat" when activated appropriately. The answers returned by such a network will depend on context, just as people's answers do; contextual bias is again modeled by activation.

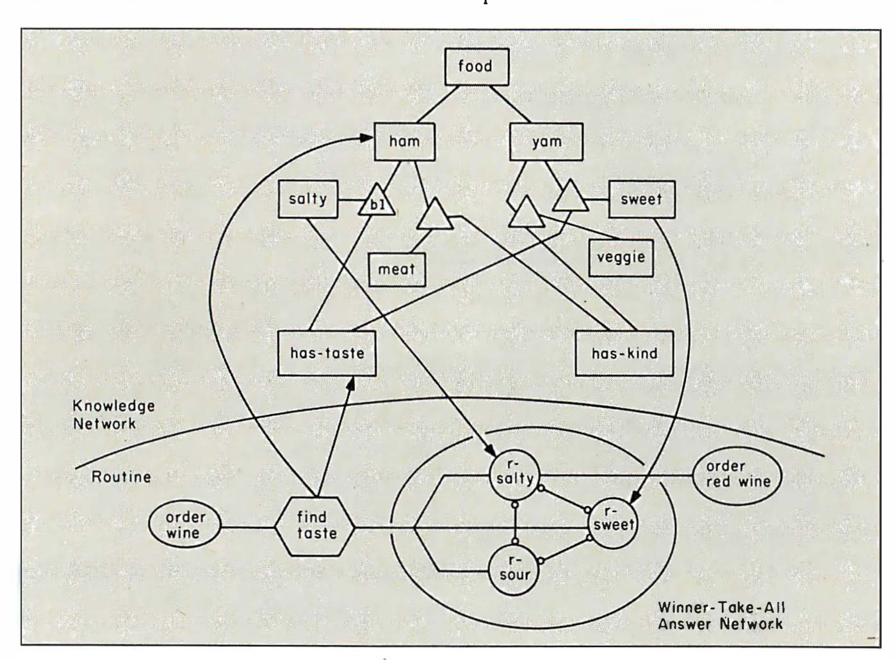


Figure 4: *Interaction between a knowledge network and a routine.*

The examples of cube perception, word disambiguation, and question answering are typical of the current applications of massively parallel computational models in AI. The examples are condensed and they omit many important considerations, but they are representative of the current level of attainment. In no case are the connectionist programs as sophisticated as conventional AI systems for similar tasks. The general notion of massively parallel models in AI is quite new, and we do not yet understand where its ultimate strengths and weaknesses will lie. We do know that the development of highly parallel computers will have a marked effect on the practicality of connectionist approaches to AI.

Even if we had discovered parallel algorithms for vision and language tasks and could run them efficiently on parallel hardware, we would be missing a crucial element of intelligence—learning. No system that cannot incorporate new knowledge and change its behavior could be called intelligent. This is an important issue

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for all of AI but is especially critical for connectionist models. If we model our system as a set of rules, we'll have no conceptual difficulty in adding more rules, although the question of which rules to add remains unsolved. For connectionist models, the intelligence is in the connections—but we know that the brain grows essentially no new connections. How could such a system, even in principle, incorporate new knowledge?

The neural substrate of memory and learning is one of the great unsolved scientific questions for which we certainly have no definitive answers. But connectionist theories of learning are compatible with current brain research and are computationally feasible. The key idea is that while new connections are rare, *weight change* in connections appears to be common. We also know that each unit can have thousands of incoming and outgoing connections. Our hypothesis is that most of these connections are only potentially important and that learning involves strengthening the appropriate connections. Suppose, for example, the network of figure 4 needed to learn that spinach was a salty vegetable. Our model suggests that there are uncommitted triangular nodes that are weakly connected to many combinations of objects, properties, and values. In an ideal case, one of them will be linked to "spinach," "has-taste," and "salty," among other things. This unit will become highly activated by the simultaneous activation of three of its neighbors and, by strengthening its active connections, can become dedicated to the new association. This example omits many important issues; the whole learning theory is in a very primitive stage. Geoffrey Hinton, in the article "Learning in Parallel Networks" (page 265), describes a related but different learning scheme based on the assumption that concepts are represented diffusely as the activity of many, many units. All of the connectionist AI efforts badly need more theoretical and experimental work, which leads us to an active interest in parallel computers.

PARALLEL COMPUTERS

Clearly, massively parallel AI models have a natural fit to parallel computers. The speed of our current simulations on sequential machines is slow enough to be a major bottleneck. While some kinds of programs are hard to transfer to parallel computers, connectionist simulations are straightforward to move. If we have 100 processors and a network of 20,000 units to simulate, we just assign 200 units to each processor. There are technical questions about the best way to partition the network, but the basic idea is simple. It is less clear how to monitor and modify the behavior of such systems, and this leads to basic research questions in parallel computation. A number of machines with hundreds of processors are being built in various labs. Our group at the University of Rochester is working with the Butterfly multiprocessor of Bolt Beranek and Newman; we expect to have a 128-processor system running this summer. A parallel version of our connectionist simulator is one of the major driving applications for the Butterfly.

Possibly the best way to program many problems for a multiprocessor is to express them as a massively parallel network. While breaking a problem into 256 equal pieces is difficult, it may be fairly easy to express the problem's natural parallelism and let a compiler map the result onto whatever hardware is available. This seems to be the experience of the Cal Tech group on the physics problems they have attacked, and it appears to be true for many AI problems. The success of this approach could be a coincidence, but it might be related to the fact that intelligence evolved on massively parallel hardware. ■



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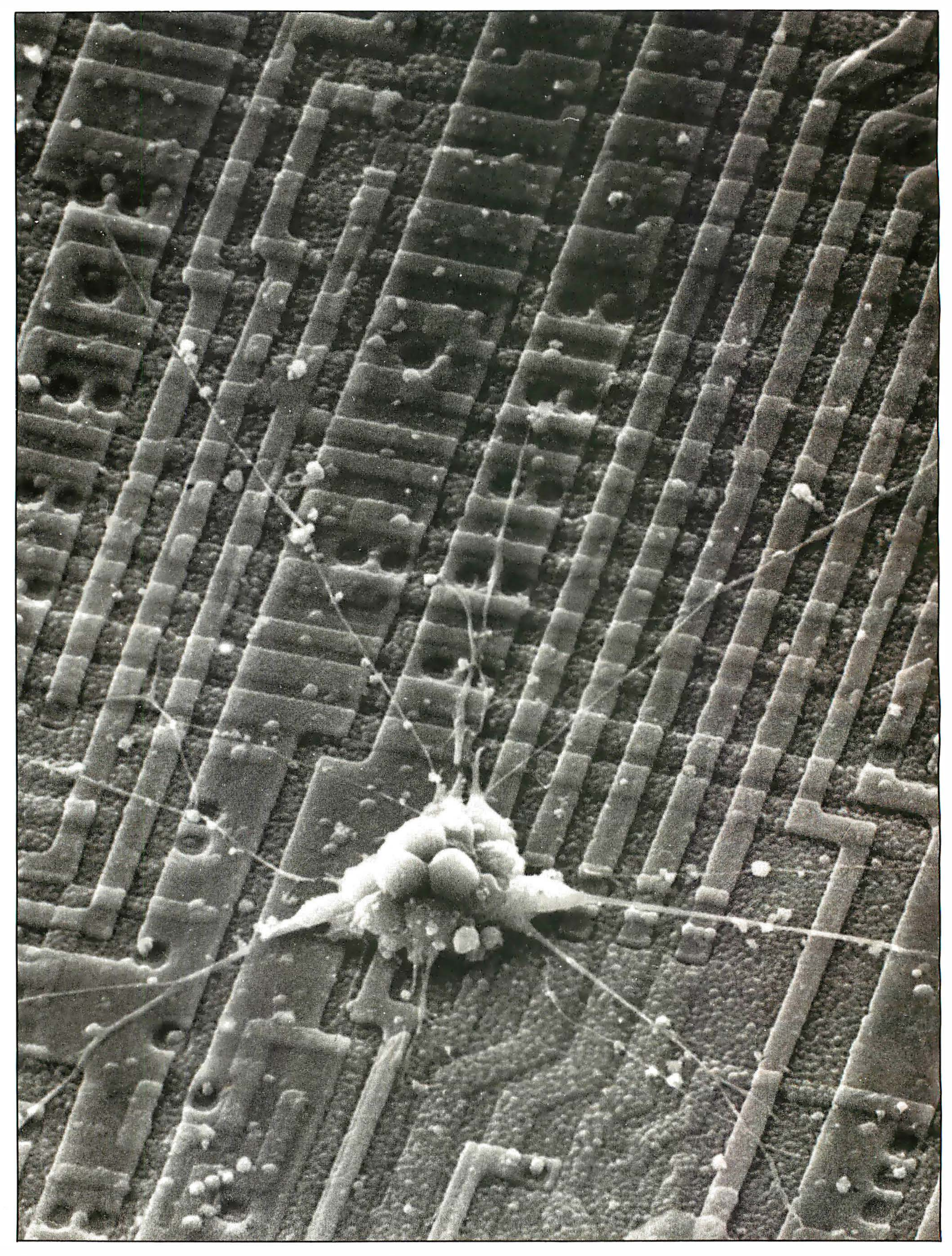


Photo 1: A *scanning electron micrograph of brain cells grown in tissue culture on a* Motorola 68000. *The center clump of balls is a group of somas, and the thin lines radiating outward from the clump are the neural processes. The* IC *traces are 2 to 5 microns across, and the traces on the nerve processes taper to less than* 0.2 *micron across.*

MICROGRAPH TAKEN BY JUDY TROGADIS. FOR MORE DETAILS SEE PAGE 299.

REVERSE ENGINEERING THE BRAIN

BY JOHN K. STEVENS

Chipping away at the brain

COULD WE DEVELOP more efficient "sixth-generation" artificial-intelligence (AI) computers using circuitry copied directly from the brain, perhaps using radical new architecture, new hardware, and an entirely new logic? This question seems to have been raised about once a year for the last two decades. The answer continues to be "Probably not right away," but as our understanding of principles used in neural processing evolves, it is a possibility that must be taken seriously. Moreover, some new digital designs such as the Boltzmann machines (see "Learning in Parallel Networks" by Geoffrey E. Hinton on page 265) closely parallel the overall architecture of the brain.

First we will review what might be called the device physics of the brain, focusing on the physical and electrical principles that optical nerve cells use to process information. Then we will discuss how silicon-based designs might be adapted to make use of the brain's approach and how such designs might be used in some high-speed processing applications.

While today's digital hardware is extremely impressive, it is clear that the human retina's real-time performance goes unchallenged (table 1). Actually, to simulate 10 milliseconds (ms) of the complete processing of even a single nerve cell from the retina would require the solution of about 500 simultaneous nonlinear differential equations 100 times and would take at least several minutes of processing time on a Cray supercomputer. Keeping in mind that there are 10 million or more such cells interacting with each other in complex ways, it would take a minimum of 100 years of Cray time to simulate what takes place in your eye many times every second. How does this impressive piece of "bio-ware" work?

A BRIEF INTRODUCTION TO NERVE CELLS

The retina's nerve cells function as complex analog processors. The connections between these cells, the characteristics of their connections, and the shape of the cells themselves all seem to play a major role in determining the basic parameters of the analog processing "program."

Nerve cells come in many different shapes and sizes, but they can be placed into two broad categories—local processing "interneuron" cells and output cells. The local processing cells have all of their inputs and outputs limited to a very small region (usually a few hundred microns), while the output cells communicate from one part of the brain to another, from the brain to muscle, or from sensory organs to the brain.

The nerve cell, or *neuron*, can be thought of as a stand-alone analog-logical processing unit. Each cell has an inside and an outside separated by a plasma membrane. The inside of the cell and the fluid surrounding the cell have different concentrations of

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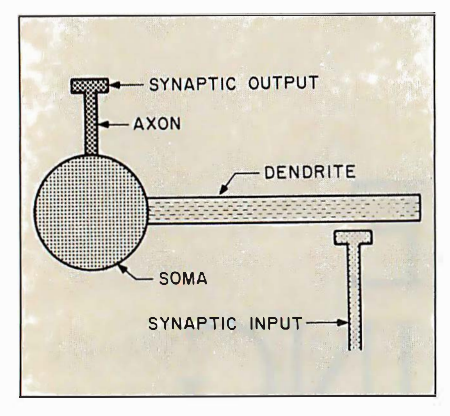


Figure 1: *A summary overview of a typical nerve cell.*

charged ions, which creates a potential difference across the membrane. The concentration of the inside ions is controlled by many "ion pumps" located in the membrane itself. The ion concentration of the fluid surrounding the cell is just filtered blood and is regulated by special ion pumps found in the kidneys. These differential ion concentrations provide the electrical energy for all nerve cells and are exactly analogous to a battery. The full circuit requires a resistor in series with the battery to represent the ion leakage across the plasma membrane. The active pumps in the cell's membrane and kidneys are analogous to a battery charger, but instead of using a 110-volt wall plug, they use glucose or other nutrients as the power source.

Table 1: *A comparison of specifications for a hypothetical image-processing system using state-of-the-art integrated circuitry and the human retina.*

Specification	Typical IC Product	Retina
circuit layout	two-dimensional	three-dimensional
IC line width	1–3 microns	0.1–1.0 micron
number of gates	approx. 1,000,000	approx. 25,000,000,000
resolution (pixels)	2048 × 2048	10,000 × 10,000
PC board trace width	250 microns	0.2–3.0 microns
power consumption	200–300 watts	0.001 watts
system volume	approx. 10,000 cu.in.	approx. .0003 cu.in.
total weight	20,000–50,000 g	<1 g.

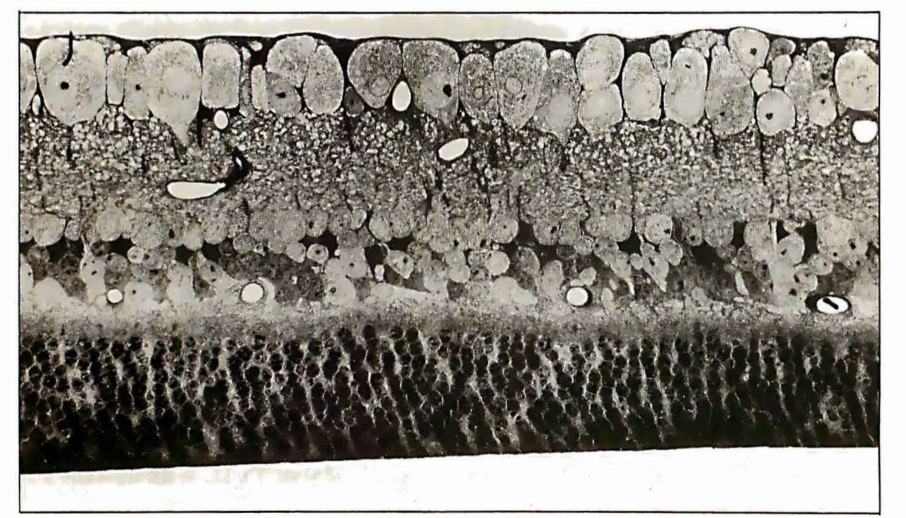


Photo 2: *An electron micrograph of a cross-section of retina about 0.1 micron thick and about 200 microns by 500 microns across. The light would activate the receptors (located at the bottom of the picture), and the final output would come from the top at the ganglion cells. The large round objects are somas, or cell bodies, and the very small profiles layered between the cells are nerve processes that make synaptic contacts with each other. Sequential series of the micrographs are used to reconstruct cells similar to those seen in figure 7.*

The Soma

Each cell has a large round central body called a *soma* (photos 1 and 2, figure 1) that contains the genetic and metabolic machinery necessary to keep the cell alive. The soma takes the glucose found in the surrounding fluid and converts it to a more usable form of energy called ATP (adenosine triphosphate). The ATP drives the active pumps directly. The soma also synthesizes lipids and proteins that are used to maintain the cell's membrane, synapses, gates, and the nerve-process skeleton (cytoskeleton).

The Passive Dendrite

Attached to the soma are long, irregularly shaped nerve processes (hairlike projections) called *dendrites*. These dendrites often have diameters under 1 micron and extremely complex branching shapes. Dendrites are electrically passive and can be represented as a series of capacitors and resistors. Their primary function is to receive inputs from other cells via specialized contacts called *synapses* or to connect other dendrites to synaptic outputs. One very important point that we will discuss in some detail is that the shape of a dendrite can have a dramatic effect upon the time course and final potential of any synaptic input. Thus, the same synaptic input on two differently shaped dendrites can have dramatically different effects. Synaptic inputs on a dendrite can either be summed and passively conducted to local synaptic outputs located on the same dendrite (in interneurons) or passively conducted back to the soma, where an action potential may be initiated in output cells.

The Active Axon

A second type of nerve process also attached to the soma is called an *axon*. The axon differs from the dendrite in that it is electrically active and can

serve as the final output channel of the cell. Axons are always found on the output cells but often do not appear on interneurons, particularly on interneurons that have both inputs and outputs on dendrites. The axon is a nonlinear threshold device that produces a rapid, all-or-none voltage increase and decrease of about 1-ms duration. This voltage pulse, which is called an *action potential*, has a fixed amplitude and occurs when the resting potential within the soma rises above a critical threshold. The rapid changes in potential associated with the action potential are due to specialized proteins contained in the axon's membrane that selectively allow sodium and potassium ions to flow across the membrane, down their concentration gradients. You might think of these action potential gates as simply a series of interconnected one-shots.

Anatomically, the gates begin on the soma just before the actual axon leaves the cell. When the synaptic inputs located on the dendrite of a cell are activated, the potential may be passively conducted to the soma near the axon. If the sum total of all of these inputs as seen by the soma or axon is above the threshold of these gates, they will be activated and produce an action potential. Once this first group of gates has been activated, they change the internal axonal potential even more and activate the next set of gates located farther down the axon. These more distant gates raise the axonal potential again and activate even more distant gates, and so on, for the entire length of the axon, up to many feet in total length.

Synaptic Inputs and Outputs

Axons terminate in specialized contacts, called synapses, on other nerve cells. Synapses make contact with the dendrites of other cells and are capable of changing a dendrite's local potential in a positive or negative direction. When the potential on the axonal side (the presynaptic side) is raised, special compounds called neurotransmitters are released. Their release seems to be graded as a function of the presynaptic voltage waveform. Neurotransmitters are capable of opening gates similar to those described above for the action potential, except that these gates are located on the dendritic membrane and are activated chemically. When a synaptic gate is open, it selectively allows charged ions to flow across the membrane, either into or out of the cell. This in turn changes the internal dendritic potential. The total number of gates opened depends upon the total number of transmitter molecules released. A given synapse may excite or inhibit a cell. A single cell will always have many synaptic inputs on its dendrites and may have many synaptic outputs on its axons or dendrites to many different cells.

The output synapses from output cells are always located on the end of an axon. However, the output synapses from interneurons are located on the passive dendrites near the input synapses. Since the action potential has a fixed waveform, the synaptic outputs from the axon of an output cell will also have a fixed waveform. In contrast, since the potentials inside a dendrite are graded analog signals (due to analog summation of many different synaptic inputs), the interneuron synaptic outputs may also be graded. Thus, output cells have graded analog inputs with digital, all-or-none final outputs; interneurons have graded analog inputs but also have graded analog outputs.

The Methods

Advanced recording methods that depend upon submicron electrodes placed near individual cells in living brains and in tissue culture have taught us a great deal about the function or what could be called the software and hardware of brain cells. These electrodes make it possible to record action potentials and in many cases penetrate the soma and record intracellular potentials from synapses that have been activated on a peripheral dendrite. It has also been possible through other methods to measure the physical characteristics and properties of nerve cells, individual portions of cells, and even the properties of membranes and proteins embedded in the mem-

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branes. Until recently, it has been difficult to incorporate these physical parameters into a comprehensive model of submicron device physics, or what we call the design rules of the brain.

As I mentioned, the shape of nerve-cell processes plays an important role in controlling their function. Unfortunately, these processes are almost always well below 1 micron in diameter. A major difficulty has been that to accurately create an electrical or physical model of a nerve cell requires a detailed knowledge of surface area, length, and branching patterns of all processes and location of synaptic inputs. Because the cells are small and have extremely complex three-dimensional geometries, these parameters cannot be accurately obtained using the light microscope, which has a resolution of only about 1 micron. The scanning electron microscope allows us to see cells at higher resolution, but the cells must be removed from their circuit in the brain and placed on a special flat substrate or grown in tissue culture directly on the substrate.

Thus, scanning microscopes cannot be used to analyze intact three-dimensional circuits of the brain. The transmission electron microscope has more than adequate resolution. But to see the cells at high resolution, they must be sliced into very thin sections, usually less than 0.1 micron (photo 2). Thus, while the submicron structure can be resolved, the three-dimensional structure of the cells is lost.

The solution has been to simply slice the brain into thin serial sections and then, by using special computer systems, to reassemble the individual cross-sections into a full three-dimensional reconstruction of the original object (figure 2). Technological advances over the last few years have made this almost routine, so it

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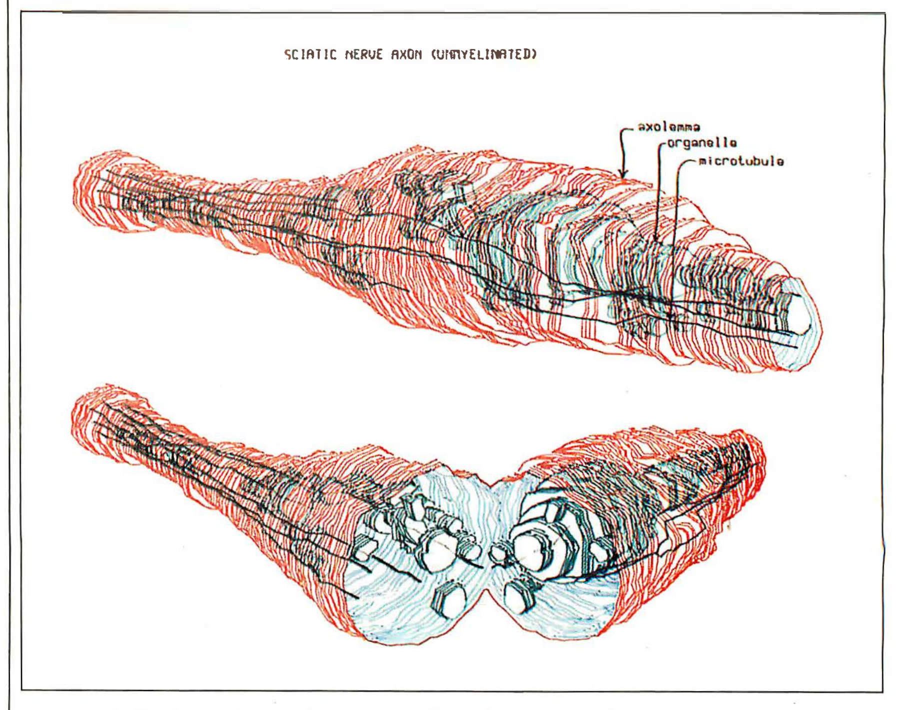


Figure 2: *Electron microscopic reconstruction of an axon. The internal structure of a dendrite would be similar. The long tubes (microtubules) and round green objects (organelles) play a role in controlling the local geometry of the nerve process. This process, reconstructed by M. Greenberg (Playfair), has a diameter of about 1 micron. Reprinted by permission of Academic Press from* Advances in Cellular Neurobiology *(see Bibliography).*

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is now possible to study the structures inside the cells that control shape and thus control the device physics of the cells.

Creating Equivalent Circuits

Each of the various nerve-cell components described above has an electrical circuit equivalent. If you combine this electrical equivalent with the submicron three-dimensional geometry of the cell, it is possible to create reasonably accurate models of nerve-cell processing. In what follows I will illustrate the principles used by nerve cells for processing signals by describing the electrical equivalents for a dendrite, the power supply, and the synaptic contact. I will also show how the shape of a cell's processes can alter inputs and outputs and how the cell's internal skeleton can alter process shape. It is also possible to create an equivalent circuit for the axon, but for the sake of simplicity I will limit myself to the passive portions of the nerve cell and will not discuss the electrical properties of the axon.

The Form and Electrical Circuits of the Passive Dendrite

Brain-cell dendrites have a skeleton that controls the shape and, to some extent, the branching patterns of the process. As I will discuss below, this skeleton is particularly important in controlling how a brain cell processes information. The dendrite has an outer skin, or membrane, that consists of a very thin layer of oil-like substances called *phospholipids*. Phospholipids have high specific resistivity and capacitance and can be thought of as insulators. The inside of the nerve-cell process is filled with a highly conductive gel, or *axoplasm*, that for our purposes can be thought of as a conducting wire. Thus, a nerve-cell dendrite in the most simple electrical terms is a conducting wire, the axoplasm, with an outer insulating layer, the membrane. The nerve process can be represented with simple electrical equivalents consisting of a ladder network of passive resistors and capacitors.

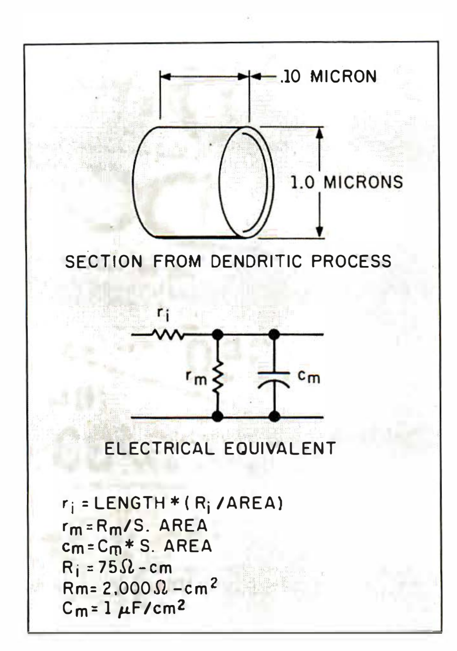


Figure 3: *Electrical equivalent of a dendritic circuit. The dendrite segment is about 0.1 micron in diameter. S.area= surface area of the cylinder and area= cross-sectional area.*

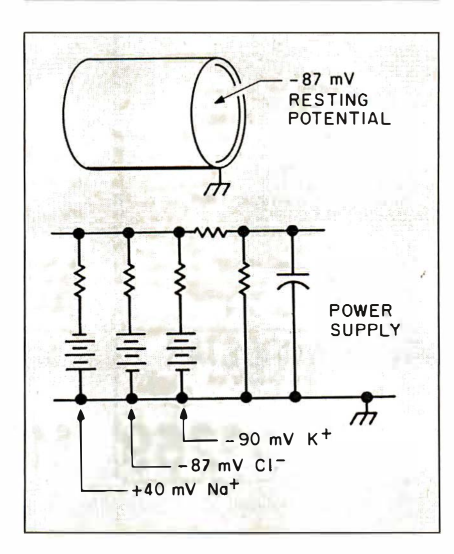


Figure 4: *Electrical equivalent of the power supply of a nerve cell. The differences in voltages between this figure and the text reflect normal ranges of cell potentials.*

A simple model of a portion of a dendrite is shown in figure 3. Below the model is the equivalent ladder network of resistors and capacitors that represent that model. The resistor labeled r_m is the resistor used to represent leakage out of the membrane, while the resistor labeled R_i is the resistance offered by the internal gel or cytoplasm. Finally, c_m is the capacitive component of the membrane. These values are calculated from specific resistivities that have been experimentally measured for different cell types and by measuring the detailed geometry of the cell itself. The computation is virtually identical to that now used by IC (integrated-circuit) designers in calculating resistances and capacitances on a chip. IC designers know the specific resistivity of polysilicon, silicon, and metal layers. When given the geometry of a pad, they can compute its total resistance and capacitance.

The specific capacitance of the phospholipids that make up the dendrite's membrane is about 1 microfarad per square centimeter. Thus, we measure the surface area of one small region of the process and multiply it by the specific membrane capacity. The dendritic portion in figure 3 would have a total capacitance of 1.57×10^{-9} microfarad, a membrane resistance of 1.27×10^{12} ohms, and an axial resistance of 9.55×10^{4} ohms.

The Nerve-Cell Power-Supply Circuit

The power supply for a cell can be represented as a series of batteries in series with a resistor (figure 4). Each battery represents the differential concentration across the cell's membrane of a specific ion. The voltage of the battery for a specific ion is determined directly by its Nernst equilibrium constant, which is given as

$$\text{millivoltage} = 61 \times \text{Log}(|OUT|/|IN|)$$

The concentration of the positively charged ion Na^+ is much higher outside the cell than it is inside the cell by a ratio of about 10:1. Its Nernst equilibrium potential is therefore +61 millivolts (mV). Other ions typically found around cells in warm-blooded animals are K^+, with a Nernst equilibrium potential of about −90

(continued)

mV (minus because the concentration of K^+ is greater on the inside of the cell), and Cl^-, with a potential of −87 mV. The series resistors shown in figure 4 represent leakage of these ions across the membrane to charge the capacitor to its final value. Using special recording methods, it is possible to determine the value of each leakage resistor. Once that is known, we can quickly compute that the potential difference across the membrane will be about −87 mV.

Since this "resting potential" is relatively constant throughout the cell, it is usually not explicitly included in the models or computations. However, the principle of using ionic gradients and membrane resistance to create potential differences is important and will be used below in the description of synapses.

The Synapse or Neural Gate Circuit

You might think of synaptic inputs as voltage-controlled changes in the membrane resistor connected to an ionic battery. In some cases the battery may be positive and thus produce a net excitatory change inside the dendrites, and in other cases the battery may be negative and thus produce net inhibition inside the cell. Figure 5 illustrates a schematic synapse making contact with a dendrite. When the voltage inside the synapse increases, neurotransmitters are released. These neurotransmitters selectively (depending upon their chemical composition) alter the permeability of one or more ions. In effect, these neurotransmitters change the value of the resistor connected to an ionic battery that in turn leads to a change in the resting potential of the cell. A typical gate might have 5.0×10^{12} ohms resting value and 5.0×10^8 ohms during activation.

One important point is that a synapse cannot be modeled as a simple voltage input to the dendrite, nor can it be safely represented as a simple injection of current. Rather, it is a complex conductance change within a complex passive RC (resistance-capacitance) network. The final time course and potential seen across the cell's membrane will therefore not be just a function of the synaptic battery and resistor but also of the membrane resistor (r_m), axial resistor (r_i), and membrane capacitor (c_m). Since these components are controlled to some extent by the shape of the cell, the geometry of the cell can be used to control synaptic strength. This principle is illustrated below.

The Retinal Amacrine Cell Electrical Circuit

Figure 7 illustrates a retinal amacrine cell, reconstructed by the computer from serial electron micrographs. The amacrine cell is of particular interest because it has a complex geometry that includes highly irregular and varicose dendrites that attach to the soma. It is a classic interneuron with many synaptic inputs and outputs over the entire cell's surface, and no axon.

Once the surface area and volumes have been computed, the cell is reduced to a simple geometric schematic that approximates the original shape using cylinders similar to those shown in figure 7. You can then easily reduce this schematic to an equivalent circuit by using a membrane resistor, axial resistor, and membrane capacitor to create a large RC ladder network similar to that seen in figure 6. This network can be simulated using conventional linear circuit analysis (see October 1978 BYTE) on almost any small computer.

I have simulated the cell shown in figure 7 using two identical synapses placed on different parts of the cell (A and B in figure 8). I have not included the batteries and resting potential resistors since they would all be equal in this circuit. The synaptic inputs consist of a resistor and a 100-mV battery as shown in figure 5. A synaptic input is modeled as a rapid decrease in the value of the synaptic resistor for 50 ms and then a return to a very high resting value. The lower

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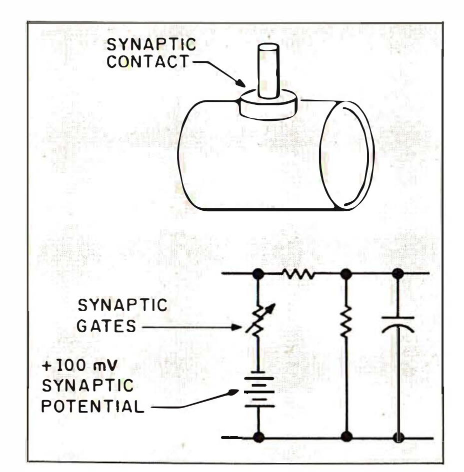


Figure 5: *Electrical equivalent of a synaptic gate. We use an arbitrary battery of 100 mV in our models of nerve cells.*

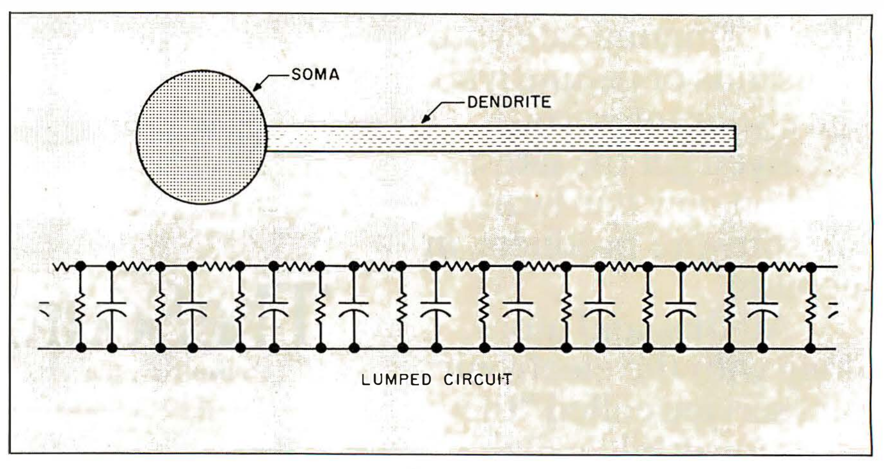


Figure 6: *The circuits shown in other figures may be cascaded to create whole cell models.*

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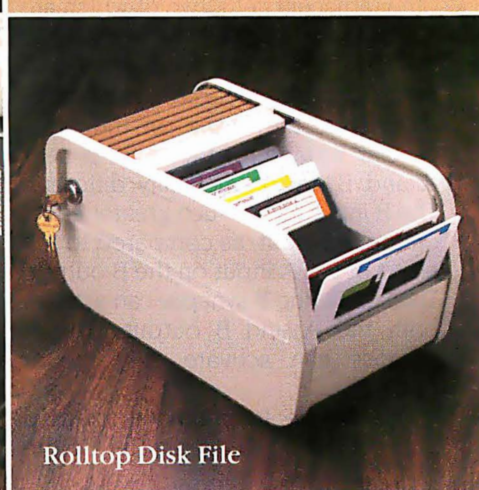
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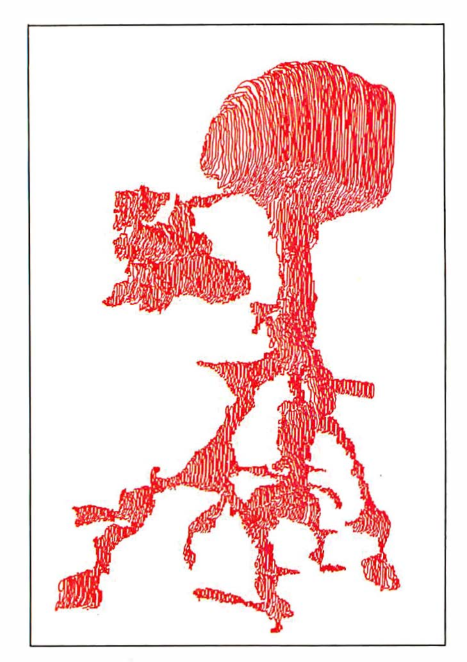


Figure 7: A *computer-reconstructed nerve cell from serial electron micrographs similar to those seen in photo 2. The soma diameter is about 10 microns. This amacrine cell from a retinal circuit was reconstructed by R. Jacobs, Playfair, using micrographs collected by B. McGuire.*

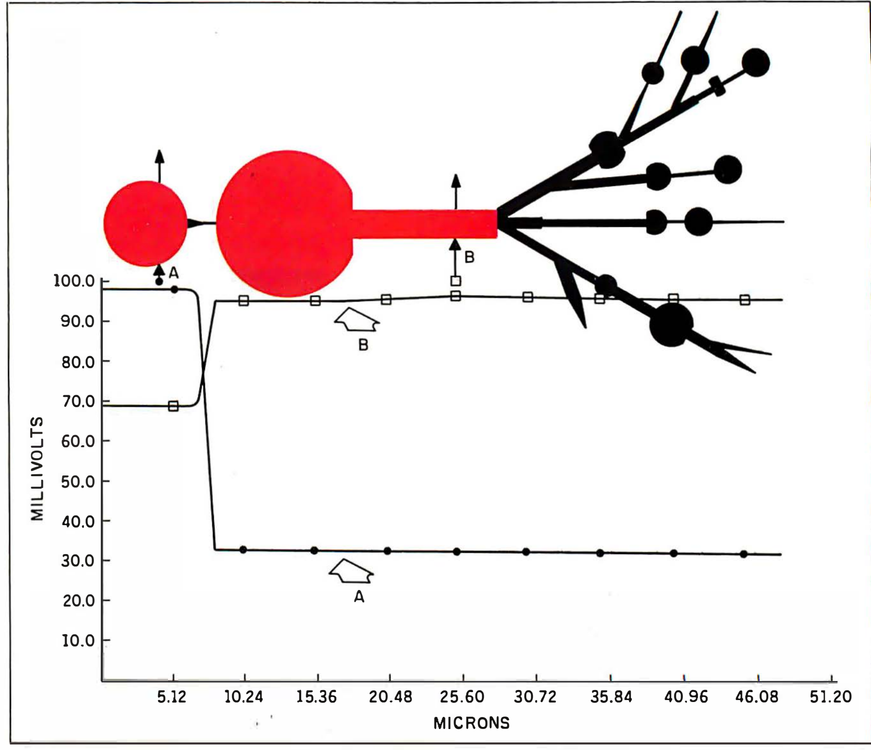


Figure 8: *Electrical model of the cell shown in figure 7. Some of the software used to compute these plots was developed by Dr. S. Ellias, Massachusetts General Hospital, Harvard Medical School.*

part of figure 8 shows the maximum peak of this response inside the cell on the graph. Each line represents the peak voltage along the dark portion of the cell during activation of the synapse.

Since this cell is an interneuron, it does not have an axon (amacrine means "without axon"), nor does it have an action potential. It does, however, have many synaptic outputs to other adjacent cells, two of which are illustrated by large arrows pointing up in figure 8. Keep in mind that the A and B synaptic inputs are identical. Yet the effects they have on the intracellular voltage for the outputs near A and B are dramatically different. The B input has a much greater effect on the A output, as compared to the effect of the A input on the B output. Thus, while the B synapse can activate both the A and B outputs, the A synapse can activate only the A output.

This simple function was created and controlled by geometry of the nerve cell itself. One can imagine other effects when both synapses are simultaneously activated or when other synaptic inputs are activated farther out on the dendrite. Thus, the specific analog-logical functions of a nerve cell can be controlled by the cell's geometry. This manipulation of cell form can be thought of as the device physics the brain uses to control logical functions.

Can We Adapt the Device Physics of the Brain to Silicon-Based Circuits?

The tantalizing question raised by these observations is "Can we adapt this simple principle of changing three-dimensional geometry to silicon-based circuits that could simulate brain circuits?" The answer is "Yes, quite easily." Jack Kilby of Texas Instruments, whose important insight led to the first IC 25 years ago, made us realize that it was possible to control many important silicon-based passive parameters such as the value of pull-up or pull-down resistors by changing the size and shape of the etched area. While the constants for resistances and capacitances are several orders of magnitude different from brain constants, it is interesting that the circuits in figures 3 and 6 are exact equivalents of those used to simulate an interconnection within a silicon chip. The equations and software used to simulate the nerve cell above are almost identical to the software used to simulate a full IC during design.

Projects to create these silicon-based neurons, called *silicrons*, are just now getting under way. Conceptually, the shape of the cell is simply etched into silicon in place of the conventional linear interconnections. Gates are placed at locations where synaptic inputs and outputs might be located, and for output silicrons we can simulate an axon with a simple Schmitt trigger circuit or one-shot.

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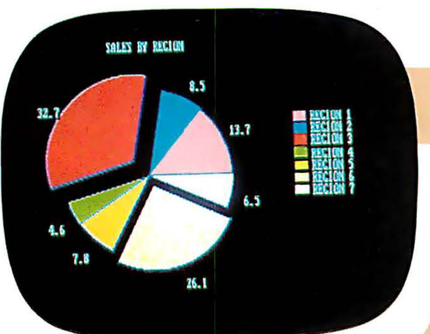
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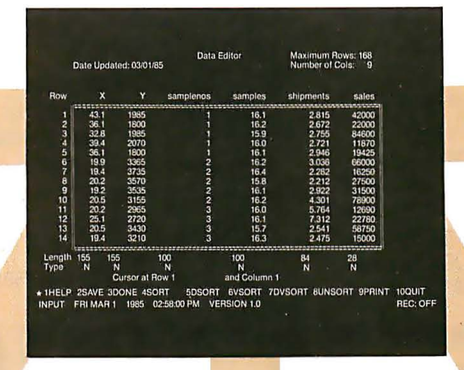
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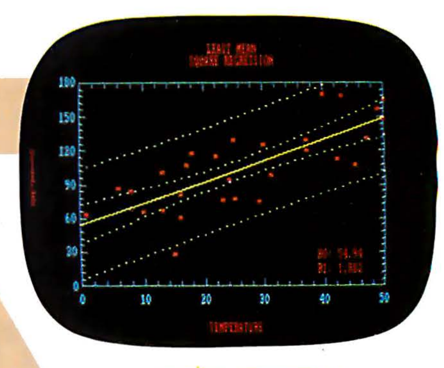


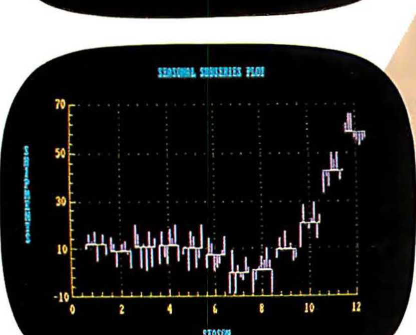
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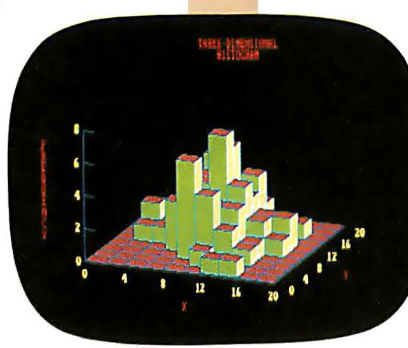
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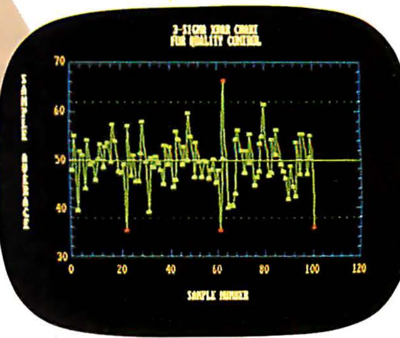












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a laboratory curiosity until one final problem has been resolved—how do we create new and arbitrary programs? There is no simple way to change or modify the strength of connections from one silicron to another. Since researchers do not really have a clear understanding of how the brain modifies its own circuits (the device physics of learning), any silicon-based solutions will be nonbiological. Ongoing biological work is encouraging and suggests that in some cells active shape change of dendrites may lead to changes in synaptic strength. Nevertheless, it is safe to say that it will be some time before we will have a full understanding of perhaps the most impressive feature of neural circuits: their ability to program themselves. In the meantime, it will certainly be possible to create very fast neuronlike devices with well-defined, prewired functions such as CCD (charge-coupled device) image processing. However, it will be quite some time before we can create what could legitimately be called a sixth-generation computer based on a neurological model. ■

The micrograph of brain cells grown in tissue culture by Judy Trogadis (see page 286) is available as a museum-quality poster for $7 (U.S.) plus $3 for postage and handling. Phone (713) 664-7457 or 526-9617 or write Synaptic Poster, 8 Alexander St., Brampton, Ontario L6V 1H6, Canada (VISA and MasterCard accepted). All proceeds from the sale of the poster will support the research described in this article. Copyright 1983, 1985, J. Trogadis and J. Stevens.

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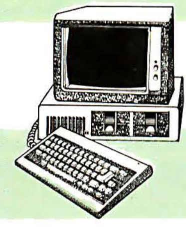
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THE TECHNOLOGY OF EXPERT SYSTEMS

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Transplanting expert knowledge to machines

THE PURPOSE OF this article is to introduce expert systems. Initially, we'll define these systems. Next, we'll discuss methods for building them, including the advantages and disadvantages of each method. Finally, we'll review the computer resources needed to build and run expert systems.

DEFINITION

Expert systems are a class of computer programs that can advise, analyze, categorize, communicate, consult, design, diagnose, explain, explore, forecast, form concepts, identify, interpret, justify, learn, manage, monitor, plan, present, retrieve, schedule, test, and tutor. They address problems normally thought to require human specialists for their solution. Some of these programs have achieved expert levels of performance on the problems for which they were designed (see reference 6).

Expert systems are usually developed with the help of human experts who solve specific problems and reveal their thought processes as they proceed. If this process of protocol analysis is successful, the computer program based on this analysis will be able to solve the narrowly defined problems as well as an expert. (For a discussion of successful expert systems, see reference 2.)

Experts typically solve problems that are unstructured and ill-defined, usually in a setting that involves diagnosis or planning. They cope with this lack of structure by employing heuristics, which are the rules of thumb that people use to solve problems when a lack of time or understanding prevents an analysis of all the parameters involved. Likewise, expert systems employ programmed heuristics to solve problems. Figure 1 is an example of a complex heuristic used by TAXADVISOR, an expert system that gives estate-planning advice (see reference 17).

Experts engage in several different problem-solving activities. For instance, the following problem-solving activities have been identified in MYCIN (see figure 2): identify the problem, process data, generate questions, collect information, establish hypothesis space, group and differentiate, pursue and test hypothesis, explore and refine, ask general questions, and make a decision (see reference 11).

Experts are capable of

- Applying their expertise to the solution of problems in an efficient manner. They are able to employ plausible inference and reasoning from incomplete or uncertain data.
- Explaining and justifying what they do.
- Communicating well with other ex-

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perts and acquiring new knowledge.
- Restructuring and reorganizing knowledge.
- Breaking rules. They have almost as many exceptions as they have rules. They understand both the spirit and the letter of a rule.
- Determining relevance. They know when a problem is outside their expertise and when to make referrals.
- Degrading gracefully. At the boundaries of their expertise, they become gradually less proficient at solving problems, rather than suddenly incapable (see reference 4).

Expert systems have modeled only the first three expert capabilities to any extent, and even explanation and knowledge acquisition have just begun.

Expert systems, like human experts, can have both deep and surface representations of knowledge. Deep representations are causal models, categories, abstractions, and analogies. In such cases, we try to represent an understanding of structure and function. Surface representations are often empirical associations but are sometimes "compiled" from an understanding of structure and function. In the former case, the association between premises and conclusions of rules is based on empirical observation of past association. Causality is implicit in the rule, rather than explicit.

Deep representations enhance the explanatory powers of expert systems. With surface representations, all the system knows is that an empirical association exists; it is unable to explain why, beyond repeating the association. Where more fundamental insight is available, deep representation will enable the system to respond more substantively. If computer induction is used for knowledge acquisition, a model for understanding events in the domain (a deep representation) often guides the induction of rules from examples by distinguishing meaningful hypotheses from coincidences in the data. It is also likely that deep representation will enhance the incorporation of the last four previously listed expert capabilities into expert systems. Surface representations have offered little in this regard.

However, surface representations have their advantages if the only concern is problem-solving performance, empirical associations, or compiled understanding. They should be less costly to formulate than causal models. This lower cost can provide a reasonable level of explanation along with a primitive form of knowledge acquisition. If a domain's expertise is based on empirical association, as in many areas of medicine, surface representations are the only kind available (see reference 4).

The best approach to expert-system building is probably to use deep representations when they are cost-effective and surface representations for the rest of the system. This approach has already been explicated in a paper by Hart (reference 12) and implemented in Digitalis Advisor, a system that provided advice on digitalis dosages for cardiac patients (see reference 29).

RULE 216
(This rule applies to clients and is tried to find out whether a short-term trust should be recommended.)

If:
1) The client and/or spouse do wish to shift property income to another (not for legal support), etc., for at least 10 years or until the death of the beneficiary,
2) The client and/or spouse do desire to eventually reclaim control of this property (for retirement, estate liquidity, etc.),
3) The client and/or spouse are in a higher income bracket than the beneficiary,
4) The client and/or spouse are willing to relinquish control of the beneficial enjoyment of the property,
5) The client and/or spouse are able to provide for their living needs without this income, even in the event of disability or unemployment,
6) The client and/or spouse do not plan to have the trust income used to pay life-insurance premiums on his/her life without the consent of an adverse party,
7) The client and/or spouse do not plan to use the trust for a leaseback of assets, and
8) A: The client and/or spouse have a person (e.g., a parent) they are supporting without legal obligation with this property income (will lose a dependent if trust is formed),
   B: The client and/or spouse have a child, not a minor, that they will be putting through college with this property income (can set up early and accumulate income without tax problems), or
   C: The client and/or spouse are using some of their after-tax income for the benefit of some other taxpayer (child's marriage and/or home purchase, etc.),

Then: It is definite (1.0) that client should TRANSFER ASSETS TO A SHORT-TERM TRUST.

Figure 1: *An example of a* TAXADVISOR *rule.*

BUILDING EXPERT SYSTEMS

An expert system is able to make decisions on a par with an expert primarily because its structure reflects the manner in which human specialists arrange and make inferences from their knowledge of the subject. The system is driven by a database of inexact and judgmental knowledge that is typically made up of if-then rules when surface representation is used, or frames and semantic nets when deep representation is used (see "A Glossary of Artificial Intelligence Terms" on page 138). Domain knowledge is processed in a strict order of deductive inference and is invoked by a pattern match with specified features of the task environment. Figure 3 is an example of pattern matching by TAXADVISOR. Because uncertainty is usually involved in expert judgments, expert systems must allow

conclusions to be reached with less than certainty. Figure 4 illustrates how TAXADVISOR copes with uncertainty during a consultation. (For more information on uncertainty mechanisms in expert systems, see reference 32.)

The type of computer program that is used to develop an expert system cannot have its flow of control and data utilization rigidly fixed because such a structure is ill-adapted for simulating a human's responses to a complex, rapidly changing, and unfamiliar environment. Instead, such a program must examine the state of the world at each step of the decision process and react appropriately because new stimuli continually arise. The type of program that has been developed to cope with this constant change is a loosely organized collection of pattern-directed modules (PDMs) that detect situations and respond to them (see reference 31). The rule in figure 1 is a PDM from TAXADVISOR.

Each PDM examines and modifies data structures that model critical aspects of the external environment. In TAXADVISOR, the client's financial-planning situation and objectives constitute the environment. A PDM should be written as a single and separate unit that is independently meaningful within the task domain of the program. This aids incremental program growth and debugging, since revision of one PDM does not affect the others. It also provides explanation power; a single PDM can be used to explain a recommendation by the system.

Any system composed of several PDMs, one or more data structures that may be examined and modified by the PDMs, and an executive program to schedule and run the PDMs is called a pattern-directed inference system (PDIS). In effect, a PDIS factors complex problems into manageable, largely independent subproblems.

Surface Representations

Rule-based systems (RBSs) were originally used in cognitive modeling of short-term memory. Since expert

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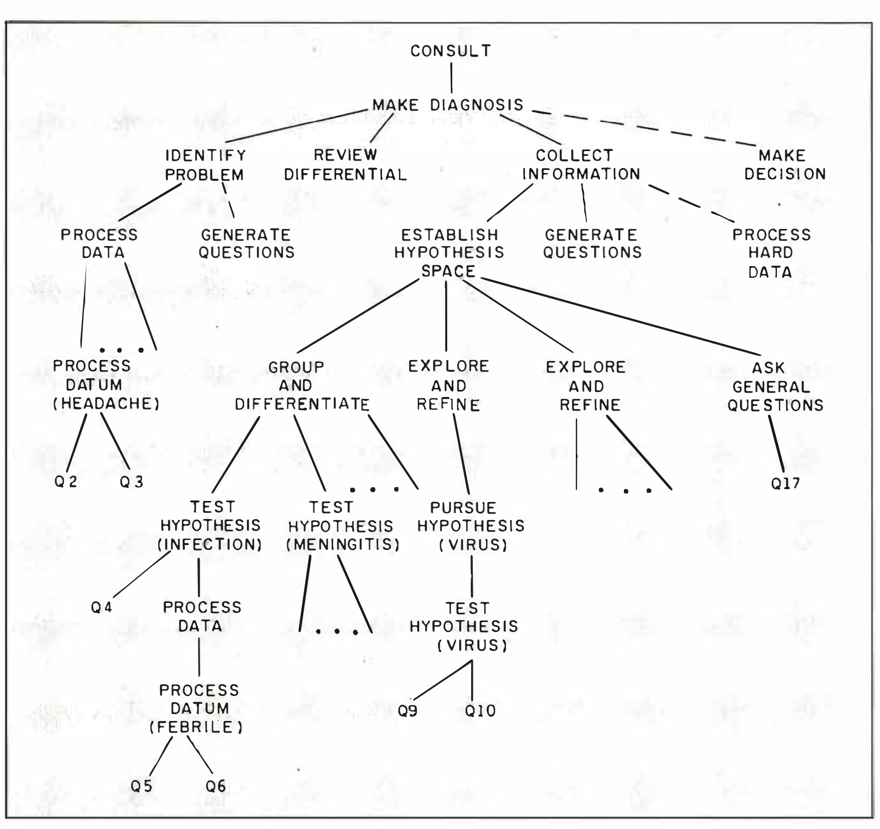


Figure 2: *The* MYCIN *problem-solving hierarchy. Question numbers* (Q2, *etc.*) *correspond to questions asked in the consultation. Solid lines show tasks actually done, dashed lines those that might be done.* (*Figure used with permission; see reference* 11.)

Necessary Attributes for Short-Term Trust	Prestored Value	Client's Value
1) Does client wish to shift property income to another (not for legal support) for at least 10 years or until the death of the beneficiary?	yes	yes
2) Does client desire to eventually reclaim control of the property?	yes	yes
3) Is client in a higher income-tax bracket than the beneficiary?	yes	yes
4) Is client willing to relinquish control of the beneficial enjoyment of the property?	yes	yes
5) Is client able to provide for his living needs without this income even if disabled or unemployed?	yes	yes
6) Does client plan to have trust income pay life-insurance premiums on his life without consent of an adverse party?	no	no
7) Does client plan to use the trust for a leaseback of assets?	no	no
8) Does client have a person he is supporting without legal obligation?	yes	yes

Figure 3: *An example of pattern matching done by* TAXADVISOR, *performed to determine if the client should be forming a short-term trust. The Prestored Value column shows the pattern of attribute values that a client must have before* TAXADVISOR *will recommend a transfer of assets to a short-term trust. Since the client's pattern matches the prestored one, the trust will be recommended.*

(begin)

—Formation of a Temporary Trust—

1) Does client wish to shift property income to another (not for legal support) for at least 10 years or until the death of the beneficiary?
**YES
2) Does client desire to eventually reclaim control of the property?
**YES
3) Is client in a higher income-tax bracket than the beneficiary?
**YES
4) Is client willing to relinquish control of the beneficial enjoyment of the property?
**WHY

This will aid in determining whether client should form a temporary trust. It has already been established that

1) Client wishes to shift property income to another (not for legal support) for at least 10 years or until the death of the beneficiary,
2) desires to eventually reclaim control of the property, and
3) is in a higher income-tax bracket than the beneficiary.

Therefore, if

1) client is willing to relinquish control of the beneficial enjoyment of the property,
2) is able to provide for his living needs without this income, even if disabled or unemployed,
3) does not plan to have trust income pay life-insurance premiums on his life without the consent of an adverse party,
4) does not plan to use the trust for a leaseback of assets, and
5) A: has a person (e.g., a parent) he is supporting without legal obligation with this property income,
B: has a child, not a minor, that he will be putting through college with this property income, or
C: is using some of his after-tax income for the benefit of some other taxpayer,

then

client should form a temporary trust
(back to question 4 . . .)

**YES

5) Is client able to provide for his living needs without this income, even if disabled or unemployed?
**YES (8) [Whenever a response is made with less than certainty, the system user enters a number betwen 1 and 9 indicating his degree of certainty in that response.]
6) Does client plan to have trust income pay life-insurance premiums on his life without consent of an adverse party?
**NO
7) Does client plan to use the trust for a leaseback of assets?
**NO
8) Does client have a person he is supporting without legal obligation?
**YES
I recommend that the client form a short-term trust.
[The degree of certainty that the system has in this recommendation is .8. This certainty factor (CF) was calculated as follows. The temporary trust rule's action CF was 1.0 and it had an "AND" premise. In such a case, the rule's CF is the minimum CF used in the responses, or .8. Since the system's threshold CF is .2, the recommendation was made.]

(end)

Figure 4: *A partial interactive consultation with* TAXADVISOR. *The user's input is in uppercase.*

systems attempt to imitate people, it was natural that RBSs would also be used in their development. To date, RBSs are by far the most common structure for expert systems. Among the successful rule-based expert systems that have been developed are the following:

- MYCIN—diagnoses infections (reference 26)
- HEURISTIC DENDRAL—identifies organic compounds (reference 8)
- PROSPECTOR—aids geologists in evaluating mineral sites (reference 5)
- PUFF—analyzes pulmonary function tests (reference 15)
- INTERNIST—performs diagnosis in internal medicine (reference 22)
- XCON (formerly R1)—configures the VAX-11/780 computer system (reference 16)
- SACON—provides engineers with advice on structural analysis (reference 1)

Because of the popularity of RBSs, several domain-independent systems have been developed to make it much easier to build rule-based expert systems in many fields. The following is a partial list of domain-independent systems:

- EMYCIN (reference 30)
- AGE (reference 21)
- OPS5 (reference 16)
- ADVISE (reference 18)
- Hearsay-3 (reference 7)
- AL/X (reference 23)
- Expert-Ease (Human Edge Software Corp., Palo Alto, California)
- KS 300 (Revamped EMYCIN; from Teknowledge Inc., Palo Alto, California)
- KES (Intelligenetics Inc., Palo Alto, California)
- Personal Consultant (Texas Instruments Inc., Dallas, Texas)

An RBS is composed of PDMs called rules, each with a left-hand side (the antecedent, a logical combination of propositions about the database) and a separate right-hand side (the consequent, a collection of actions). An RBS separates data examination (done by the left-hand side) from data modification (done by the

right-hand side of the rule).

Most RBSs are production systems (PSs), in which matching and scheduling are explicitly defined by the operation of the executive (control) program. The control schema can be characterized as having four basic parts:

1. Selection: select relevant rules and data elements. Selection may be trivial (e.g., on each cycle all rules and all data elements can be considered) or quite complex (e.g., special filters can be designed to eliminate from consideration many rules that could not possibly match the current data). In TAXADVISOR, rules are organized in a hierarchy to narrow the rules considered.
2. Matching: compare active rules against active data elements, looking for patterns that match, i.e., rules whose conditions are satisfied. Figure 3 is an example of pattern matching.
3. Scheduling: decide which "satisfied" rule should be "fired." "Firing" consists of accessing and executing the procedures associated with the pattern elements that matched the current data. If more than one rule is satisfied, conflict-resolution heuristics are used to decide which rule to fire.
4. Execution: fire the rule chosen during the scheduling process. The result of execution is a modification of data elements or structure. With TAXADVISOR, execution results in an estate-planning recommendation for a client. This is illustrated in the test consultation in Figure 4 (see reference 31).

PSs are either consequent-driven systems or antecedent-driven systems. A consequent-driven (backward-chaining) system, which is the type used in TAXADVISOR, uses rule consequents (which represent goals) to guide the search for rules to fire (with TAXADVISOR, estate-planning actions to recommend). The system collects those rules that can satisfy the goal in question and tries to satisfy the consequents of those rules, which usually represent the values of variables. In order to find these values, the values of the rule antecedent must be found. To satisfy each antecedent, which represents a subgoal, the system collects those rules whose consequents satisfy its value. The process of working backward through the rules from consequents to antecedents to consequents in search of a causal chain that will satisfy the goal is called backward chaining. (For a simple backward-chaining program written in BASIC, see "Knowledge-Based Expert Systems Come of Age" by Richard O. Duda and John G. Gaschnig, September 1981 BYTE, page 238.)

With antecedent-driven (forward-chaining) systems, program execution consists solely of a continuous sequence of cycles terminating when a rule's action dictates a halt. At each cycle, the system scans the antecedents and determines all rules with antecedents that are satisfied by the contents of the database. If there is more than one such rule, select one by means of a conflict-resolution strategy. Perform all actions associated with the selected rule and change the database accordingly. For example, with R1 (XCON), you enter all the information on the problem into the database, and the system then applies the rules to reason forward from the data to the conclusions. In summary, forward chaining consists of putting the rules in a queue and then using a recognize-act cycle on them.

Some forward-chaining systems try to control the search for rules in the recognize cycle by grouping rules into packets. These rule groupings are appealing conceptual structures, since they group rules according to the subtopic that they deal with. Object-oriented programming can also be used to organize collections of rules. In object-oriented programming, we give objects behavior, and thus we can distribute the control of rules into rule, rule-packet, and domain objects. This approach, which has been taken in LOOPS, a domain-independent system (see reference 27), also allows multiple instantiations of the same set of rules to solve subproblems of the

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same type within one session.

The primary difference between backward and forward chaining is a top-down versus bottom-up style of linking rules together. Though the most common, these are not the only control structures for rule-based systems. For example, rules are represented as an "inference" network in PROSPECTOR (see reference 5).

Deep Representations

Frame- and network-based approaches allow the implementation of "deeper-level" reasoning such as abstraction and analogy. Reasoning by abstraction and analogy is an important expert activity. You can also represent the *objects* (e.g., "pump" in figure 5) and *processes* (e.g., the "start" instructions in figure 5) of the domain of expertise at this level. What is important are the *relations between objects*. Deep-representation expert systems perform inference using relations represented by networks or frames. A semantic network is a graph of the relations. A frame or script system (see references 20 and 24) organize the objects and their relations into *entities* (recognizable collections of objects). Frame systems also provide a system to inherit attributes from a taxonomy of entities. Thus, a frame system implements the semantics of some of the relations between objects. With a semantic-net or frame system you can represent objects of the domain of expertise as well as the process, strategies, etc., that are also part of the domain. The control of frame or semantic-net systems is usually much more involved than with surface systems and is implemented in a way that an explanation facility can't get at. But surface systems are "shallow"; a surface system may be viewed as a projection of deep-level knowledge of a domain for a specific

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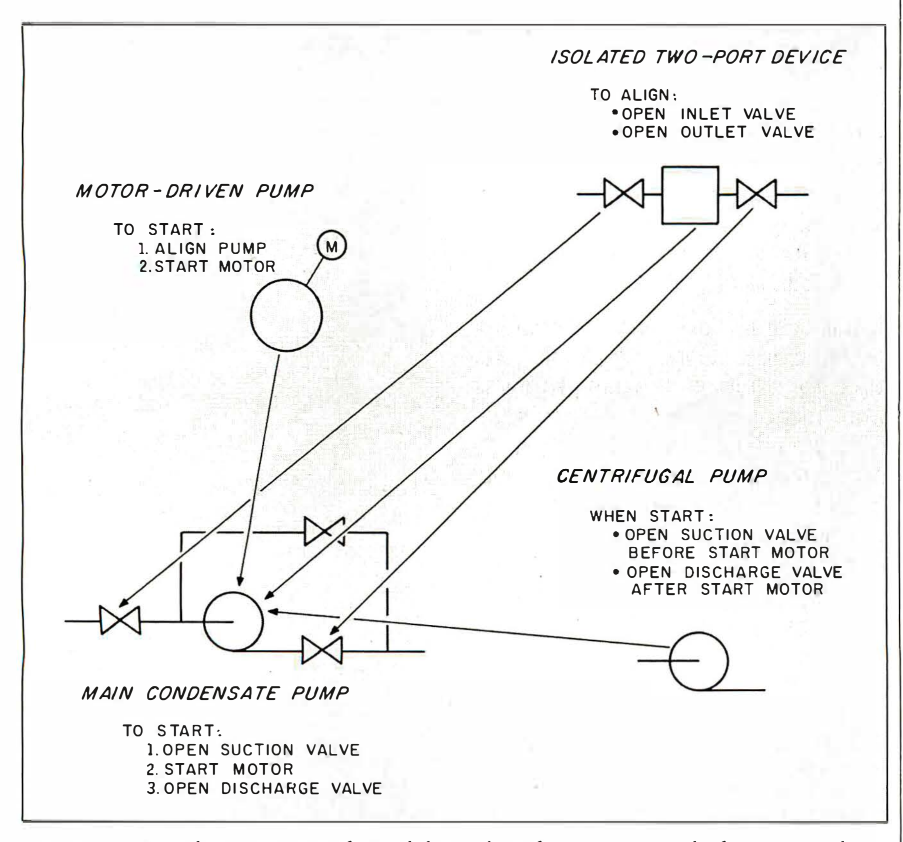


Figure 5: *Procedure steps are obtained from the subcomponents and abstractions of an object, here a main condensate pump. This example comes from Steamer, a tutorial system designed to teach operating procedures of shipboard steam plants.*

Some systems have a built-in capability for taking a file of expert decisions and generalizing from this knowledge an executable rule.

expert activity.

One type of expertise that has been represented with a deep-level approach is tutoring (see "The LISP Tutor" by John R. Anderson and Brian J. Reiser on page 159). Here we want to convey to the pupil domain knowledge that is best represented at the deep level: concepts, abstractions, analogies, and problem-solving strategies.

Steamer is a training aid developed jointly by Bolt Beranek and Newman Inc. and the Navy Personnel Research and Development Center. Its goal is to teach operating procedures of shipboard steam plants. These procedures consist of a series of steps on subcomponents of the plant. The components and procedures are represented as frames in Steamer, as are the abstractions of components and procedures that experts use in teaching steam-plant operations. The steps of a procedure come from the abstractions and subcomponents of the device the procedure applies to. The ordering of the steps comes from a third represented entity: operating principles. These principles are culled from experienced operators and represent "compiled" knowledge of steam-plant operation (although they are not represented as rules but frames).

Knowledge Acquisition

The following are ways of acquiring knowledge in a form that can be used by an expert system (reference 19):

- being told
- analogy
- example
- observation, discovery, and experimentation
- reasoning from deep structure

The manual acquisition of knowledge from human experts is a very labor-intensive process. There is an acknowledged need to have aids for knowledge acquisition as part of the system.

Methods to speed knowledge acquisition are now becoming available in the form of machine learning of rules from examples. Systems such as Expert-Ease have a built-in capability for taking a file of expert decisions from you and generalizing from these an *executable rule*. In a sense, you are able to transplant chunks of decision-making skill from your own brain to the personal computer, a possibility foreseen as early as 1966 by Earl Hunt and his colleagues.

The machine procedure that allows this skill transplant was developed from a Pascal-coded program called ID3 (Iterative Dichotomiser 3) due to Professor Ross Quinlan of the New South Wales Institute of Science and Technology.

A number of conclusions follow from Quinlan's work:

1. It is possible, using such a program, to generate machine-executable solutions for complex decision problems in a fraction of the time a programmer would need for developing a solution by conventional hand coding.
2. The resulting solutions are super-efficient as compared with those obtainable by the old hand methods.
3. It is important to make up your mind in advance whether super-efficiency is all you demand of a machine-executable solution, or whether you *also* want the resulting rule base to be understandable on inspection.

If the answer to the third statement above is that user transparency of induced rules is desired, then (unless it is a very small one) do *not* treat your problem as one big superproblem with a single associated file of examples. Instead, first break it down into a main problem and a set of subproblems, even going further (to the level of sub-subproblems) if the complexity of the problem domain seems to call for it. The originators of this style, which is known as "structured induction," are Drs. Shapiro and Niblett (reference 25). Corporations enjoying the use of powerful inductive generators such as ITL's FORTRAN-based EX-TRAN system or Radian Corporation's C-coded RuleMaster have applied the approach to the building of complex systems for trouble-shooting large transformers, severe-storm warning, circuit-board fault diagnosis, and user-friendly guidance to set up numerical batch jobs in seismic analysis in the oil industry. Rates of production of compact installed code in excess of 100 lines per worker day are now commonly reported.

Any robust expert system takes a tremendous amount of resources to develop. Once developed, the knowledge along with the control structure can be "compiled out"; that is, the system of rules is rewritten into a piece of code that performs the same function on a personal computer. For example, some expert systems (ADVISE, EMYCIN, OPS5—see reference 10) can generate code or other primitive forms of the knowledge for use on a personal computer. (Systems run on a personal computer are usually referred to as "delivery systems.")

Knowledge Representation

As AI researchers point out, a robust expert system that can explain, justify, acquire new knowledge, adapt, break rules, determine relevance, and degrade gracefully will have to use a multitude of knowledge representations that lie in a space whose dimensions include deep/surface, qualitative/quantitative, approximate (uncertain)/exact (certain), specific/general, and descriptive/prescriptive. Systems that use knowledge represented in different forms have been termed *multilevel systems*. Steamer is an example of one such expert system.

Steamer uses the following representations:

1. A graphical (icon) representation of the objects of the Steamer domain, such as valves, pumps, tanks, and systems composed of these.
2. A frame representation of Steamer objects, procedures, and operating principles. This is used for describing, explaining, categorizing, abstracting, and referring.
3. An assertional database where assertions about Steamer entities can be made and retracted.
4. A quantitative numerical simulation of the steam plant that is used in illustrating cause and effect and ramifications of the application (or misapplication) of procedures.

Work is just beginning in building such multilevel systems, and they will be a major research topic for this decade. Work needs to be done in studying and representing in a general way the different problem-solving activities an expert does (see reference 3). When you build expert systems, you realize that the power behind them is that they provide a regimen for experts to crystallize and codify their knowledge, and in the knowledge lies the power.

RESOURCES NEEDED

Before resource needs are discussed, you must precisely define the type of expert system you want to build. If you wish to build a large, "custom" model expert system (i.e., it is not feasible to use many of the smaller domain-independent systems that are available), you will need substantial resources: large memory, good language support, and fast execution of the code. You may need to develop such a system in LISP on hardware specialized to processing the language, or on time-sharing machines with a large address space. Such "custom" systems are usually referred to as "prototype" or "development" systems. They can either be developed for a specific domain (e.g., MYCIN) or be domain-independent (e.g., ADVISE).

If you are able to build a less complex expert system using an existing domain-independent system or if the system has a rule-compilation facility that allows applications to be run on personal computers, then a personal computer (preferably with 512K bytes) is sufficient. If all you need are resources to run an existing expert system, a large personal computer should nearly always be sufficient.

There is no obvious line of demarcation for a given project. However, certain barriers make personal computer use less desirable as system size and complexity increase.

SYSTEM BARRIERS

Many high-level languages do not offer the right primitives (i.e., programming-language statements) for developing expert systems. Among the desirable primitives are

- A parser or interpreter that parses statements during program run time. Without this, you have to write a parser for the rules.
- List and nonnumeric processing primitives.
- A language design that allows incremental compilation and other fast prototyping facilities. Incremental compilation enables you to recompile a function or other portion of a file without recompiling the entire file.

The view that many people in the field are adopting is that high-level languages like Pascal, Ada, and C are acceptable for the delivery system, but for prototyping, a language like LISP or Prolog is preferred. Program-generation tools are then used to write the system in the delivery language.

The knowledge-intensive approach to expert systems implies that the memory will be highly utilized in all but the most nontrivial applications. AL/X is one example that ran on a 64K-byte machine, but it was a small expert-system shell. Since memory prices have gone down and many small machines have broken the 64K-byte barrier, we can expect that more expert systems can be developed, at least for the delivery system, on per-

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Some researchers predict that memory needs of advanced expert systems will drive development of encyclopedic memories.

sonal computers. Some researchers predict that the memory needs of advanced expert systems will drive the development of encyclopedic memories for personal computers.

CONCLUSION

Expert systems can be built in many ways, involving rules, networks, frames, and combinations thereof, with all sorts of variations within these categories with respect to knowledge representation and control. We could not begin to cover all possible approaches to building expert systems, since new ones are being developed almost daily.

Even if the most efficient approach has been ascertained for the domain in question, the most cost-effective computer resource must still be determined. In most cases, approach selection at least narrows the choice for resources; in some cases, approach and resources can be selected together. However, this hardly reduces the complexity of the choice. To make matters worse, computer resources are changing as rapidly as the new system-building approaches are being developed. The best we can hope to convey is an awareness of the opportunities and complexities involved in the development of expert systems. ■

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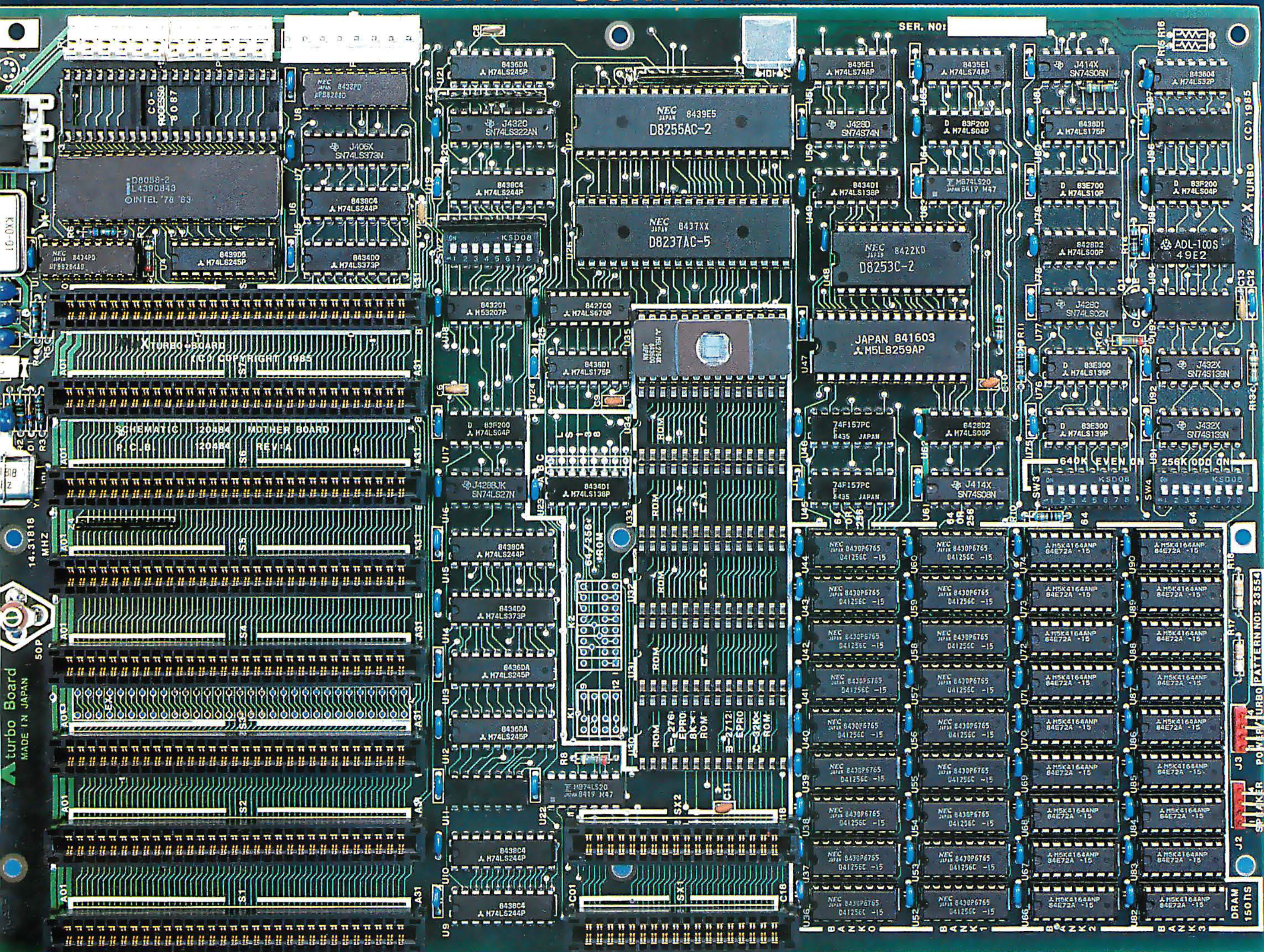
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INSIDE AN EXPERT SYSTEM

BY BEVERLY A. THOMPSON AND WILLIAM A. THOMPSON

From index cards to Pascal program

AN EXPERT SYSTEM will allow anyone with some expertise to create an outline of the process used to solve a particular problem. This outline can be used to generate a series of questions that lead a nonexpert through the solution of similar problems. Many different techniques are used to represent an outline of expert knowledge. One method currently employed is the use of IF. . .THEN sentences, called rules, to make factual statements about the problem area.

In this article we will describe one way that an expert system can use a set of rules to conduct a consultation session. We will describe the mechanics of how an expert system operates by creating a "cardboard inference engine," and we'll then examine some of the programming considerations for translating the cardboard system into Pascal.

Before we begin describing how rules are used in an expert system, we should get a clearer idea of where the rules come from and the structure that they represent. Imagine for a moment that you are an expert in the field of botany, and you have just received a phone call from a woman who wants your help in identifying the botanical family of a plant that she has found. Since you can't see the specimen, you must rely on information supplied by the caller. However, since she is not an expert, it is very difficult for her to know what information will help you to make the identification. You will have to ask questions in order to get the caller to supply the facts you need to solve the problem.

Let's assume that you have asked enough questions to determine that the plant in question is a tree that belongs to the botanical class gymnosperm. Figure 1 shows one possible decision procedure that can complete the possibilities in this case. In table 1, rules 1 through 4, you can see how the diagram shown in figure 1 is represented as rules using IF. . .THEN statements. The set of rules in table 1 and the information in table 2 comprise an incomplete botanical knowledge base that we will use to answer questions about plant type (herb, vine, shrub, or tree), class of tree (angiosperm or gymnosperm), and family of gymnosperm (cypress, bald cypress, or pine). Because we are using an incomplete knowledge base, we can ask well-formed questions that the system cannot answer (e.g., family membership of a vine). Nonetheless, we believe that our simple example will give you some insight into what an expert system is and how it works.

THE KNOWLEDGE BASE

It is important to understand that knowledge is not a random collection of facts but a collection of facts related by some overall structure. In the example above, the IF. . .THEN rules provide that structure. The collection of facts used to capture all of the information in a problem area is called the knowledge base. In the system we will present, the knowledge base consists of three main elements—rules, prompts, and translations.

Each rule in table 1 is made up of a conditional part, which is preceded by the word "IF," and a conclusion part,

(continued)

Beverly and William Thompson (RD 2, Box 430, Nassau, NY 12123) are the founders of MicroExpert Systems, a company specializing in artificial-intelligence tools for microcomputers. In addition to writing the MicroExpert System program, they are writing a book on expert systems that will be available soon.

which is preceded by the word "THEN." Each clause within these parts is made up of an attribute, which is a keyword or phrase that is some quality about which we are seeking information; a value, which is assigned to an attribute either as a response to a question or a conclusion to a rule; and a predicate (the word "IS" in our system), which relates the two.

Since one of the tasks of the system is to ask the caller to supply information about some of the attributes, the questions to be asked (the prompts) will have to be stored in the knowledge base. The attributes TYPE, FAMILY, and CLASS do not have questions associated with them because the user is never expected to supply any information about them.

Another item associated with the attribute is the translation. This is used to expand the keyword to make the rules more readable. There are two different ways to form translations. The following example illustrates the first of these:

Attribute: STEM
Translation: The stem of the plant
Attribute: TYPE
Translation: The type of the plant
Rule without translation: IF STEM IS GREEN THEN TYPE IS HERB.
Rule with translation: If the stem of the plant is green, then the type of the plant is herb.

When forming a translation of this type, you must keep in mind that whatever phrase is chosen will be directly substituted for the attribute. The predicate and value will remain exactly as they appear in the untranslated rule.

If the method above is used when the value of an attribute is YES or NO, the resulting phrase is very unnatural. We can get around this problem as follows:

Attribute: BROAD AND FLAT
Translation: The shape of the leaves is /not/ broad and flat
Rule without translation: IF TYPE IS TREE AND BROAD AND FLAT IS YES THEN CLASS IS ANGIOSPERM.
Rule with translation: If the type of plant is tree and the shape of the leaves is broad and flat, then the class of the tree is angiosperm.

If the value had been NO, the clause would have read "the shape of the leaves is not broad and flat." Since the predicate and value are already contained in the translation, they are not restated after the translation.

The Cardboard Inference Engine

Now that we have described all of the items in the knowledge base, we are ready to construct our cardboard inference engine. To make it easy to manipulate the individual items in the knowledge base, let's think of each rule as being placed on a separate index card. Since both prompts and translations are associated with the individual attributes, we can also make an index card for each attribute that lists the keyword, the translation, and the prompt, if there is one. The rules in our knowledge base are shown in table 1; the complete set of attribute cards is shown in table 2. At this point it may be helpful to actually make this set of cards. The step numbers listed in the description that follows refer to the sample session shown in table 3.

The Goal Stack

With our knowledge base completed we can use our cards to guide us through a consultation. The first step in any consultation is to choose a goal for the session (step 1). In this example we will make FAMILY the final goal of our consultation. To begin we should set aside the attribute card for FAMILY on a separate pile called the goal stack. The attribute that appears on the top of the goal stack is called the current goal.

The Context Stack

As we proceed in the consultation, we must keep track of all the facts that we discover. When an attribute is as-

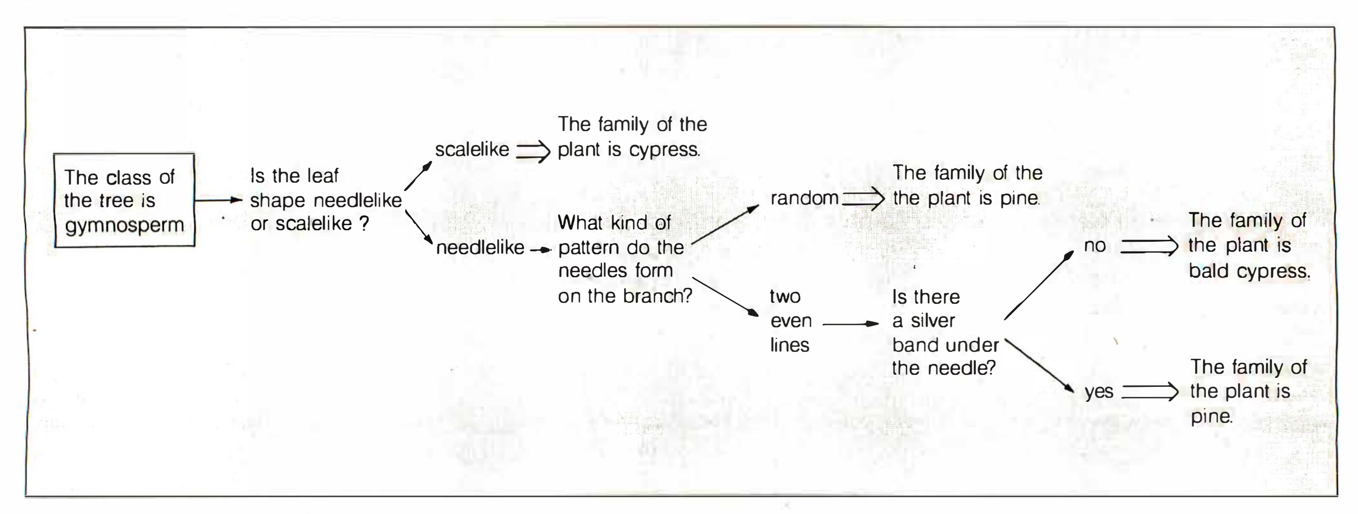


Figure 1: *A flow diagram for determining the family of a gymnosperm tree.*

Table 1: *The rules for the sample botany expert system.*

1	IF	CLASS IS GYMNOSPERM
	AND	LEAF SHAPE IS SCALELIKE
	THEN	FAMILY IS CYPRESS .
2	IF	CLASS IS GYMNOSPERM
	AND	LEAF SHAPE IS NEEDLELIKE
	AND	PATTERN IS RANDOM
	THEN	FAMILY IS PINE .
3	IF	CLASS IS GYMNOSPERM
	AND	LEAF SHAPE IS NEEDLELIKE
	AND	PATTERN IS 2 EVEN LINES
	AND	SILVERY BAND IS YES
	THEN	FAMILY IS PINE .
4	IF	CLASS IS GYMNOSPERM
	AND	LEAF SHAPE IS NEEDLELIKE
	AND	PATTERN IS 2 EVEN LINES
	AND	SILVERY BAND IS NO
	THEN	FAMILY IS BALD CYPRESS .
5	IF	TYPE IS TREE
	AND	BROAD AND FLAT IS YES
	THEN	CLASS IS ANGIOSPERM .
6	IF	TYPE IS TREE
	AND	BROAD AND FLAT IS NO
	THEN	CLASS IS GYMNOSPERM .
7	IF	STEM IS GREEN
	THEN	TYPE IS HERB .
8	IF	STEM IS WOODY
	AND	POSITION IS CREEPING
	THEN	TYPE IS VINE .
9	IF	STEM IS WOODY
	AND	POSITION IS UPRIGHT
	AND	ONE MAIN TRUNK IS YES
	THEN	TYPE IS TREE .
10	IF	STEM IS WOODY
	AND	POSITION IS UPRIGHT
	AND	ONE MAIN TRUNK IS NO
	THEN	TYPE IS SHRUB .

Table 2: *The set of attribute cards for the botany expert system. The attributes are in capital letters, followed by their translations and the appropriate prompt.*

CARD 1	STEM
	the stem of the plant
	Is the stem of the plant woody or green?
CARD 2	POSITION
	the position of the stem
	Is the position of the stem upright or creeping ?
CARD 3	ONE MAIN TRUNK
	the plant does /not/ have one main trunk.
	Does the plant have one main trunk ?
CARD 4	TYPE OF PLANT
	The type of plant
CARD 5	BROAD AND FLAT
	the shape of the leaves is /not/ broad and flat
	Is the shape of the leaves broad and flat ?
CARD 6	CLASS
	The class of the tree
CARD 7	LEAF SHAPE
	the leaf shape
	Is the leaf shape needlelike or scalelike ?
CARD 8	NEEDLE PATTERN
	the pattern the needles form along the branch
	Is the pattern that the needles form along the branch a random one or are the needles in 2 even lines ?
CARD 9	SILVER BANDS
	there is /not/ a silver band under each needle
	Is there a silver band under each needle ?
CARD 10	FAMILY
	the family of the plant

signed a value we will take its attribute card and place it on a pile called the context stack. Since we must also save the value that is assigned to the attribute, a card containing the value of the attribute must be placed along with the attribute card. We will also need a discard pile for rules that we want to remove from the knowledge base. We are now ready to see how these pieces can be put together to form an inference engine. An inference engine is a method of systematically choosing goals, evaluating rules, and interacting with the user in order to obtain a value for the final goal.

Choosing a Rule to Evaluate

First try to find a rule card that gives some information about the current goal attribute in its conclusion part (the statements following the word "THEN" in the rule). This process of searching through the conclusions of rules to solve goals is referred to as backward chaining (also called goal-driven inference or consequent reasoning). If you find a rule that contains the attributes of the current goal in its conclusion, you can go on to "Evaluating the Rule"; otherwise, you will have to resort to the procedure described in the section "Asking the Caller for Information."

Evaluating the Rule

Once we have chosen a rule to evaluate, we must compare the statements in the condition part of the rule, one by one, with the facts that are already known. These facts are contained on the context stack. As we make this comparison we will discover that one of three possibilities can occur:

1. *Evaluating an unknown rule*: The value of a rule is unknown when one or more condition clauses in the current rule do not appear on the context stack (as with rule 1 in step

(continued)

2 of our example shown in table 3). Before this rule can be successfully evaluated the unknown information must be discovered, so the attribute card listing the first unknown attribute (CLASS in our example) will be placed on the goal list along with the rule card containing the unknown rule. The goals that go on the goal list after the final goal are sometimes referred to as subgoals. Return to "Choosing a Rule to Evaluate" and try to find a rule with CLASS in its conclusion.

2. *Evaluating a false rule*: A rule is false when one of the statements on the card has a clause that is contradicted by a fact on the context stack (in step 6, rule 7 has the value GREEN for the attribute STEM, which was contradicted by the user input). In this case, the current rule card is placed on the discard pile, and you must return to "Choosing a Rule to Evaluate."

3. *Evaluating true rules*: A rule is said to be true when each of the clauses in the condition part of the rule matches an item on the context stack (rule 9 was established as true in step 12). When all of the clauses in the condition part are true, the statements in the conclusion part must also be true. Since this rule was chosen to be evaluated because it contained the current goal as its conclusion, you should remove the current goal from the top of the goal stack and place it on the context list. The rule card left behind on the goal stack (rule 5 in our example) should be returned to the top of the rule card pile so it can be reevaluated. The rule card we have just evaluated (rule 9) is kept with the attribute card on the context list to show the value of the attribute and how it was reached. This rule card will also be used to answer questions that the caller may later ask about this conclusion. If there are no other goals on the goal stack, the problem has been solved. If there are goals remaining, return to "Choosing a Rule to Evaluate."

Asking the Caller for Information

In the event that no rule can be found that can provide information about the current goal, you must turn to the caller to help provide the necessary information (in step 5, we ask the caller for information because none of the rules have STEM in their conclusion). This is where we make use of the prompts that have been placed on the attribute cards. Unfortunately, if no prompt appears on the card, it means that the caller can provide no information about the attribute in question. In this case, we have reached a dead end and will have to end the consultation without finding a solution to the problem. If this occurs, there is either some problem with our rules or this branch of the knowledge base was left unresolved.

When a prompt does appear on the current goal card, we use it to question the caller. Once the caller has supplied the missing information, we can remove the current goal card from the goal stack and place it on the context stack. If there is a rule card with this goal, it should be placed on the top of the pile of rule cards. You will also have to make a card that lists the value and place it on the context stack with the attribute card. Once this has been done we can return to "Choosing a Rule to Evaluate."

Why and How

In the course of a consultation it is not uncommon for the caller to want to know why you are asking a certain question. In table 3, step 13, we were unable to find a rule that gave any information about BROAD AND FLAT, so

(continued)

Table 3: A *step-by-step illustration of a cardboard-inference-engine consultation, showing stack volatilities.*

step	evaluate rule#	value of rule	response to prompt	goal stack attribute	goal stack rule#	context stack attribute	context stack value	context stack rule#	discard rule#
1				FAMILY					
2	1	unknown		CLASS	1				
3	5	unknown		TYPE	5				
4	7	unknown		STEM	7				
5	no		WOODY	TYPE	5	STEM	WOODY		
6	7	false							7
7	8	unknown		POSITION	8				
8	no		UPRIGHT	TYPE	5	POSITION	UPRIGHT		
9	8	false							8
10	9	unknown		MAIN TRUNK	9				
11	no		YES	TYPE	5	MAIN TRUNK	YES		
12	9	true		CLASS	1	TYPE	TREE	9	
13	5	unknown		BROAD+FLAT	5				
14	no		NO	CLASS	1	BROAD+FLAT	NO		
15	5	false							5
16	6	true		FAMILY		CLASS	GYMNOSPERM	6	
17	1	unknown		LEAF SHAPE	1				
18	no		SCALELIKE	FAMILY		LEAF SHAPE	SCALELIKE		
19	1	true				FAMILY	CYPRESS	1	

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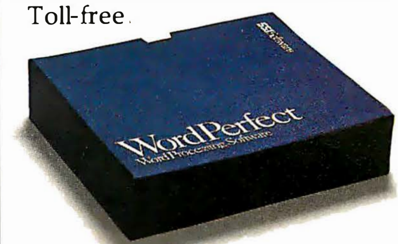
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we have just asked the caller the prompt for BROAD AND FLAT. Before answering, the caller asks why we have asked this particular question. To find the reason we need look no further than the top rule on the goal stack. The reason we are trying to find a value for BROAD AND FLAT is to get one of the pieces of information needed to solve the goal CLASS in rule 5. By fitting the information from the goal stack into the following form we will answer the question "Why?":

We are trying to find a value for the class of the tree.
We already know that the type of the plant is tree.
If we can show that the leaf shape is not broad and flat
then we will know that the class of the tree is gymnosperm.

Notice that we have substituted the translation for each attribute to make the information more readable.

If the caller now wants to know "Why is CLASS important?" the process is repeated, moving back another item in the goal stack. This can continue until all of the subgoals on the stack are exhausted.

Returning to the example above, the caller may now be satisfied with why you have asked about BROAD AND FLAT but may ask, "How do you know that the type of the plant is tree?" This question can be answered by finding where that attribute appears on the context stack. If there is a rule card with the attribute card, the rule on that card caused the value to be placed on the context stack. To answer the question, we would use the information in the rule to form our response:

the type of the plant is tree
was proven using rule 9
This rule states that:
If the stem of the plant is woody
and the position of the stem is upright
and the plant does have one main trunk
then the type of the plant is tree.

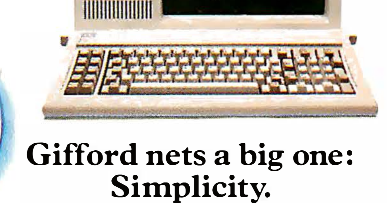
When no rule card is placed with the attribute card on the context stack, we can inform the caller that he or she must have supplied the fact in response to a prompt.

Allowing a caller to interrupt a consultation to ask how and why makes the process more understandable and more educational to both consultant and caller.

Now that we have made a mechanical model that contains all of the pieces of our expert system, it is a fairly straightforward task to lay out program structures to automate the process. We can now introduce some Pascal

(continued)

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structures to aid in the construction of an expert system.

Conceptually, we can separate the knowledge-base rules and attributes from the inference engine, which employs the knowledge base to reach conclusions. Of course, we could hard-wire the knowledge base into the expert-system program, but then the program would be inflexible. If we wanted to expand the knowledge base to include family-of-vines data or to create a different expert system for insect identification, we would have to rewrite the program. Alternatively, we can make it one of the program's duties to read the rules, prompts, and translations from a file and transform them into a form that can be operated on by the inference engine. This is the approach we will take. The translation is accomplished by means of a *parser*. A parser is a routine that reads statements in a given language and determines whether the statements are legal in that language. As a by-product of its activity, a parser may also produce a transformed representation of the statement for use by other parts of the program. The parser we will discuss is available for downloading from BYTEnet Listings (telephone: (603) 924-9820).

One of the decisions that must be made early in the design of an expert system is the method of entry and storage for the knowledge base. One convenient method is the use of a standard text editor to enter and store the rules, prompts, and translations as ASCII (American Standard Code for Information Interchange) text files. This can lead to difficulties in maintaining the integrity of the knowledge base, but it greatly simplifies the overall program design, since it will not be necessary to write any data-entry routines. In our text file, the rules should have the same form as on our index cards.

THE PARSER

The language the parser recognizes is described by a grammar. A grammar is a set of definitions that specify how the basic symbols of the language, called tokens, may be legally combined. In this case, a token is any string of characters surrounded by blanks. We can think of the rules, prompts, and translations as statements in a rule language.

The first step in programming a parser is to completely describe the language that the parser will recognize. The Backus-Naur diagram in table 4 describes the grammar that the program must recognize. Backus-Naur form (BNF) is a shorthand for describing syntax. It uses two special symbols: "::=" (read as "is defined to be") and "|" (read as "or"). For example, the first line of table 4,

sentence ::= rule | prompt | translation

is read "a sentence is defined to be a rule, a prompt, or a translation." Names enclosed in quotes must appear exactly as shown. Other symbols are syntactical categories and are defined in the grammar. The phrase

rule ::= rule_number 'IF' condition 'THEN' conclusion '.'

tells us that a rule is made up of a rule number followed by the keyword "IF." This is followed by a condition (to be defined elsewhere in the grammar), the word "THEN," and a conclusion. Finally a "." terminates the rule. The definition of a condition,

condition ::= clause | clause 'AND' condition

tells us that a condition is made up of a clause or a series of clauses connected by the word "AND." A definition such as this is called right-recursive, since it contains the object being defined on the right-hand end of the definition. The recursion in such a definition doesn't necessarily terminate. A condition could legally consist of an infinite number of clauses. Obviously, any program trying to parse such an object would run into problems of time and memory constraints. The BNF gives a good theoretical definition of the grammar but doesn't necessarily contain information about the practical limitations imposed by implementing the grammar on a real computer.

The advantage of using the BNF definition is that it is relatively straightforward to implement a parser for a grammar that has been defined in this manner. The definition provides a guide for the top-down design of the program. You start by assuming the existence of a routine,

(continued)

Table 4: *The grammar for the expert system's rules, prompts, and translations expressed in* BNF.

```
sentence ::= rule | prompt | translation
rule ::= rule_no 'IF' condition 'THEN' conclusion '.'
rule_no ::= digit | digit rule_no
condition ::= clause | clause 'AND' condition
clause ::= attribute predicate value
attribute ::= token | token attribute          (max 30 characters)
predicate ::= 'IS'
value ::= token | token value                  (max 30 characters)
digit ::= '0' .. '9'
token ::= (any string, up to 30 characters, surrounded by blanks)
prompt ::= '@PROMPT' attribute end_of_line text end_of_line '@'
end_of_line ::= (<RET> for UCSD, <RET><LF> for TURBO)
text ::= (any string, up to 80 characters)
translation ::= '@TRANS' attribute end_of_line text end_of_line '@'
```



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Many of the procedures that will make up the parser are recursive because their definitions are recursive. This technique is called recursive-descent parsing.

which we will call scanf, that will read tokens from the input file.

To write the parser, start at the first line of the grammar and write a procedure that can accept a token from a file and decide if it is the starting token of rule, a prompt, or a translation, read the next token, and call the appropriate routine to analyze the rest of the sentence. The procedure sentence in the BYTEnet program does that. The procedure rule in the same program expects to be called with the token having the value "IF." If this is true, it calls condition; if not, it calls the error routine and exits. This process continues, following the BNF, until we get to the procedures attribute, predicate, and value, which will save the items they recognize for later use.

The definition of value uses "AND" as a terminating token, so that attempting to use values such as "hard and woody" will cause the parser to terminate in an error. We could resolve this problem by modifying the definition of rule in the grammar to use some other keyword in place of "AND" or by building some sort of backtracking into the parser. Backtracking would allow the parser to back up to the point in a sentence that caused an error and try an alternate possibility.

All the procedures making up the parser must cooperate by the convention that when they return they will have scanned past all the tokens that they recognize, leaving the first token in the next phrase in the global variable called token.

Many of the procedures that will make up the parser, such as condition and attribute, are recursive because their definitions are recursive. This type of top-down recursive technique is called recursive-descent parsing.

Using this grammar we can mix rules, prompts, and translations together in one file. The rules illustrated in table 1 can be entered as shown. The prompts and translations in table 2 must be changed in order to match the grammar. For example:

```
@trans stem @
The stem of the plant
@
@prompt stem @
Is the stem of the plant woody or green ?
@
```

(continued)

To change the kind of rules recognized by the program, modify the grammar and then, using the new grammar as a guide, rewrite the routines that process the grammar.

A cross-reference program that uses the parser routines described in this article can be downloaded from BYTEnet. The source code is available in a UCSD or Apple Pascal version and a Turbo Pascal version. The set of rules used in this article is also available as a text file as well as a more complete knowledge base that identifies the genera of conifers in the northeast U.S. The cross-reference program will read a knowledge base from a text file and produce an alphabetized list of the attributes along with their translations, prompts, and values. The numbers of the rules containing each value will also be displayed.

While the cross-reference program represents about 16K bytes of source code, it is only part of an expert system. In the rest of this article, we will present the specifications for a full-blown program to implement the cardboard inference engine in Pascal. The specifications are based on a program we wrote called MicroExpert System, which is available on disk from McGraw-Hill for IBM and Apple computers for $39.95. The package includes full documentation and source code and is a straightforward realization of the complete cardboard inference engine. (MicroExpert is a trademark of MicroExpert Systems.) The cross-reference program on BYTEnet can be used with the MicroExpert program without modification.

DATA STRUCTURES

Parsing ensures that the rules in the file are well formed, but this is only part of an expert system. The major function of the system is to interpret the rules and find a value for the goal of the consultation. The rest of the program must be designed to support this function.

Along with parsing the rules, the program must allocate storage for prompts, translations, and rules. For rules it will be necessary not only to store attributes and values but also to represent the overall structure of the rules in a compact manner. Prompt and translation strings must be stored in a way that will allow them to be associated easily with their respective attributes.

There are numerous methods of accomplishing this association. In our system, MicroExpert, we used linked lists of records called *items* to store most of the data elements necessary for the operation of the inference engine. This is slightly wasteful of storage, but it simplifies the overall program design. Listing 1 shows an item as it would be defined in Pascal.

There are two basic kinds of items. The rule item contains the attribute, the value, the rule number, and the kind of item (condition or conclusion). Since in the rule description we have allowed only one kind of predicate, "IS," we have not included the predicate in the item. For each clause in the rule, an item is created. The items making up the clauses in a rule are linked together by means of a pointer. Finally, another pointer is inserted into an array that points to the first item in the rule. This structure is represented in figure 2. Each rule is thus stored in memory as a pair of linked lists, one for the condition and one for the conclusion of the rule.

Prompts and translations are also stored by means of a linked-list organization. When the parser reading the knowledge-base file encounters a prompt or translation, an item is created for the attribute, if one does not already exist. The item is inserted into a linked list of attribute items and, as prompt and translation lines are read, they are also linked together and pointed to by fields in the attribute list. This structure is diagramed in figure 3.

Linked lists are a useful programming mechanism for manipulating symbolic structures such as rules. Unfortunately, languages like Pascal provide few intrinsic routines for handling lists. In order to implement an expert system in Pascal, routines for manipulating lists and managing storage must be designed. Pascal provides intrinsic procedures for manipulating dynamic storage. Unfortunately, these routines vary somewhat among different versions of Pascal. Most versions provide a new procedure to allocate storage, but the method of releasing dynamic data when it is no longer needed differs slightly among the versions of Pascal that we wished to use.

Since we wanted MicroExpert to run under Apple and Turbo Pascal with only minor modifications, we chose not to use the Pascal intrinsic dispose, which is not included in the Apple version. Instead we maintain another list of items. When a request is made for a new item, the program first checks this list. If the list is empty, it calls the intrinsic function new to get space for the item. If the list is not empty, the top item of the list is returned and the

(continued)

Listing 1: *Pascal code to describe an item and related data types.*

```
TYPE
  string80 = string[80] ;
  word = string[word_size] ;
  counter = 0 . . maxint ;
  item_type = (cond,concld) ;
  item_ptr = ^item ;
  string_ptr = ^string_rec ;
  string_rec = RECORD
                 info : string80 ;
                 next_line : string_ptr ;
               END ;
  item = RECORD
           next : item_ptr ;
           attr : word ;
           CASE boolean OF
             TRUE : ( val : word ;
                      kind : item_type ;
                      rule_no : counter ) ;
             FALSE : ( prompt_ptr : string_ptr ;
                       trans_ptr : string_ptr ;
                       val_ptr : item_ptr) ;
         END ;
```

COND CONCLD

ITEMS

NIL

STEM POSITION

WOODY CREEPING

7

COND COND

8

8 8

9

NIL

TYPE

VINE

CONCLD

8

Figure 2: *The linked-list representation of rule 8.*

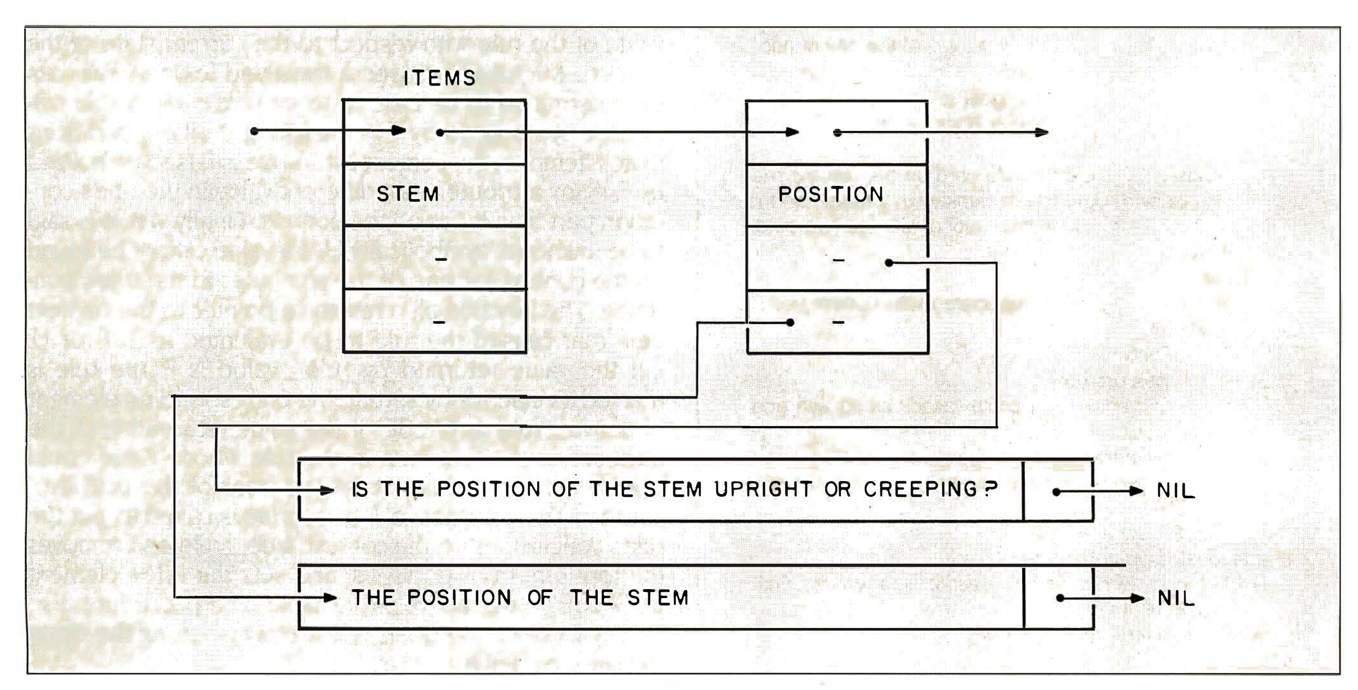


Figure 3: *The linkages between the attribute list and the prompt and translation lists are illustrated for the* POSITION *attribute.*

list pointer is set to point to the next item on the list. Similarly, an item can be released by making its next pointer point to the top of the list and the list pointer point to the just-released item.

Several other list-handling routines will also be necessary. A routine must be included to check to see if a particular attribute is on a given list and, if found, return a pointer to the location on the list. A routine to create a new item, put it on the front of a list, and fill in values for the fields in the item record will be needed. Similar routines will be needed to insert items at the end of a list and to insert an item in a list in alphabetical order.

Besides using these routines, the program builds several other lists that correspond to structures described in the cardboard inference engine. We must build a goal list of items that contains the main goal and subgoals generated by the inference engine. The context is also a linked list of items that is used to keep track of facts derived during processing. Although both of these structures were previously referred to as stacks, we have implemented them as linked lists. Since a stack is just a linked list that is always accessed at its first element, we will use the terms "list" and "stack" interchangeably.

In the description of the cardboard inference engine we mentioned a discard pile upon which rules were placed when they were no longer active. In the program, it is convenient to use an array of Booleans to perform the same function. Each element is initially set to the value TRUE. As the rule becomes inactive by being discovered to be true or false depending upon the current context, the corresponding element in the active-rule array is set to FALSE.

Table 5: *Pseudocode for the inference-engine procedure.*

```
BEGIN
  put the final goal on the goal stack.
  done := false.
  WHILE NOT done DO
    IF a rule can be found to evaluate
      THEN
        CASE value of rule OF
          true      : BEGIN
                         put attribute card from goal stack
                         and the rule card being evaluated
                         on the context stack.
                         IF there was a rule card with the goal
                           put it on top of the pile of rule
                           cards.
                         IF the goal stack is empty
                           THEN done := true.
                       END.
          false     : put the rule card on the discard pile.
          unknown   : put the first unknown attribute on the
                        goal stack along with the rule card.
        END.
      ELSE
        IF there is a prompt associated with current goal
          THEN
            BEGIN
              ask prompt.
              put answer on context stack along with goal
              card.
              IF there was a rule card with the goal card
                place the rule card on top of the rule pile.
            END.
          ELSE done := true.
  IF final goal is on context stack
    THEN the answer is the value associated with the final
         goal attribute.
    ELSE no answer could be found.
END.
```

THE INFERENCE ENGINE

The inference engine can be implemented by following the pseudocode of table 5. This is illustrated by routine infer, shown in listing 2, which begins by calling get_main_goal to ask the user for the final goal of the consultation. It stores this in the global variable main_goal and also creates an item containing main_goal and puts it on the goal_list.

The program then begins to loop until the Boolean variable done becomes TRUE. It first uses the Boolean function found_rule to determine if a rule is available to be evaluated. This function implements the backward-chaining feature of the program and works by searching the conclusion parts of each active rule to see if there is a match for the goal on the top of the goal stack. If it finds a match, the function returns a value of TRUE and a pointer to the item in the rule that gave the match.

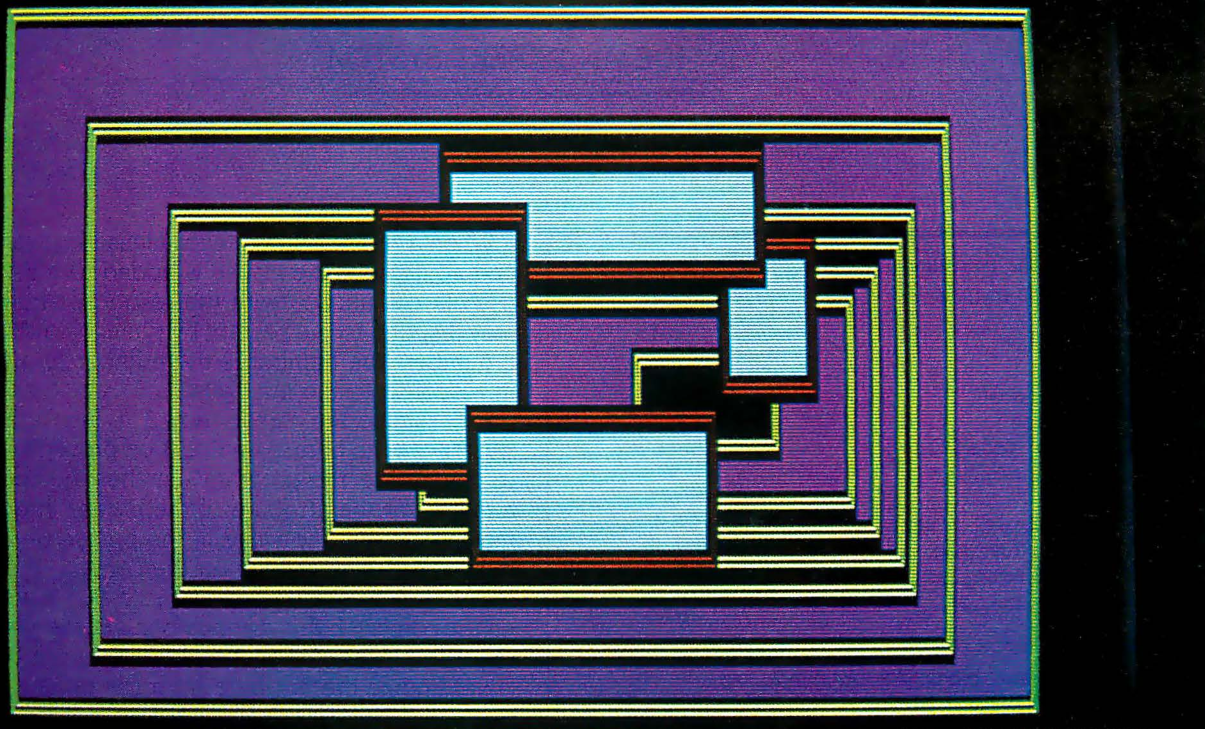
If a rule containing the current goal could be found, the function rule_value is called to determine the logical value of the rule with respect to the current state of the context. MicroExpert uses a tri-valued logic. A rule can be determined to be true, false, or unknown. A rule can be true, symbolized by T in the listing, if all its conditions match items on the context list. A rule is false, symbolized by F, if any attribute has a different value in the rule's condition part than it has on the context. Finally, a rule is said to be unknown, symbolically U, if a value cannot be found on the context for one of the attributes in the rule's condition. The function also returns a pointer to the context item that caused the rule to be evaluated as T, F, or U.

If the value returned by rule_value is F, the rule is marked as inactive by setting the corresponding element of active_rule to FALSE. If the value returned is U, the attribute of the first item in the rule whose value could not be determined is put on the front of the goal list.

If the value returned is T, true_rule is called to put the rule's conclusions on the context; true_rule also removes the top item from goal_list and sets the rule's element to FALSE in the active_rule table. The procedure also checks to see if the goal_list is empty, setting the done indicator to TRUE if it is.

If no rule can be found by found_rule, the program calls

(continued)



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Listing 2: *The procedure* infer *is a Pascal realization of the pseudocode in table* 8.

```
PROCEDURE infer ;
  BEGIN
    get_main_goal ;
    done := false ;
    WHILE NOT done DO
      IF found_rule(ptr)
        THEN
          CASE rule_value(ptr^.rule_no,reason) OF
            T : true_rule ;
            F : active_rule[ptr^.rule_no] := FALSE ;
            U : put_on_goal(reason) ;
          END
        ELSE
          IF found_prompt(attr_list,prmpt_ptr)
            THEN
              BEGIN
                why_ptr := goal_list ;
                get_answer ;
              END
            ELSE done := TRUE ;
      what ;
      IF NOT on_list(main_goal,context,ptr)
        THEN writeln('No value could be found for ',main_goal) ;
    END ; (* infer *)
```

the function found_prompt to search the attribute list for a question to ask the user in order to get a value for the goal. The function returns a value of TRUE and a pointer to the matching element in the attribute list if the attribute has a prompt associated with it.

If a prompt cannot be found, the done indicator is set to TRUE and the loop terminates. This usually indicates some kind of inconsistency in the rule base, and the interpreter will terminate without finding a value for the main goal. If a prompt was returned, get_answer is called to display the prompt and get a value for the goal attribute from the user.

The program continues in this manner, searching for rules to evaluate and, when necessary, asking the user for information, until either the goal list is exhausted or no prompt can be found. The program then calls what to print out the contents of the context and finally checks the context list and prints a message if the main goal is not on the context.

IMPLEMENTING WHY AND HOW

In response to the user query "why," the program prints out the goal pointed to by why_ptr, which infer initially set to point to the current goal. It also prints the translated rule that caused the goal to be placed on the goal list. The rule number for this rule was stored in the goal item when the item was created by put_on_goal; why_ptr is then updated to point to the next goal on the list, so that successive responses of "why" will print the contents of goal_list and the rules examined by the system in establishing the goals.

When a rule is printed, each clause is given a number, and an item for the clause is added to a list. This list is used in conjunction with the response "how." The user may respond to the prompt by typing "how" followed by a number. The number is the number of a line printed in response to the last "why."

For example, the phrase "how 3" is interpreted as "How was or can the phrase on line 3 be proven?" In response to this phrase, the program searches the context list for a match for the attribute of the phrase in question. If a match is found, the value in the phrase is compared to the corresponding value on the context. If these values match, the program prints the rule that placed the item on the context. If this rule number is 0, the program prints that the phrase was proven by user input.

Not finding the attribute from the phrase on the context indicates the logical value of the phrase has not yet been determined. In this case, the conclusion parts of the rules are searched for a match for the attribute in the phrase. If a match is found, the rule number of the matching rule is printed. If no match can be found, a message is printed indicating that the phrase can be determined only by user input.

VARIATIONS ON A THEME

The system we have described and our MicroExpert program are both designed for people who want to experiment with expert systems. What we have tried to provide is the bare bones of an expert system, with enough modularity and openness of design to encourage modification and experimentation. As a conclusion to our article, we would like to suggest some possible directions for variation in the design that we have presented.

As we mentioned, the structure of inference on the cardboard system is backward chaining. An equally valid method of inference is the forward-chaining or data-driven engine. In this method, at any point during the consultation, the system searches the condition parts of the rules for any rule that may be true and performs their conclusion part. This adds new information to the context, and the process is repeated.

Methods can also be designed that are combinations of the two types of inference. As described, we put only the conclusion of the current rule on the context, i.e., the rule that produced the current goal. Finding a value for this goal may cause other rules to become true, but the system will ignore them. A relatively simple modification would be to search the rule base for all rules that have the current goal in their conditions and evaluate them. If any of these rules add items to the context, repeat the process until no new items are added.

Another useful modification to the inference engine would be the inclusion of new predicates such as "IS NOT" and numerical operators such as "+," "−," "*," and "/." These predicates would allow more complex relationships among attributes but will also increase the complexity of the function that evaluates the rules. ■

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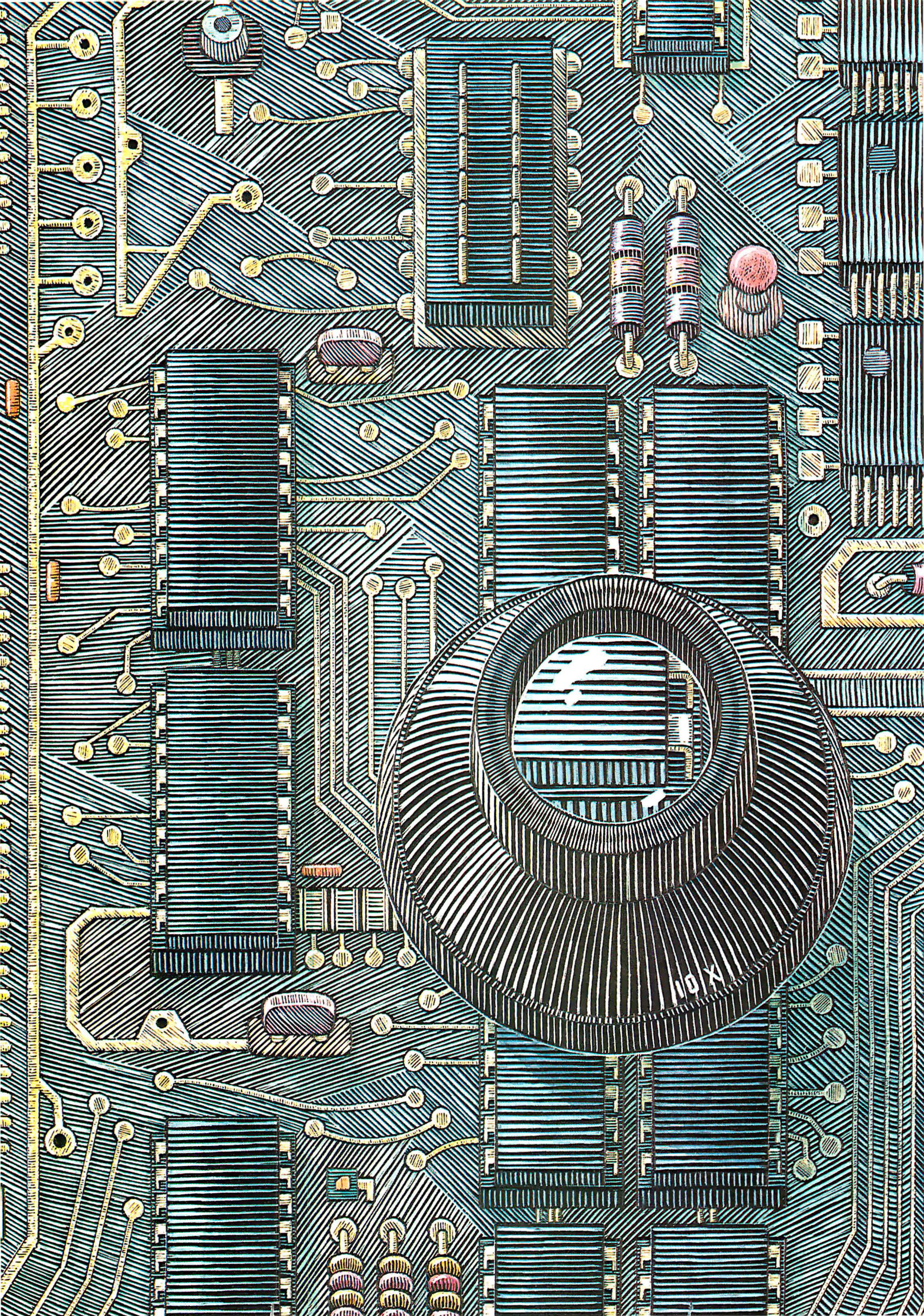
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13 CORPORATE ACCOUNT PROGRAM—Almost 50% of The NETWORK's members are corporate buyers and users *(see opposite page left).* The NETWORK can establish open account status and assign designated account managers to expedite orders, and coordinate multiple location shipments.

14 QUANTITY DISCOUNTS—For large corporations, clubs, and repeat or quantity buyers The NETWORK can extend additional single order discounts, when available to us from our manufacturers and distributors.

15 PRICE PROTECTION—The PC Industry is crazy!! Prices change not yearly or monthly or even weekly but often day by day! These changes are sometimes up *but are mostly down!!!* **THE NETWORK GUARANTEES THAT IN THE EVENT OF A PRODUCT PRICE REDUCTION, BETWEEN THE TIME YOU PLACE YOUR ORDER AND THE TIME THE PRODUCT SHIPS YOU WILL ONLY PAY THE LOWER AMOUNT!!**


10X

Reviews

ARTIFICIAL INTELLIGENCE. The phrase seems randomly applied in a wide variety of contexts by a growing number of people from diverse backgrounds. This month's theme section gives you the theories and the potential as viewed by some of the world's most astute observers. "But," you ask yourself, "what can I do with it?" And in order to answer that question satisfactorily you have to know what products are available now, what they can do, and their specific approach to AI. One point you couldn't really get away from until now was the fact that most AI products were specialized and expensive. Building your own knowledge base and using the computer to help you arrive at a solution that neither you nor it knew in advance depended on custom databases and large amounts of computing power. With our first review this month, we see that things may be starting to change.

Insight, from Level 5 Research, sells for $95, is designed for IBM Personal Computers (PCs) and compatibles, and lets you build your own expert system through goal-outlining procedures and probabilistic reasoning. Reviewer Bruce D'Ambrosio doesn't give it high marks for completeness, but he notes that some of the basic tools are there. For example, while Insight gives you Boolean and numeric data types, it does not give you character data or the capability to structure variables into records or frames. Still, its inability to structure data isn't a major handicap as long as the problems are simple and you use a single kind of data. Mr. D'Ambrosio gives Insight a nod as a possible AI learning aid. Expert-system development tools are beginning to work their way down to the microcomputer level, and Insight is an example of something you can use right now. It's not fully realized in some respects, but it's not a game either.

John Unger takes a look at ITT's entry in the IBM PC-compatible sweepstakes, the XTRA. Mr. Unger notes that while the XTRA may be attractive in a lot of home or office situations, it breaks no technological ground. It uses an 8088 microprocessor at a 5-MHz clock rate, just slightly faster than the IBM PC's 4.77 MHz but not so fast that it can't run most IBM PC applications software. ITT bundles a communications package with the XTRA, which is logical enough when you think about it. Except that not every communications company thought about it. The AT&T 6300, for example, is bereft of communications software. It's an indication that the XTRA's designers and packagers used some forethought. Mr. Unger reports that the XTRA features a number of these design touches, which seem to indicate that the company made an effort to provide a product that can complement, as well as compete with, the IBM PC.

—Glenn Hartwig, Technical Editor, Reviews

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	512K	1Mbyte	2Mbyte
SemiDisk I, S-100	$995	$1795	
SemiDisk II, S-100	$1295	$2095	$2549
IBM PC, XT, AT	$945	$1795	$2499
QX-10, QX-16	$799		$2499
TRS-80 II,12,16	$995	$1795	$2499
Battery Backup Unit	$150		

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Cygnet Technologies Inc.'s Communication CoSystem is a combination of hardware and software for integrating the telephone with your IBM Personal Computer (PC) or compatible. For example, you can use it to store a 400-listing telephone directory—each number of which you can access by category, alphabetical order, frequency of use, or with a special speed-dialing code. Each desktop unit gives you one or two telephone lines that you can mix between tone dialing or rotary dialing or both. You get three-party conference calling. You can dial with the phone still on the hook; this is actually more useful than it sounds because you can listen with half an ear to a volume-controllable speaker for the other party to pick up before you have to give it your complete attention. You also get the option of connecting a microphone and using the unit for general conference calling.

If you have two or more CoSystems you get attended or unattended electronic mail. You can also exchange screens and send and receive files to disk. An electronic calendar lets you store your appointments, and it beeps when it's time to be somewhere, call someone, or do something.

What it won't do is let you use one telephone line simultaneously for both voice and data. I've heard about exotic systems that provide this kind of line sharing, and I thought CoSystem—priced at about $1800—was expensive enough to be that exotic.

Still, for an office where individuals do a lot of telephone work along with a lot of noncommunicating work on an IBM PC, the CoSystem offers a lot of useful features. Because of the price tag, I doubt if it will displace a pop-up menu program combined with a regular push-button-phone/modem-within-arm's-reach for most BYTE readers, but I wouldn't be surprised if I saw one in use at a car-rental agency.

General Computer Company, Cambridge, Massachusetts, showed us its Hyperdrive, an internally mounted 10-megabyte hard disk for the Macintosh. The expansion package also grows the RAM to 512K bytes. What the company does is line up a dealer. You go to the dealer, who takes your Mac, opens it up, installs the hard disk and new RAM, closes it up, gives it back, and charges you $2795. Simple, except that it voids the Apple warranty. To get around this, General Computer issues you a new warranty for your Mac as well as for whatever the dealer installs (you can get the Hyperdrive without the 512K-byte expansion package for $2195 if you already have a Fat Mac, but one way or another, you have to have 512K bytes on your machine). General Computer also installs a fan with a temperature-sensor circuit that kicks into high when the temperature rises.

By mounting the hard disk internally and using a direct logic board interface to connect it to the Mac's main circuit, General Computer has left the serial port alone. You still get to use the standard connections for the modem, printer, or Applebus.

Hyperdrive comes also with extensions to the Macintosh system software. You can partition the hard disk into 32 file drawers or "virtual disks" that automatically resize themselves whenever you add or remove data. You can add password protection at the file level, and you can also encrypt your files and applications. The icon-oriented user interface stays the same, except that you get new icons for the new functions.

We're supposed to get one of these megaMacs for evaluation, and I'm looking forward to seeing how well it performs.

We've been running the Ericsson PC for the past few weeks as a sort of common-property IBM-compatible for those of us who need only occasional access to the 5¼-inch MS-DOS/PC-DOS format. It has a very nice amber-on-brown display, and the little stand for elevating the monitor is one of those features whose merits become increasingly appreciated. It's supposed to have an ergonomically enhanced keyboard, and on the desk it does seem quite comfortable; for laptop typing, however, I found it too light and the cord too short. Hardly major complaints, being subjective as they are. Too, I thought it curious but not horribly distressing that, while compatible with all of the application programs we have put into it, it will boot only its own version of DOS. The MS-DOS we've used for other IBM PC-compatibles simply won't work. It's not that the disk just spins forever in the drive—the screen goes dead, the drive unit goes dead, and you can't restart it with a Ctrl-Alt-Del. However, seeing as how you get Ericsson DOS with the system, this particular curiosity is simply a curiosity and nothing more.

The Ericsson PC looks intriguing from a number of aspects. It does seem generally compatible with most standard software, and it gives the appearance of being well planned in terms of those features the user will have the most contact with, i.e., the keyboard and the screen. It has a nice small footprint for a desktop, and the evaluation unit sent to us came with a rack for housing it on edge on the floor. This is another unit I'm looking forward to reviewing.

—Glenn Hartwig, Technical Editor, Reviews



S·Y·S·T·E·M R·E·V·I·E·W

The ITT XTRA

It's compatible with—and it improves upon—the IBM PC

BY JOHN D. UNGER

The IBM Personal Computer (PC) is an easy mark for improvement, and almost every compatible today does many things faster or better than the PC. The ITT XTRA is no exception; it combines compatibility with a number of improvements on the IBM PC and some of the clones. There are, however, no important hardware innovations to differentiate it from compatible microcomputers. Rather, some other, more subtle reasons may form the basis for choosing the XTRA.

It appears that ITT is aiming the machine at business users who have an IBM or similar computer at the office and want a compatible machine at home. The communications software bundled with the XTRA suits this purpose.

A color/graphics board also allows the computer to run IBM PC game software. I reviewed an XTRA with 256K bytes of RAM (random-access read/write memory), two double-sided double-density floppy-disk drives, and a monochrome monitor and monochrome display board. This standard configuration has a list price of $2395.

HARDWARE

The XTRA (see photo 1) has the conventional three-piece grouping: a main unit that contains the processor and disk drives, the monitor, and a detached keyboard.

The ASCII (American Standard Code for Information Interchange) keyboard differs slightly from the IBM PC/XT keyboard (see photo 2). Both the Caps Lock and Num Lock keys have light-emitting diodes (LEDs). All of the keys repeat after about half a second. The keycodes are identical to those for the IBM PC.

The amber monitor measures 12 inches diagonally and produces crisp, high-quality characters in a font style that is easy to read (see photo 3). The characters, formed from a 7- by 9-pixel matrix in a 9- by 12-pixel cell, are displayed on an 80 by 25 screen. There is no blurring or distortion as the screen scrolls. The monochrome mode includes the standard attributes—reverse video, blinking, half- and high-intensity, and underlining—in various combinations and permutations. I cannot say much about the graphics capability of the system since I did not have a graphics board to test in the XTRA. However, I did note that the BIOS (basic input/output system) ROM (read-only memory) routines included interrupt-driven functions that appear identical to those used in creating medium- and high-resolution graphics on the IBM PC, and graphics video RAM is located at the same memory addresses as in the IBM PC.

STORAGE

The XTRA uses half-height double-sided double-density disk drives, each with a storage capacity of 360K bytes. The drives operate quietly. However, the slot for the lower or B: drive sits only 2⅝ inches above the table top. If the keyboard is less than 6 or 7 inches from the front of the main unit, it is difficult to insert disks into the drive without flexing them somewhat to clear the keyboard.

The user's guide contains complete and easy-to-follow instructions for installing a half-height 10-megabyte hard-disk drive. This is a modification that requires an expansion card with a controller for the hard disk.

INTERNALS

To lift the cover off the main unit and gain access to the IBM-compatible expansion slots, the disk drives, and the motherboard, you need only remove two screws from the rear panel. The XTRA uses an 8088 microprocessor at 5 MHz, a nominally faster clock rate than the IBM PC's 4.77 MHz. Next to the 8088 is a socket for installing an 8087 arithmetic coprocessor. The motherboard can hold 256K bytes of RAM (the XTRA uses standard 4164 64K-bit RAM chips in its memory); expansion cards can bring additional memory to a total of 640K bytes. Because the XTRA performs a parity check

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on its RAM, nine 64K-bit chips have to be installed for every additional 64K bytes of memory. When powered up, the system takes about 32 seconds to check the RAM with 256K bytes installed. To disable the check, you can open the case and easily set 1 position on one of two 8-position DIP (dual-inline package) switches. The switches also set the amount of motherboard memory, the type of monitor, the number of floppy-disk drives, a screen time-out feature, and the presence or absence of the 8087 coprocessor.

The XTRA comes with 32K bytes of ROM, most of which holds the BIOS, but the ROM also provides a set of system diagnostics. These routines are mentioned only briefly in the documentation I received, but the optional technical reference manual describes them in more detail. Pressing the Esc, Ctrl, and Alt keys at the same time runs the program. Typing H at the => prompt gives you a menu with options for running diagnostics of the system hardware, memory, disk drives, video display, and keyboard. The menu also provides access to powerful utilities that read and modify disk sectors and memory.

INTERFACES

The main unit's back panel contains two 25-pin DB-25 connectors. One, labeled "Printer," is a female Centronics-compatible printer port; the other, marked "Comm. Line," is an RS-232C male asynchronous serial port for communications or a serial printer. An ITT-supplied communications program can configure the serial port from 110 to 9600 bps (bits per second). Both ports are "hard-wired" into the motherboard and therefore do not use the expansion slots. The optional Combo expansion board includes a second parallel printer port.

SOFTWARE

Advertisements I have seen offer the XTRA only with the standard ITT-DOS 2.11 (MS-DOS 2.11) and Advanced BASIC, ITT's BASIC-language interpreter. As might be expected from a communications company like ITT, the ITT-DOS disk contains an asynchronous communications program that enables you to access on-line telecommunications services as soon as you connect your modem. Or you can access a nearby computer by running a cable directly from the RS-232C communications port on the XTRA. The communications program includes options to choose parameters, to upload or download ASCII files, and to exit to the operating system without disconnecting. It is a simple, straightforward communications program, but it lacks many of the features—like providing a directory of

(continued)



Photo 1: An ITT XTRA *with two* 360K-*byte disk drives.*

phone numbers—of PC-Talk III.

ITT describes Advanced BASIC as Microsoft MS-BASIC with GW-BASIC extensions. The full-screen editor and command syntax will be familiar to users of either BASICA or GW-BASIC. The graphics and music commands are identical to those of BASICA; in fact, the two chapters in the ITT BASIC manual describing these features are taken directly from Lyle J. Graham's *Your IBM PC* (Berkeley, CA: Osborne/McGraw-Hill, 1983). Improvements in the BASIC benchmarks over those for the IBM PC must be owing to enhancements in the BASIC interpreter because the processor clock speeds are nearly identical. The user's guide suggests that the disk with the BASIC interpreter includes a number of sample BASIC programs, but the disk I received with my system did not contain these files.

I used WordStar and Multiplan written for the IBM PC to run the benchmark tests for the XTRA; both packages ran perfectly.

Documentation

The user's guide provides simple, easy-to-follow instructions for setting up peripherals and the computer hardware; it also describes the MS-DOS functions that run the system software. The BASIC manual is well organized, with separate sections on file I/O (input/output) and the more complex graphics and sound commands. The third manual explains the MS-DOS commands and the more elaborate programs like EDLIN and DEBUG. The manual is quite complete and includes the DOS functions available through BIOS ROM interrupts, of considerable interest to programmers writing software for the XTRA.

Compatibility

I tested a few crucial pieces of IBM software, including WordStar, Multiplan, and the DeSmet C Compiler; all of them ran without problems. Perhaps more important, I examined the BIOS ROM interrupt structure and memory model. There is little to prevent almost complete compatibility with the IBM PC. The biggest difference between the XTRA and the IBM is that the IBM has part of its BASIC interpreter in ROM. Software that uses this feature directly will not run on the XTRA.

There is excellent compatibility between IBM BASIC and ITT's Advanced BASIC. Virtually all programs written in BASIC for the IBM should run on the XTRA with little modification.

The five IBM-compatible expansion slots on the XTRA enable you to add many optional features and functions. Of course, the only sure compatibility test for software and hardware is to try it on the XTRA.

Sales and Support

The first XTRA advertisements I saw proclaimed a nationwide sales and service network through the ComputerLand franchise. I visited a near-

(continued)

Photo 2: *The* ITT XTRA *keyboard has* LEDs *on the* Caps Lock *and* Num Lock *keys and a layout that resembles the* IBM Selectric.

Photo 3: A *sample screen display on the* ITT XTRA's *amber monitor.*

AT A GLANCE

Name
ITT XTRA

Manufacturer
ITT Information Systems
POB 52016
Phoenix, AZ 85072
(800) 321-9872

Components
Processor: 8088 at 5 MHz; socket for 8087 coprocessor
Memory: 128K dynamic RAM (standard) expandable in 128K increments to 640K; 32K ROM (BIOS, bootstrap, and self-test) expandable to 64K; 4K text video RAM on monochrome board, 16K graphics video RAM on color/graphics board
Display: monochrome is 80 columns by 25 lines
Monitor: monochrome, 12-inch diagonal, 640- by 400-pixel resolution
Keyboard: detached QWERTY with 84 keys including 10 function keys, numeric keypad, and cursor keys

Software
MS-DOS 2.11, Advanced BASIC, asynchronous communications

Expansion Capability
Five card slots (IBM PC bus)

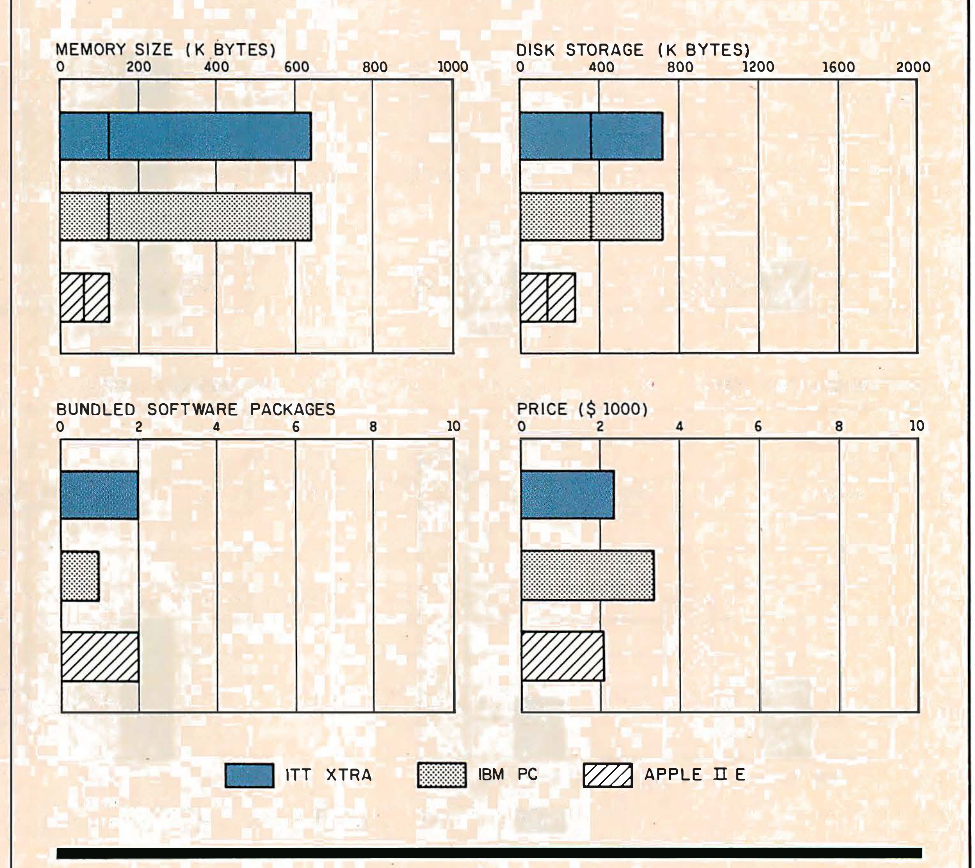
Documentation
User's guide, 218 pages; Advanced BASIC manual, 505 pages; ITT-DOS manual, 410 pages

Prices

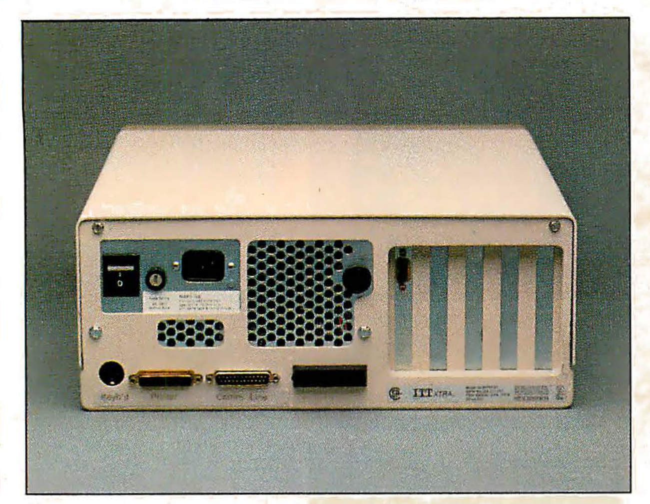
Model I (128K, single 360K drive, monochrome)	$1895
Model II (256K, two drives, monochrome)	$2395
Model III (256K, single drive, 10-megabyte hard disk, monochrome)	$4395

Monochrome units include monochrome monitor and monochrome expansion board

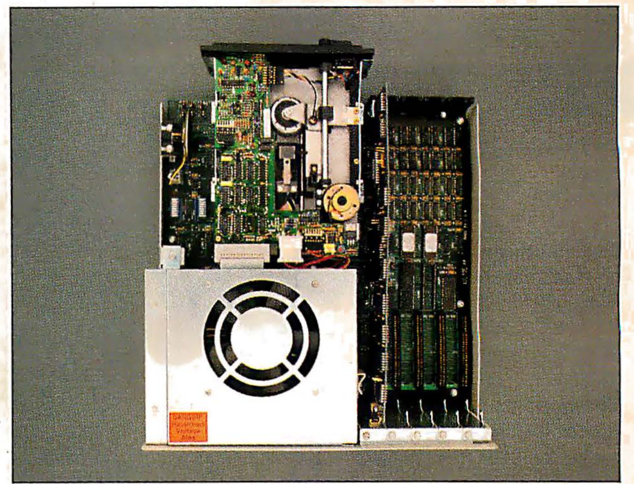




The Memory Size graph shows the standard and optional memory available for the three computers under comparison. The Disk Storage graph shows the highest capacity of a single floppy-disk drive for each system. The Bundled Software Packages graph shows the number of software packages included with each system. The Price graph shows the list price of a system with two high-capacity floppy-disk drives, a monochrome monitor, a printer port and a serial port, 256K bytes of memory (64K bytes for 8-bit systems), and the standard operating system and BASIC interpreter for each system. Note that the price of the ITT XTRA does not include the cost of the color/graphics board.



The rear panel has a Centronics-compatible printer port, an RS-232C port, and five IBM-compatible expansion slots.



Inside the XTRA. The disk drive extends toward the front of the unit. The five expansion slots and fan are evident.

DISK ACCESS IN BASIC (SEC)

	ITT XTRA	IBM PC	APPLE IIE
WRITE	33	56	37
READ	32	46	36

BASIC PERFORMANCE (SEC)

	ITT XTRA	IBM PC	APPLE IIE
SIEVE	185	191	245
CALCULATIONS	56	69	94

SYSTEM UTILITIES (SEC)

	ITT XTRA	IBM PC	APPLE IIE
40K FORMAT/DISK COPY	11	9.6	22
40K FILE COPY	8.8	5.8	45

SPREADSHEET (SEC)

	ITT XTRA	IBM PC	APPLE IIE
LOAD	10	8.1	18
RECALCULATE	10	11	22

The graph for Disk Access in BASIC shows how long it takes to write and to read a 64K-byte sequential text file to a blank floppy disk. (For the program listings see June 1984 BYTE, page 327, and October, page 33.) In the BASIC Performance graph, the Sieve results show how long it takes to run one iteration of the Sieve of Eratosthenes prime-number benchmark. In the same graph, the Calculations column shows how long it takes to do 10,000 multiplication and division operations using single-precision numbers. The System Utilities graph shows how long it takes to format and copy a disk (adjusted time for 40K bytes of disk data) and to transfer a 40K-byte file using the system utilities. The Spreadsheet graph shows how long the computers take to load and recalculate a 25- by 25-cell spreadsheet where each cell equals 1.001 times the cell to its left. Microsoft Multiplan was the spreadsheet used. The tests for the XTRA used MS-DOS 2.11 and ITT Advanced BASIC. Tests for the Apple IIe were done with ProDOS. The IBM PC was tested with PC-DOS 2.0.

by outlet to get some background pricing and technical information and to see what kind of support an owner of an XTRA might receive. I didn't mention that I was writing a review of the XTRA. A prominently displayed XTRA with a large "40% OFF" sign immediately caught my eye. A salesman told me that I was indeed a lucky fellow if I wanted an XTRA because the store had two hard-disk models in stock at a sale price of $2995, marked down from the list price of $4995. When I asked about the sale, he told me that the computer had not "moved" very well, and that they were no longer going to stock it.

I telephoned two other stores. At the first store, someone said they had never sold the XTRA. When I mentioned ITT's claim that ComputerLand franchises are selling the machine, the person said that individual store managers could decide whether to carry a given computer. A salesman at the third store said that they had stocked the XTRA for a few months but discontinued it due to poor sales.

I still needed information on the price and on the availability of hardware and software options, so I called the toll-free phone number that ITT provides. A very helpful woman described the available options but said that she "wasn't allowed" to give out prices. ITT was running a promotional rebate program for the XTRA, and each dealership could set its own price for the microcomputer in order to compete for prizes. She then gave me the phone numbers for the stores I had already contacted; when I explained my experience with these stores, she gave me the phone number of ITT's sales representative for my area, whom I then called. He informed me that he worked for the part of the ITT sales force that deals with large purchases. Nonetheless, he gave me price information and told me that he could sell at list price to individuals if they couldn't otherwise find what they wanted.

Conclusion

The machine appears to be well made and sturdy; I had absolutely no trouble with it. And if something goes wrong, the built-in diagnostics should help pinpoint problems. The documentation lets even novice computer users set up the hardware and get the system running smoothly. The XTRA should run most of the software available for the PC, and it is easy to add PC-style expansion boards. However, you should consider ITT's relationship with ComputerLand and where you would go for sales and support. ITT's toll-free telephone number ((800) 321-7661) for technical information compensates somewhat for the problem. ITT's low price, especially considering the discounts I encountered, makes the XTRA an attractive value. ■

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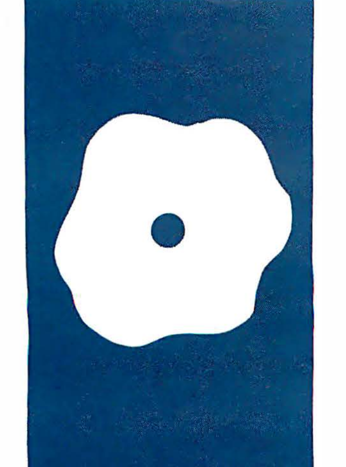


ALLOY QICSTOR-PLUS

COMDEX/Spring '85

ALLOY
Computer Products, Inc.

Alloy Computer Products Inc., 100 Pennsylvania Avenue, Framingham, Massachusetts 01701. Tel: (617) 875-6100, TWX: 710-346-0394
In Europe: Alloy Computer Products (Europe), Ltd., Cirencester, Gloucestershire, England. Tel: 0285-68709, Tlx: 43340



S·O·F·T·W·A·R·E R·E·V·I·E·W

Insight— A Knowledge System

An expert system with limited potential

BY
BRUCE D'AMBROSIO

Insight, an artificial-intelligence (AI) system developed by Level 5 Research for IBM PCs and compatibles, lets users develop expert systems at reasonable cost. Insight is a user-friendly, rule-based, knowledge system, combining If. . .Then rules with goal outlining and probabilistic reasoning. It needs 128K bytes of RAM (random-access read/write memory) and one disk drive, and it sells for $95. Upon close examination Insight is limited and lacks many facilities required for developing practical knowledge-based programs. It might be best suited for educational purposes.

Insight is a member of a growing class of programming systems that are rule-based. These programming systems include an "inference engine" capable of flexibly interconnecting facts the programmer (knowledge engineer) provides specific to the problem. This frees you from concern about the flow of control in the program and lets you concentrate on the knowledge necessary to solve the problem. Key aspects of such systems are the facilities for structuring data, the flexibility of the rule language, the efficiency of the inference engine, and the program-development environment (availability of an editor, debugger, etc.).

DATA STRUCTURING

AI systems are designed for complex problems that are not amenable to normal programming techniques, and they have generally provided highly sophisticated facilities for structuring data. Although Insight has two basic data types, Boolean and numeric, neither character data nor the simplest structuring of variables into records or frames is available. Also, variables reside in a single global context, analogous to early compilers in which no local variables existed within subroutines.

Variable names in Insight can have embedded spaces; this permits writing rules that look very advanced but have an underlying simplicity. For example, in Insight you can write

```
IF the animal has hair
THEN the animal is a mammal
```

This looks less impressive if you know that the animal has hair is simply a variable name and could just as easily have been written the-animal-has-hair.

This lack of data-structuring capability is not important for simple problems in which you never need to consider more than one of any kind of data. Imagine, however, a problem in which you need to consider several pieces of data of the same type. For example, you might need to gather information about all of an individual's bank accounts to advise him on banking services. Or you might have a diagnostic program that needs to gather information about several occurrences of failure before reaching a diagnosis. Rule-based systems do exist that offer the ability to structure basic data into more complex units that can be referred to independently. (EMYCIN, the first general-purpose mainframe system designed for expert-system development, has such a facility called "contexts.")

For example, you might gather all the facts about a bank account into a context called "bank account." You would then be able to write a rule in the form

```
IF there is a bank account with
deposits > $10,000
AND that same bank account has
stable months > 6
THEN . . . .
```

You could achieve the same effect in Insight only by laboriously reproducing each rule and data item and adding an extra variable to record the number of accounts:

```
IF number of accounts ≥ 1
AND bank account 1 deposit amount
> $10,000
AND bank account 1 stable months >6
THEN . . .
```

(continued)

Bruce D'Ambrosio (555 Tulsa St., San Lorenzo, CA 94580) is studying for his Ph.D. in computer science at the University of California at Berkeley.

AT A GLANCE

Name
Insight

Type
Knowledge system

Manufacturer
Level 5 Research
4980 South A-1-A
Melbourne Beach, FL 32951
(305) 676-5810

Format
5¼-inch floppy disk

Computer
IBM PC or compatible, DEC Rainbow, Victor 9000

Features
Rule compiler, inference engine, and sample knowledge bases

Documentation
44-page users guide

Price
$95

Audience
Those interested in AI technology and expert systems

Comments
A simple system of limited utility—best as an educational tool

IF number of accounts ≥ 2
AND bank account 2 deposit amount > $10,000
AND bank account 2 stable months > 6
THEN . . .

You have to hope that no one has more accounts than you allowed for. While you could use this technique for simple situations, you're in trouble if you need to nest such constructs (for example, if you wish to record a series of deposits for each bank account).

RULE LANGUAGE

Like the data-structuring facility, Insight's rule language is the minimum for a rule-based system. Unlike the data facility, however, there is no way around the limitations. The only operations available in Insight's rule language are testing a Boolean variable's truth value, comparison of a numeric variable's value to a constant, and display of recorded text. Insight provides no facilities for assigning values to numeric variables (other than by asking the user), performing even the most limited forms of arithmetic computation, or modifying text in any way before display (for example, by inserting the user name or the name of the current context).

Perhaps the language's most limiting feature is that it does not provide any underlying general-purpose language into which the knowledge engineer can escape. It has been estimated that as much as 30 to 50 percent of the knowledge in a typical EMYCIN system is not in rules but is coded directly in LISP. Personal Consultant, a Texas Instruments knowledge-engineering tool for its TI PC, provides this facility with an escape into IQLISP, the underlying language. And M.1, a knowledge system from Teknowledge (Palo Alto, California) for the IBM PC, has extended the rule language into a complete symbolic-programming system, so that any arbitrary knowledge can be incorporated. Insight has provided neither of these alternatives, and this seems to be a serious limitation.

As an example, consider the following rule:

IF liquid assets + equity > $100,000
THEN client is wealthy

Insight has no way to express this rule, except for the trivial interpretation that liquid assets + equity is a single variable.

INFERENCE ENGINE

The inference engine in Insight, like that in many rule-based systems, is a simple backward-chaining engine. Insight also has a structured goal mechanism that provides some explicit measure of control over the running knowledge program. This facility lets you specify which problem areas in a particular Insight knowledge base interest you. And it allows construction of large multifaceted knowledge bases. I found this of limited utility.

Other facilities provided by the inference component of some knowledge systems include "why" questions that display the currently active rule, display of text that further describes the information requested, and justifications of conclusions reached. Although Insight always displays the most immediate conclusion being sought, it does not provide any facility to display the entire rule or any way to display the chain of reasoning that led it to consider that rule.

One nice feature is the ability to attach text explanations to variables. When a value is requested for a variable, say "liquid assets," you can press function key 4 to get an explanation of the term "liquid assets."

And finally, Insight has an optional report that you can produce at the end of a consultation and direct to the console or the printer; the report serves some of the purposes of justification. However, this report appears to be a randomly ordered listing of all rules considered and the conclusion reached. For one simple problem I presented (using the 15 rules for determining an animal species), Insight produced a five-page justification listing. A justification should be

a more reasoned argument, limited to those rules that directly apply to the conclusions. This report feature might be useful for debugging, but it is not of much use as an end-user facility.

Environment

The user interacts with Insight through a menu- and function-key-based interface. This interface is simple, easy to use, and seems well thought out. When the system can determine a list of options for a variable, it presents them, and you can scroll through the list with the cursor until you select the desired option (shown by highlighting).

You can use the function keys to select options such as restart (start the consultation over from the beginning), expand (display text explanation of this variable if one is available), and help (display Insight's internal-help text describing what is happening, format for correct entry, and so on). The combination of user-defined expand displays, clear internal-help text, and menu-based display and input do make an Insight knowledge system easy to use.

In General

Insight is a compiler-based system, so rules, once written, must be processed by a rule compiler before the Insight inference engine can use them. Most of the compiler/interpreter arguments apply to rule-based languages as well as procedural languages, so you would expect Insight to be fast, capable of handling large programs, but not as convenient for program development. In fact, all these expectations are correct. (Insight is memory-dependent, but on my system the compiler can compile rule bases of over 4000 rules. M.1 can hold only about 200 rules, and TI PC about 400.)

Insight has shortcomings if you use it for program development. You cannot obtain displays of the currently active rule chains. Since it is the inference engine, not the knowledge engineer, that links rules together, such a display would be very helpful in understanding the relationships between rules when building a knowledge base and would help the user understand why a rule-based program is asking a particular question. Also, as is usual with compiler-based systems, you cannot interrupt a running program and inquire about the values of program variables (actually, symbolic debuggers for compiled procedural languages do offer this capability, but Insight has nothing comparable).

Insight provides no special aids for program development. The knowledge engineer must supply his own editor for constructing rule bases. Once a rule base is built as a text file, the PRGEN compiler converts the rule base into executable form. The compiler has no options, and errors detected during compiling are displayed on the console. The error display includes the text-file line number and a short error message. Although these error messages don't always point directly to the problem in the source file, it is not too difficult to figure out what to change.

Finally, the Insight users manual (44 pages plus appendixes) is adequate for using the system but leaves many areas vague. I would like more information on such details as the algorithms used for confidence value combination or the internal structure of the inference engine. [*Editor's note: A confidence value is a method of answering an Insight question that is a numeric value between an absolute yes (a confidence value of* 1) *and an absolute no (with a value of* 0). *For example, if you were developing an expert system for choosing a wine, you could tell an expert system that you liked white wine with a confidence value of* 0.8.] Such information can be important when you are attempting to engineer a complex knowledge base.

For building rule-based systems, Insight is a product that offers a friendly user interface and a rule compiler for fast execution of large rule bases. For $95, it offers an inexpensive way to explore the possibilities of rule-based systems. Its data-structuring facilities and rule language are so limited, however, that it is only suitable for a small class of problems. ■

More on MultiMate

C J Puotinen did not stress enough MultiMate's problems with repagination and virtual paging in "Leading Edge and MultiMate" (November 1984, page 287). The product is a nightmare for anyone who writes more than one-page documents. MultiMate was geared toward a secretarial staff, but it's being recommended by salespeople as a Wang clone. There is no comparison; Wang's dedicated word processor works without a hitch, and professional writers can use it comfortably for composition.

MultiMate is so unreliable that you shouldn't trust it for important documents. It is also unbearably slow for final editing when you are switching between pages.

MultiMate works so poorly that I'm reluctant to spend money on a replacement in case that doesn't work either. Suffice it to say, I've learned to take the time to make backup copies so I can recover the parts of text I lose when repagination doesn't work. And Ms. Puotinen doesn't even mention how inconvenient it is to make a backup copy or the time it takes to proofread documents for MultiMate's errors. Before switching to a Tandy 2000 and MultiMate, I used Microsoft Word and an IBM PC; I have regretted my switch since I made it.

Maureen Fleming
Stamford, CT

Spirit 80

I consider BYTE to be among the best computer magazines published today. However, one problem undermines your good editorial and journalistic intentions: your reviews, and those of other magazines, are simply not to be trusted.

I have a Mannesmann Tally Spirit 80 printer, and I have just finished reading Mark Welch's review (November 1984, page 335). Mr. Welch makes much of paper jamming but fails to point out two vital characteristics of the machine that prospective buyers need to know about.

First, the Spirit offers only elite type. Also, only its right tractor slides; the left one is fixed. Should you wish to run labels, you cannot run them in the center, but only at the left margin. For a word processor that normally starts text in column nine, the left margin default must be adjusted to zero.

Shel Kagan
Bristol, RI

The Tandy 2000

I read with pleasure the articles in BYTE concerning Tandy's computer products—particularly the review "The Tandy Model 2000" by Mark S. Jennings (December 1984, page 239). As an alternative to the IBM PC or PC XT, the Tandy 2000 is a truly exceptional machine. I would like to make some comments about Mr. Jennings's fine review.

Mr. Jennings does not adequately explain the speed advantage of the 80186 microprocessor. Simply stating that it has a higher clock rate is not enough—the 80186 was completely re-engineered and the microcode was overhauled. An 80186 running at 4.77 MHz (standard IBM speed) is almost twice as fast as the 8088. By almost doubling the clock rate from 4.77 to 8.0 MHz, the Tandy 2000 can operate as much as four times faster than the IBM PC; some operations are even faster. In addition, the 2000 is not hampered by transferring data from the processor to memory over an 8-bit data bus—it has a true 16-bit data bus.

I must take exception to the claim that the Model 2000 does not achieve overall increased performance. I agree that the greatest improvement is achieved when running a processor-intensive application; however, the corollary is not necessarily true. Disk-based applications run faster for two reasons: ability to use the 16-bit data path and a much faster disk drive than the Teac drives used in the IBM PC. Mr. Jennings states that there is no significant difference in disk I/O (input/output) speed, yet the published benchmark times indicate approximately a 50 percent improvement.

Mr. Jennings was not nearly critical enough concerning Tandy's manipulations of the basic input/output system (BIOS) for this machine. Fortunately, since his article was written, Tandy has released MS-DOS version 02.11.xx, which fixes many of these problems. Software that depends on the features normally available on the IBM PC now works correctly.

Several times, Mr. Jennings alludes to having to perform a two-step operation for formatting and copying a disk; Disk Copy on the IBM PC does both. He must have missed the COMPDUPE utility, which not only does both but also performs a verify and a disk byte-for-byte comparison.

Mr. Jennings correctly identifies an area that has pained us all: Color update on the monitor was terribly slow. The BIOS "error" that caused this has been corrected with the new release of MS-DOS. Also, Mr. Jennings is not entirely correct in saying that you cannot generate text in the color-graphics mode. *If* you are mixing text and graphics, this is true. If you want only color text, you can program the monochrome attribute ports (beginning with 0198 hexadecimal) to provide full-color attributes for your application at black-and-white speed. You can use this technique within BASIC by setting the screen into the black-and-white text mode with a SCREEN 0,0,0 statement and using Out to set the port values.

I find that the Format command does not have extra options; in fact, several options available on the IBM PC are missing. Specifically, the options for formatting a single-sided disk, formatting with eight sectors, and allocating system file space are not available. While the first two options are not really meaningful with the 96-tpi (tracks per inch) drives, the latter option is a loss. You cannot build a distribution disk with the space allocated for system files.

On the issue of software compatibility, I find that many generic MS-DOS programs will run with no changes. Unfortunately, most IBM PC programs go directly to the hardware or ROM (read-only memory) firmware to bypass the system's slow speed. This is particularly true in most BASIC applications and I find these most incompatible with the MS-DOS machines.

Mr. Jennings alludes to the generic nature of the software available through Tandy's Express Order Software. This is incorrect: Each package available through

(continued)

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this service is completely compatible with the 2000 and generally will not work with any other IBM-type machine. Most have been fine-tuned to make use of the 2000's superior capabilities and are hardware-specific.

Mr. Jennings comments that the 2000 must be able to read IBM disks to run the software. The 2000 can read any IBM-format disk, either single- or double-sided and either eight or nine sectors per track. Many of the software packages I have received are generic IBM PC/Model 2000 and come on single-sided disks compatible with PC-DOS 1.X or 2.X. Because of the narrow disk head required for 96 tpi, the 2000 cannot write understandable data to an IBM PC disk unless it has just been formatted.

JOHN B. HARRELL III
Washington, DC

In regard to the 2000's processor, my article mentions that the 80186 has a 16-bit data bus and that it has a number of functions on the chip rather than in separate chips as does the IBM PC's 8088. I don't know about any overhauls of microcode. In any case, I have run a large number of programs on both machines and have yet to see any program perform more than three times faster on the 2000.

The lead to the article clearly states that the 2000 has better overall performance than the IBM PC. I correctly state that increases in performance depend on the program. Programs that are processor-intensive will show the most improvement.

You overstate any disk-access speed advantage that the 2000 might have over the IBM PC. The Disk Access in BASIC benchmark is a poor benchmark to compare pure disk-access speed because a significant amount of time is spent by BASIC interpreting the code. Please note that the 2000 is actually 41 percent slower than the IBM PC in the 40K File Copy benchmark; this benchmark is a better measure of how quickly the computer can simply read and write to disk. It might be true that the 2000 is faster in seeking random data on disk; I don't know because I haven't seen any benchmarks. In any case, the average 2000 user is unlikely to notice improved disk performance over an IBM PC; my overall impression is that maybe it is a tad slower.

By the way, to my knowledge no IBM PC has come from the factory with Teac drives, although they are commonly fitted in the aftermarket. Tandon seems to be the most common IBM PC drive.

You are entirely correct about the COMPDUPE command. I knew about this command, but the benchmarks had been previously run by a BYTE staffer who did not know about it. This is the reason for the reference to separate commands at the bottom of the benchmark comparisons.

I think it is still correct to state that the 2000 cannot generate high-speed text in the color-graphics mode. The key point is that if you have a program that mixes color graphics and text on the same screen, you should be prepared for very slow text display.

It would have been more accurate if I had said that the Format command has different options rather than extra options. It does have one extra option (for setting skew and interleave factors) and it is missing several others. I agree that Tandy should have included the options for different disk formats.

When I stated that most of the programs available from the Express Order System were generic MS-DOS, I meant that most of them were fairly standard MS-DOS programs that the vendor could easily port over to the 2000. I did not mean to imply that they were somehow incompatible with the 2000. As to the comment that Express Order software will not work on an IBM-type machine, I think that this is usually due to copy-protection schemes and the fact that the 80-track 2000 disks can't be read by a standard IBM PC. None of the Express Order System programs that I have seen running seem to have any special fine-tuning.

Your clarification of the 2000's capabilities to read and write IBM PC disks matches my understanding. However, I think that the article is fairly clear already in this regard.

—MARK S. JENNINGS
Durham, NC

MacFORTH AND THE SIEVE

I wish to submit a correction to "The First Look at FORTH on the Mac" by Gregg Williams (December 1984, page A115). In table 1 you list the time for the Sieve of Eratosthenes in MacFORTH at 36.2 seconds. The FORTH text in listing 1 at left is from block 7 of FORTH blocks included with MacFORTH 1.1. If you load it, you'll find that it runs 10 iterations of the Sieve in 20 seconds.

I assume the times listed in table 1 are for one iteration with an array size of 8199.

DAVID R. McDONALD
Pittsburgh, PA

The Sieve program you sent does in fact run in 20 seconds. But you miss the point of a benchmark: to run the same code (as closely as possible) under different circumstances. If you had typed in the benchmark referenced in my article, your results would be close to mine. I retimed the benchmark and got times of 36.4 and 37.0. I hope this explains the difference you found.

—GREGG WILLIAMS
Senior Technical Editor

Listing 1: *Alternative Sieve benchmark for MacFORTH.*

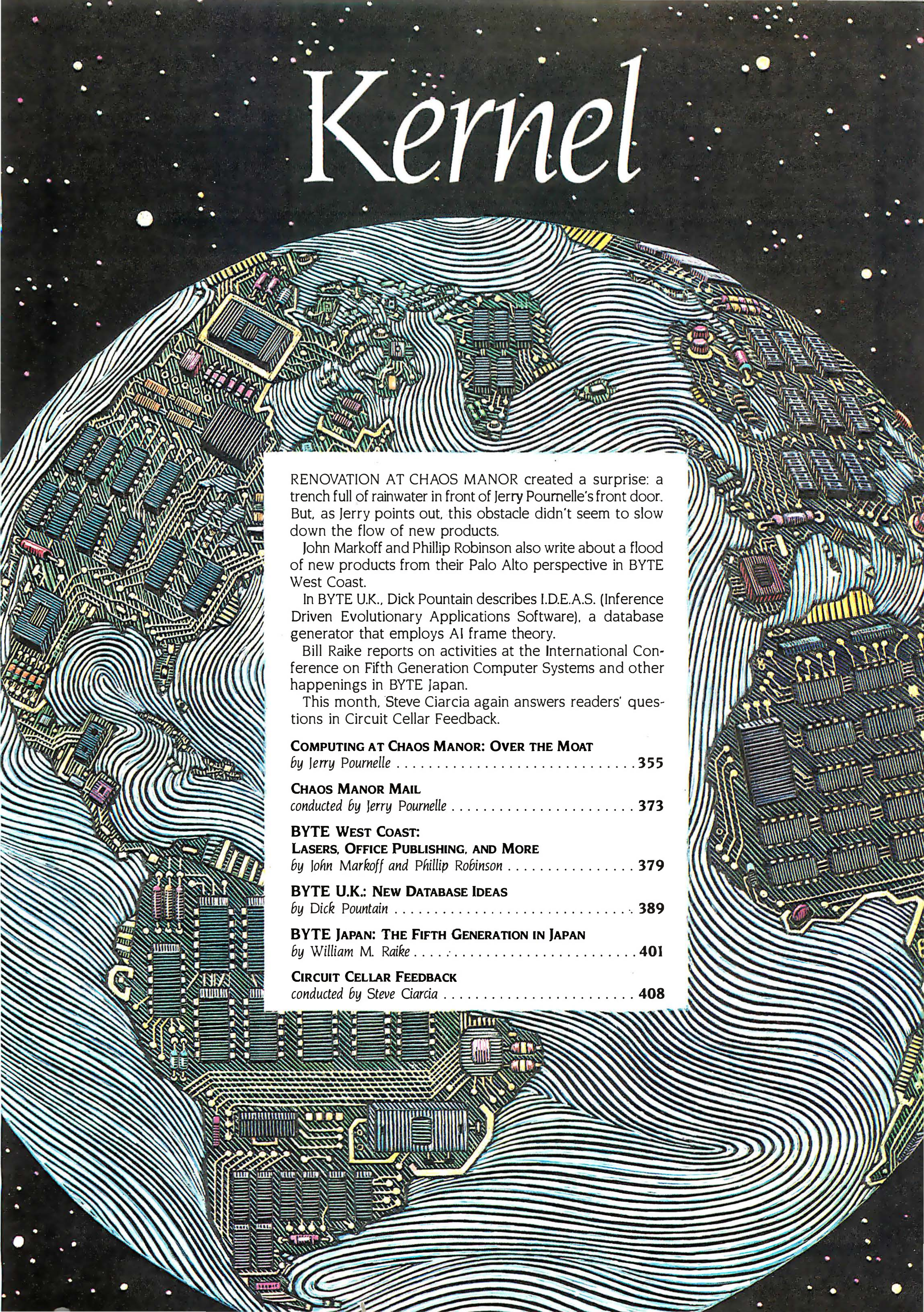
```
8192 constant size     create flags size allot

:primes  flags  size 0 1 fill ( empty array )
 0 ( prime counter )  size 0 ( range )
  do flags i+  c@
   if 3 i+  i+  dup i+  size < ( avoid known nonprimes)
      do 0 ic! dup        ( flick mod prime flags)
      + loop
    then      drop 1+ ( another prime )
   then
 loop
. ." primes ";

: 10times 1 sysbeep 10 0 do primes loop 1 sysbeep;
```

REVIEW FEEDBACK *is a column of readers' letters. We welcome responses that support or challenge* BYTE *reviews. Send letters to Review Feedback,* BYTE *Publications, POB 372, Hancock, NH 03449. Name and address must be on all letters.*

Kernel



RENOVATION AT CHAOS MANOR created a surprise: a trench full of rainwater in front of Jerry Pournelle's front door. But, as Jerry points out, this obstacle didn't seem to slow down the flow of new products.

John Markoff and Phillip Robinson also write about a flood of new products from their Palo Alto perspective in BYTE West Coast.

In BYTE U.K., Dick Pountain describes I.D.E.A.S. (Inference Driven Evolutionary Applications Software), a database generator that employs AI frame theory.

Bill Raike reports on activities at the International Conference on Fifth Generation Computer Systems and other happenings in BYTE Japan.

This month, Steve Ciarcia again answers readers' questions in Circuit Cellar Feedback.



C·O·M·P·U·T·I·N·G A·T C·H·A·O·S M·A·N·O·R

Over the Moat

BY JERRY POURNELLE

It's Christmastime at Chaos Manor, but you'd hardly notice it: there's a moat around my house. The City of Los Angeles has (finally!) come through with the building permit that lets us add a music room where the grapefruit tree used to be and a new library/office/workshop suite upstairs. The architects and contractors lost no time in breaking ground. My front door now opens on a four-foot trench. Of course, no sooner was the trench dug than we had the worst rainstorm in four years.

Amazingly, the mailman and other delivery people have braved the moat monsters, so there's plenty to write about.

ONCE MORE INTO THE BREACH

One of the first people to find his way across the moat was someone from Federal Express: three enormous boxes from CompuPro—and on a Saturday yet.

It seems I had an interesting failure. CompuPro has had a small number of hard-disk drives crash. It was rare, and fixable by reformatting; but it annoyed Dr. Godbout because his people couldn't make it happen in the engineering labs.

Then it happened to me. I'd backed up all the files—I'm *very* paranoid about that sort of thing—so all I really needed to do was reformat, but I thought I'd call CompuPro first, since I had a couple of other things to talk about. I described my symptoms and lamented that I'd have to reformat.

"Don't touch it!" Bill Godbout commanded.

"Eh?"

"We've been trying to get that bug to bite something we have a complete history of. Box up the whole system, disk drives, computer, the whole works, and ship it up. Don't even turn it on again."

"Well, okay—"

"I'll swap you a new—well, nearly new—system."

That was an offer I couldn't refuse, so up it went, and on Saturday, a week before Christmas, there arrived a new System 8/16—with some differences.

My old CompuPro System 8/16, the Golem, had Qume DT-8 8-inch floppy disks. I may be one of the last people in the world to use 8-inch floppies, but I prefer them; they're noisy, but they're *far* more reliable than 5¼-inch, and each floppy holds 1.1 megabytes, enough for a whole novel. My Qumes worked fine, and I'd just taken them out to Xerox for routine servicing—something I recommend you do every couple of years. For $60 (the minimum charge) they'll check the alignment, clean everything, and give you a complete report on any pending problems. Anyway, my disks had just returned when the CompuPro boxes arrived.

Qume no longer makes the DT-8 drives. CompuPro now sends half-height Mitsubishi double-sided double-density drives. They're just a little slower—4-millisecond (ms) stepping rate rather than the 3-ms rate of the Qumes—and you notice the difference, particularly when doing a Copy or Format operation. On the other hand, their major purpose is safety and backup, since the 45-megabyte hard disk is the major storage system for the 8/16.

The new Mitsubishi 8-inch floppies are incredibly quiet. CompuPro is using new and different fans, too; the result is that the new System 8/16, even with hard disk, makes less noise than Zeke II, the CompuPro Z80 (Qume 8-inch floppies, no hard disk) that I'm writing this on.

There were a couple of other surprises: instead of the three half-megabyte M-Drive/H RAM (random-access read/write memory) boards I used to have, there is now a single 2-megabyte RAM-disk board—and instead of two 5¼-inch disk drives, there's one 5¼-inch and one cartridge-tape backup. The cartridge will back up an incredible pile of files in a short time. If that seems vague, it's because I haven't read the specs; we simply turned it on and let fly, and as I write this it's backing up the main system track for my hard disk; the operation took about

(continued)

Jerry Pournelle holds a doctorate in psychology and is a science-fiction writer who also earns a comfortable living writing about computers present and future.

four minutes to store 2.1 megabytes of commands and data, a full 191 files.

Before I got the hard disk, I didn't think I needed one; now I can't imagine how I got along without it. I suspect the same will be true of the tape backup unit.

The new system came with yet another revision of the CP/M 8/16 BIOS (basic input/output system) software, which gets more sophisticated all the time. I guarantee you there will be at least one more change before you read this: just at the moment, if you try to get a "DIR L:" of the tape backup cartridge, the machine locks up so thoroughly that not even Reset will save it; we had to turn it off and back on again. *That's* going to be fixed. WRITE, the text editor I use, can automatically recover any text still in memory or on the RAM disk; but nothing unsaved will survive power-down.

Understand, there is software for getting the tape's directory; and I don't expect it to take them long to come up with a way to recover from "DIR L:". . .

NAMES, NAMES, NAMES

CompuPro has a problem: every now and again someone looks up the company's financial rating and mistakenly finds the entry for CompuCorp. CompuCorp is almost out of business and didn't do very well in the last year it got rated. CompuPro has actually lost sales because of this. The telephone receptionist is also getting weary of calls for "CompuPoo."

Thus began the great name hunt. CompuPro engaged consultants and did market research. Eventually they selected a name and kept it secret until they completed all the legal work to protect the trademark.

"It used to be," Bill Godbout said, "that you'd consult soothsayers and examine chicken entrails before undertaking something new like getting married or changing the company name."

"You're doing both—"

"Yes, and now you consult lawyers. They told me I'd be crazy to marry this year. Something about taxes. Next year. They've also approved tell-

ing you the new name. CompuPro is now Viasyn."

"Viasyn?" I asked. I didn't say it sounded like a medicine. "Why?"

"Everyone can spell it. You studied Latin. Via for way, syn for synthesis. . ."

CompuPro began as CompuKit back in the days when kit sales were usual in the micro business. (Ezekial, my first friend who happened to be a Z80, began life as Cromemco kits.) When Godbout began to sell assembled and tested gear, the company name was changed to reflect that.

"Why not Godbout Computers?" I asked.

"Market research says some customers think it's blasphemous."

"It's your name—"

"Yeah, I know. Anyway, it's Viasyn."

Oh, well. I suppose I'll get used to it.

Meanwhile, I suppose I must have collected, over the years, about a dozen letters complaining about my practice of naming my machines. Some readers are mildly annoyed, particularly if they tuned in late and can't figure out which machine I'm writing about—a legitimate complaint, and I'll try to do better in future.

Others are actually furious. One poison-pen letter—unsigned, of course—invited me to do obscene things with Adeline and dared me to print the letter.

My new 8/16 hasn't told me its name yet. I expect I'll learn pretty soon.

WHO CARES?

Suddenly everyone is talking about Framework vs. Symphony; which is better? It's the great software face-off, and every magazine I pick up has an article on the subject. The Ashton-Tate and Lotus PR people must have been working overtime to gin up all this interest.

As for me, I couldn't care less. I'm not likely to use either one. Or see below: if I do, I'm illegal.

THE COPY-PROTECTION PLAGUE

Both Symphony and Framework are copy-protected. I'm not about to entrust anything vital to a copy-pro-

(continued)

CHAOS MANOR

tected program, since, if I do, sure as anything the master disk will get lunched just after 5:00 p.m. on the Friday prior to April 15th.

I'm not familiar with Symphony's scheme; for some reason, I don't at the moment have a copy. I do have Ashton-Tate's new programs: Framework and dBASE III. They both use the Prolok copy-protection system. The company that provides it is the Vault Corporation, which is owned in part by Ashton-Tate.

The dBASE III documents come with an errata sheet that tells you: "You have been provided with two original system diskettes in your dBASE III package. Your SYSTEM diskette and its backup are not identical to each other. Each diskette has a unique identity just like a human fingerprint. Therefore, a backup copy from *one original* diskette will not boot up a copy you make of the *other original* SYSTEM diskette.

"When you boot up your system, be sure that you are using the same original diskette from which you made your backup copy."

There's also a warning: "Never use the DISKCOPY command to copy the dBASE III files to the new diskettes; use the COPY command instead. Use of DISKCOPY will result in permanent damage to your master diskette."

It does, too. You are urged by Ashton-Tate to make a "backup" copy of your dBASE III system disk; you can then use the "backup" for everything, except that when you start up dBASE III you have to have the original system disk in Drive B until the program is satisfied. If you use Diskcopy to copy the original system disk, then when you try to invoke the program your efforts are met with the message "unauthorized copy," and failure—even though you're using the original system disk. I'm not sure how Ashton-Tate's people have managed that result; one would think that a Copy utility couldn't be induced to *write* onto a source disk—but apparently they've done it.

This makes me wonder: presumably they've come up with some way to alter the Diskcopy utility; do they then

restore it when they're done mucking about with it? Or have they some crazy file that ought not be copied, and copying it moves it to a different location? I suppose I could figure out how they do it, but I can't make myself care enough.

Incidentally, a number of sources tell me that in PC-DOS the Copy utility is much more reliable than Diskcopy. Again, I don't know why. I find some of the "features" of PC-DOS incomprehensible anyway, and I've never understood why they don't have an obvious equivalent of CP/M's SYSGEN utility, which puts the operating system onto otherwise blank disks.

In any event, the copy-protection nonsense has kept me from experimenting with either Framework or dBASE III. One of these days, I'll get a Copy utility that will let me make backups and put dBASE III on a hard disk, after which I'll take it seriously, or else I'll get around to installing demons to defeat the Prolok scheme.

A demon is a small program that sits in high memory, watches what the Prolok scheme wants, remembers it, and later intercepts the Prolok disk calls to give Prolok what it wants to hear. Demons are not particularly hard to write, and they'll do a good job on many copy-protection schemes.

Until I get the copy protection defeated, though, those programs go back on the shelf; I'll review them some time when things are slow.

FASCINATING

One of my correspondents tells me that Prolok works in mysterious ways. It tries to conceal itself: 99 percent of the Prolok code doesn't exist until the program is loaded and running, at which time it goes through a complex process of decryption that's designed to be difficult to trace.

My correspondent, using PC Trace hardware, was able to follow what was going on—and discovered that Prolok has pulled in about 700 bytes, nearly 10 percent, of the IBM PC's ROM (read-only memory) BIOS code pertaining to disk-control functions.

Is this a copyright infringement? IBM has certainly taken action against other companies making free with its ROM BIOS code.

There's a more serious problem.

Ashton-Tate has sent a notice that it expects to have a copy-protection scheme that lets you put its copy-protected software onto your hard disk.

I know of no way to "protect" code on a hard disk without *reformatting* one or more sectors of that hard disk; or doing something equally drastic, like hiding deleted data address markers or some such. The scheme would involve doing "secret" things to your disk that only the program knows about.

Anyone who lets Ashton-Tate, or Vault, do that to their hard disk has got to be out of their ever-loving blue-eyed mind!

Actually, I'm not sure we wouldn't be better off if all users took the pledge: except for games, we will not buy copy-protected software. If a significant number of us do that, and we can get the other writers to push this stand, we can exorcise the copy-protection devil once and for all.

Even if you're not prepared to go that far, Lotus 1-2-3 plus Borland International's Sidekick (the $79.95 version that isn't copy-protected) has most of the features of Symphony and nearly as many as Framework; and if you already have Lotus 1-2-3, it's a lot cheaper.

UNLOCK IT

There's another solution to the copy-protection plague: programs that enable you to back up copy-protected disks. The best general-purpose backup utility we've found for the PC is System Backup from Norell Data Systems. Be sure to get the latest version; the utility changes with the times. However, *no* general-purpose Copy scheme will defeat all the different copy-protection schemes, and the latest version of System Backup will *not* copy dBASE III.

However, a number of Copy utilities, including one for dBASE III, have ap-

(continued)

peared on public-service electronic bulletin boards. If you have a modem, time, and patience, you can collect a fair number of them for free (except for the phone bills). You could also buy these from user groups, except that user groups put out their free software more or less in the chronological order they received it, so that you'll have to buy a number of disks in order to collect all the different copy-protection breakers. If you do buy a lot of user-group disks, be warned: an awful lot of "free" software doesn't work very well or do anything rationally useful.

Another alternative is to buy one of Workman's utility disks. Barry Workman collects public-domain software, tests it (but not extensively), edits the documents, and collects the stuff he thinks useful onto one disk. At last count he had six disks of CP/M utilities and at least one disk of MS-DOS stuff.

His CP/M Disk Six contains over 200K bytes of stuff. One program, Edfile, is worth the price of the whole lot. Edfile allows you to edit disk files; you can go in and change things, such as long, boring messages. (It is probably illegal, and certainly unethical, to use Edfile to remove copyright notices and serial numbers.) Edfile combines the best features of Spat and Duu (earlier disk-file editing programs) with some of the good features of DDT and Ed. I'd think anyone with an 8-bit (or 8/16) CP/M system would want this one.

Workman's MS-DOS Disk One contains all the copy-protection information he has found recently: some executable programs and some documentary files that suggest patches to remove copy protection. About half the programs on the disk are specific to the IBM PC and 100 percent compatibles; the rest are generic MS-DOS. Do understand that most of these programs are available free if you look hard enough for them.

A Z80 Modula-2

Workman has recently concluded an agreement whereby he will be dealer for a Zurich programmer who has developed a native-code Modula-2 compiler for Z80 CP/M machines.

It is a four-pass compiler: that is, it's pretty slow. At present it has no floating point, open arrays, or built-in error procedures (that is: when an error is detected, an error-message file has to be called in to tell you what happened). There's no procedure type—i.e., you cannot pass a procedure name as a parameter in a procedure call.

If you're not a programmer, you'll hate the manual; but all the information you really need is in there, if you know what to look for.

This is a programmer's Modula-2. Unless you're a fanatic, it's not something to learn the language from. However, it is Modula-2 for the Z80, and it does compile executable programs. The Zurich people are working on adding the floats, error procedures, and procedure types (in that order).

Recommended for hackers only.

S1 Exists

For over a year I've heard stories about the SI operating system. It is supposed to be totally portable, multitasking and multiuser, and better and friendlier than UNIX. It will contain the perfect programming language, enable but not require virtual memory and memory management, control any computer, right any wrong, dream the impossible dream . . .

SI was said to have been created by a Princeton faculty member and would be marketed by Multi Solutions Inc. (MSI) of Lawrenceville, New Jersey. Frankly, it sounded like a scam, and my views weren't changed when I found an MSI booth at a show last year and was told they didn't have a demonstration because their computer was lost on a truck or something. They've since told me they don't really like to ship computers around to shows because the machines often don't do well after transportation; but that wasn't what I heard at the time.

Also, MSI's literature seemed outrageous. They claim: "Only SI Vendors and Users will survive the next revolution." They offer a *huge* range of products, languages, and compilers that I am certain do not exist. Then I met one of the company's representatives. He's one of those chaps who gets too close to you and talks 50 miles a second. He promises anything, and you don't even get Arpege. After five minutes with him, I was sure it was all a scam. Just to be safe, I sent a message through the net asking if anyone had ever seen SI in operation. None had, but some had met the sales chap who so negatively impressed me; and everyone who had met him, including senior CompuPro officials, came to the same conclusion. S1 was vaporware and likely to remain so.

We were wrong. S1 exists.

The SI operating system was displayed in a small booth down at the far end of the main hall at COMDEX. The instant I came around I was seized; Robert Knight, formerly of Princeton's computer laboratories, is an old fan of my books and columns as well as the creator of S1, which he had running on an IBM Instruments CS9000 (the processor is a 68000);

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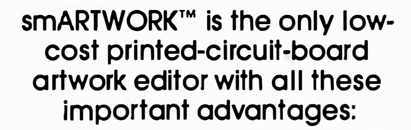
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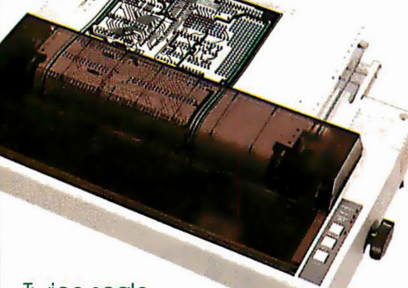
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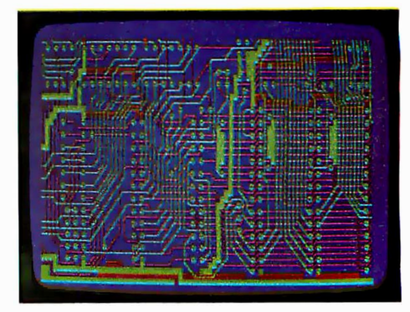


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that's a machine I'm not familiar with. There was also a Stride 440 (formerly Sage IV, also a 68000 machine), and I'm told they have a CompuPro 68000 back in New Jersey.

I got a demonstration. Of course, you can't see much at a show; there are constant interruptions. Thus, I still don't know a lot about SI. It certainly runs. It has features not present in CP/M 68000; features I'd very much like to have. It's said to be highly portable, and thus soon able to run on the 80286 and 32016 chips as well as the 68000. I'd like to see Knight get together with a good hardware house that produces machines running with a wide variety of processor chips and implement this properly. It just might be the wave of the future. Lord knows I'd be glad to learn one multitasking multiuser operating system that I could use on a lot of different machines. I'm not very keen on UNIX; at the moment, the up-and-coming operating system seems to be Concurrent DOS, and I don't know when they'll have that for 68000-based machines.

Knight claims a lot for SI. The MSI ad sheet gives prices for FORTRAN, C, Pascal, BASIC, etc., etc., but they didn't have them at COMDEX; MSI claims Pascal, FORTRAN, and C by the spring of 1985, but the only language they have so far is MSI's own SL, a kind of stripped-down Pascal. Until they have languages, SI isn't going anywhere.

I liked Robert Knight. He was perfectly honest with me on every question I asked, made no claims he wasn't ready to demonstrate, and thoroughly understood my skepticism. They're going to send a copy they claim will run on my CompuPro 68000 system. When I have it, we'll see. I don't do reviews until I have it running here at Chaos Manor.

The world is ready for another operating system.

Knight claims to have SI 90 percent finished. I suspect the rest will take longer to hack than he thinks. (Alex repeats an old motto: the first 90 percent of the work takes 50 percent of the time, and the last 10 percent takes the other 50 percent of the time.) However, Knight just might be able to bring it off. If he does, the potential is high. The world is obviously ready for another operating system; UNIX isn't going to do the job (it's a Thursday night so I can say that). Digital Research is in the doldrums. MS-DOS

(continued)

is boring. The Modula-2 operating system is exciting, but it's taking forever to get the operating system (as opposed to the language) implemented on anything but Lilith (a machine designed especially to run Modula-2). Whether S1 can win market share is open to question, but the market is wide open for something portable that will support lots of languages.

I reached the MSI booth just as they were announcing a very large ($40 million or so) development deal with a Japanese software consortium; that surely ought to be enough to keep Knight and his former student John Little working until they get things perfected, and it shows that some big-money people have confidence in them. Meanwhile, they're supposed to send me a copy, and Knight is working on a Modula-2 compiler to run under S1. I'm not holding my breath until MSI delivers, but I wish Knight well.

THE NETWORK JUNGLE

If you want computers to talk to each other, you could have problems because there are so many different networking systems. Corvus has Omninet. NCR bought the Corvus Omninet chip set, but of course its PC-to-PC net isn't compatible with Corvus Omninet. Corvus's network for Macintoshes won't talk to regular Omninet, although a planned higher-price adapter is coming Real Soon Now.

Meanwhile, CompuPro—oops, Viasyn—has opted for Datapoint's Arcnet. AT&T has a PC-to-PC-to-mini-to-mainframe network system developed largely by Locus of Santa Monica. Ethernet strides along, although the $1000 per connection hobbles it a bit. IBM has a local-area network that isn't *really* a network at all, but promises two more nets—details not clear to me—within two years.

If there's anything like a hardware standard developing out there, I haven't seen it. The only networking system I have any familiarity with at all is Corvus's; that really *will* let you network Apples and IBM PCs, and in theory you could also network S-100 systems like CompuPro, except that Corvus has stopped making and supporting the S-100 network card.

Viasyn makes very good use of Arcnet; I've seen as many as five different kinds of CompuPro systems, with a total of 16 different computers, networked in a very smooth system for shifting files and programs back and forth.

The moral of the story is simple. Unless you're a guru (in which case you don't need my advice), don't get involved in networking until you have to. If you need to network some systems, try hard to stay with one kind

(continued)

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of net and one brand of computer; if you have to connect a number of different kinds of machines, gulp hard and hire an expert.

THE GREAT SOFTWARE PURGE

They haven't begun tearing off the top of my house, but they'll start when the rain stops. That means the attic must be emptied. Which means grief. I've lived here in Chaos Manor for 20 years, and it's a *big* house. Whenever we accumulated too much junk, I would go up and floor another section of the attic, briefly creating lots and lots of room; but eventually that would fill and I'd have it to do again.

Last time there was nothing left to floor. We have managed to fill 2500 square feet to a depth of three to four feet with every conceivable kind of stuff from wedding pictures to old textbooks to unpublished manuscripts to research notes on articles and books I wrote a dozen years ago. To make it worse, the downstairs is now filled with more stuff that would have been put in the attic if there were any room for it.

It all has to go somewhere else.

Fortunately, I have a small pickup truck, and it doesn't cost that much to rent a large (20 by 30) public storage locker; a couple of frantic weekends filled the local school's paper drive bins and half-filled the locker; and then came the moment of truth.

Software flows in here like a river. Understand, I'm not complaining. I'd have nothing to write about without it, and I'm still excited when I open a package with something new and neat and different in it. Moreover, I feel some obligation to the people who sent it, particularly to the small outfits that can't afford advertising. When software first comes in, I try to figure out if it does anything interesting. More on that in a moment; but the bottom line is that if it doesn't look particularly interesting it goes into a holding file that tends to work like a first-in/last-out queue. It's supposed to be first-in/first-out, and it *is* as long as there's shelf space available; but eventually the shelves fill, the piles start, and we never reach the bottom of the pile.

Clearly, what's needed is more software shelf space—so I made some. Ruthlessly, I went through the Great Software Dumps: shelves, piles, everywhere. If it's dated prior to the spring of 1984 and I don't use it, it went. That wasn't universally true. I found a few things that looked sufficiently interesting to warrant keeping; but the rest went. The disks were stripped out and thrown into a box with a large magnet, and the documents were

(continued)

bagged for the paper drive. The hundreds of disks that are involved will eventually be bulk-erased and donated to a school.

Understand, I didn't *like* doing this. Some of the stuff was nothing more than early versions and presented no problems—how many copies of WordStar 1.6 do you really need, anyway? There were programs dating back to 1979 in there. Some was from companies no longer in business; those deserving their fate gave me no pains. Throwing out other stuff created emotional storms. There were programs that represented a lot of work and hope for small would-be publishers; people who need reviews because they can't afford to advertise. To them I apologize.

WHAT TO DO NOW

The upshot is that if you have software you want me to look at and you haven't sent anything since, say, July of 1984, you'd do well to send your latest copies. Whether I do anything with it will depend on a number of factors, many of them out of your control: if your program is Yet Another Example of a program I just received five versions of, you'd better have a snappy cover letter explaining why yours is best.

If you have the address of Chaos Manor, you can try sending it here and hope the moat monsters don't get at it. Otherwise, send review materials to BYTE, but be *sure* to mark it to my attention; and understand that sending it to me does *not* get your software to the BYTE New Products Review Editor. You must send *two* copies, one to me, one to the editorial people, if you want to be considered for both my column and a review in the magazine. BYTE selects what will be reviewed in the rest of the book by rules unknown to me; one thing is certain, they don't consult me about what they choose. Once in a while the editors in Peterborough will direct my attention to something interesting that I haven't seen, but otherwise I don't consult them either.

BYTE returns unreviewed software. I'd go broke doing that, so I don't. If I like a program and it does something I need done, I'll use it until something better comes along. If I like it but don't have any need for that capability, I'll sometimes ask the publisher if I can send it along to someone who does have a need for it. Otherwise, it goes into The System, sometimes to emerge when I'm stuck for something to write about, sometimes to molder until the next Great Purge.

SO LONG HAS IT BEEN?

Before I get to what I think is interesting software, I need to attack a complaint.

(continued)

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I have several—well, no more than four—recent letters taking me to task for concentrating on big, expensive machines to the neglect of smaller and more affordable ones. "You're too snooty to write about Kaypro, which must be beneath your notice," one letter says. Another reader believes I ignore CP/M systems, "which are really the machines for 'the rest of us' who can't afford the Macintosh." I haven't, he says, reviewed a new CP/M program for years.

My first reaction was a smile, but then I looked back through recent columns, and by gollies I have tended to write mostly about Mac, and my CompuPro (oops, Viasyn) 8/16, and the Sage (oops, Stride Micro) 68000 systems. Not exclusively, but I suppose a CP/M enthusiast could accuse me of neglecting 8080 and Z80 stuff. That's ironic; it was only a few years ago that *InfoWorld* and other computer magazines were quoting me as having "pronounced CP/M the standard for the micro industry"; while nearly all the people associated with Kaypro credit me as having given a big sales boost to their "Chevrolet" (I compared the Osborne to the VW, Kaypro to the Chevrolet, and Otrona Attache to the BMW); while I am to this day one of the very few columnists in non-Atari magazines to review Vincent Cate's little Atari Connection that lets you run CP/M on an Atari 800; and I regularly recommend an Atari 800 (or 800-compatible machine), Rana disk drives, and Wico joystick as a good youngster's system they won't grow out of too fast.

It's true that I don't much care for the Commodore machines (even though there are, I guess, more of them than anything else except the doorstop Sinclair); but that's because I do a lot of writing, and I don't much care for *any* system that uses a television screen or otherwise displays fuzzy and shaky letters.

CP/M systems are a different matter. A good Z80 CP/M system can do an awful lot; indeed, I'm writing *this* on a Z80. My accounting system (which I wrote in Compiling CBASIC); The Word Plus, still the best spelling checker on the market bar none; WRITE, the word-processing program I use to create nearly everything I do from books to these columns to my business and personal correspondence; the logbook program, and the index program I use to organize my log; Calendar/1, which organizes my schedule; every one of these programs runs on an 8-bit CP/M machine.

There are many bargains in good CP/M machines, and the Kaypro, with its bundled software, is certainly one of them. Three writing partners: John F. Carr, Dean Ing, and Roland Green have recently started using Kaypro systems, and a fourth, David Gerrold, now writes a column for the Kaypro magazine *Profiles*. They're all quite happy. Norman Spinrad loves his Kaypro 10.

I've never had a Morrow, but I hear good things about it. Barry Workman is very fond of his Lobo. The Epson QX-10 remains overpriced, but it is probably the cheapest machine you can sit down and begin using with little to no instruction, and if you add SemiDisk's RAM-disk board to the QX-10 it takes a lot of the sting out of its slow disk operations. I still use the wonderful little Otrona Attache on trips, but, alas, the Otrona company seems to have made some serious mistakes. If they'd worked as hard to promote the Attache as the BMW of 8-bit systems and continued to add bundled software to their already impressive package of programs, they might well have made themselves a profitable niche.

When all is said and done, though, there *isn't* very much exciting new software being written for Z80 machines. The reason is easy enough to see. The Z80 has the inherent limitation that it cannot directly address more than 64K bytes of memory. You can come up with ways to get at more memory, but, alas, there never developed a *standard* way to do that; the result is that nearly everyone tried a different

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method, big-memory software developed for one kind of hardware wouldn't run on anything else, debugging was costly. The market base isn't large enough, not compared to the IBM PC or the Apple II (although many Apple IIs do a *splendid* job of running CP/M programs; it only requires the right hardware addition, something like an Applicard or the Digital Research Gold Card).

There's still some solid progress being made. Every now and then, really good CP/M programs appear. Some, like WRITE, are really excellent—but they're seldom marketed by big concerns willing to spend lots of money on promotion. Many CP/M programs hang around for a couple of years, some never to be seen again, others to reappear in the public domain.

CP/M systems are adequate for many purposes and will be for years; but, alas, the micro industry is moving toward new standards of adequacy that will, eventually, relegate 8-bit CP/M computers to low-cost entry-level systems—or relics, like my neighbor's 1957 Studebaker.

So What Is Interesting Software?

Just at the moment I'm in a dilemma.

I have yet to see any computer system whatever that I would rather sit in front of for days on end than Zeke II, my CompuPro letter-series Z80. The reason is simple. Zeke II doesn't have a terminal. Instead, he has a memory-mapped video board, one of the very last of the boards from the days of Lee Felsenstein and the Sol computer. His video output goes onto a 15-inch white-on-black Hitachi high-resolution monitor that sits about 30 inches from my schnoz. The letters are big enough to read from across the room.

The keyboard is an ancient Archive keyboard. Archive has so thoroughly vanished that I can't find even a forwarding address—but Larry Niven and I have about four spare copies of their Hall-effect keyboards (no switch contacts; the keys may last forever), and except for the new Wico Smartline keyboard with its wonderful trackball, I haven't seen any keyboard anywhere that I'd even consider trading the Archive for.

The text editor is WRITE, which works only under 8-bit CP/M. Again, I have nearly every text editor known to humanity, and I have never found one better for just wailing away when you want to create lots of text—which is, after all, what I do for a living. There are lots of better *programming* editors, including WordStar (sort of everyone's second-choice editor, isn't it?), WordMaster (nearly neglected by MicroPro), Superwriter, and the EMACS-like editors sold by Mark of the Unicorn; but for just turning out 10,000 words of text in a couple of days, I've never *heard* of anything better than WRITE.

All my printing, spelling checking, communications with BYTE (hurrah! the BYTEnet for authors seems reliable lately; we've had some problems with the local New Hampshire phone system), accounting, check writing, and such like are done on larger systems, particularly the new (not yet named) Viasyn 8/16.

> *There's solid progress being made: every now and then really good CP/M programs appear.*

WRITE will, of course, work on a System 8/16, and if need be I can probably hack up a BIOS that lets the Viasyn 8/16 or its companion Shirley (CompuPro 10, now I suppose the Viasyn 10) communicate through the VDM (video-display module) memory-map video board and the Archive keyboard. It wouldn't be easy. Maybe I can talk someone else into doing it. Failing that, I can keep Zeke II and use the new Viasyn networking system to connect up. Either way, I'll get to keep WRITE and my big screen.

Alas, that's no longer quite good enough.

It isn't that there's a better program for text creation than WRITE. It's that WRITE doesn't do a lot of the fancier things that technical books demand. The spelling checker is external; not

(continued)

I don't really care to be tied to the future of UNIX.

a fatal flaw, because Word Plus is fast, but minorly inconvenient. There's no good bibliography or footnote capability. The index capability that Peter has worked out is all right, but it is pretty slow and hard for me to use. There's no on-board sort facility, no calculation, no spreadsheet. No graphics and no graphs. No explicit outline (idea processor) system, although WRITE does have features that, coupled with 500K bytes of RAM disk, work about as well. WRITE is great for letters and manuscripts; it will do a fair job on documents, but not a superb one.

Worse, there's nothing like Sidekick on Zeke II, and I have just *got* to have that program before my little green telephone index completely disintegrates. Sidekick lets me keep notes on line, calculate, look up phone numbers—not all the word-mashing things I want to do, but some of them.

Meanwhile, Tony Pietsch's Viasyn S-100 PCompatible video board, which lets you fool the System 8/16 into thinking it's a 98 percent compatible PClone (and has a jack on the back into which you can plug the Wico Smartline keyboard) is now in engineering test; I'll probably have one about the time you read this. I'll also have, probably, an extremely fast 80286 processor running the system and Z80 slave (SPUZ) boards.

I've no trouble translating WRITE files into WordStar (or any other kind) of files; thus I can, for as long as I want, continue to use WRITE to create text, pass it to some other text editor, and do extensive word processing there. I'll hang on for a while. But I *am* looking for some generic solutions; something I can begin to learn in the expectation that my time won't be wasted. That may be one big integrated program—but I doubt it. More likely, it's going to be a whole set of small utilities.

UNIX, of course, has a whole set of such utilities built into the operating system. The UNIX editor is lousy, but how long will it take a good programmer to do the functional equivalent of WRITE in C? A long time, if it's done as cleverly as Tony Pietsch did it in 8080 assembler; he kept the code amazingly compact. However, the 8088 and upwards family of chips can directly address plenty of memory; there's no *need* to keep the code so small.

I don't really care to be tied to the future of UNIX.

We'll see. Anyway, that's some of what I find interesting just now. I suppose it will change one day. . .

WINDING DOWN

I'm fading fast. Roberta tells me she has the bug, and worse, so does the housekeeper. It promises to be an interesting week.

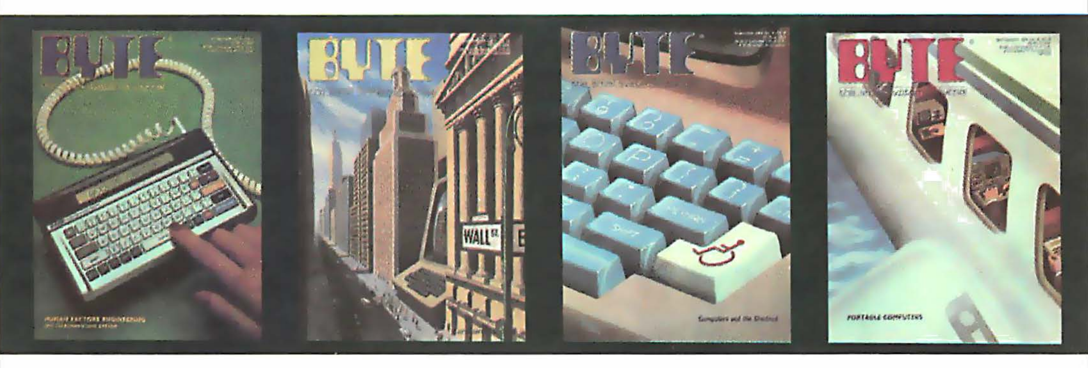
The books of the month have nothing to do with computers. I read *The Roman Empire* by Colin Wells (Stanford University Press). He disputes several of Gibbons's conclusions. Second, *The Great Siege, Malta 1565* by Ernle Bradford (Penguin). Finally, *Skywalking, The Life and Films of GEORGE LUCAS* by Dave Pollock. If you like the subjects, those are good books. Otherwise, forget it.

I've recently received three examples of the new Osborne Paperback Software Library, all for the PC and "close compatibles"; alas, no time even to open them. I was somewhat impressed with the packaging.

Now to collapse. ■

Jerry Pournelle welcomes readers' comments and opinions. Send a self-addressed, stamped envelope to Jerry Pournelle, c/o BYTE Publications, POB 372, Hancock, NH 03449. Please put your address on the letter as well as on the envelope. Due to the high volume of letters, Jerry cannot guarantee a personal reply.

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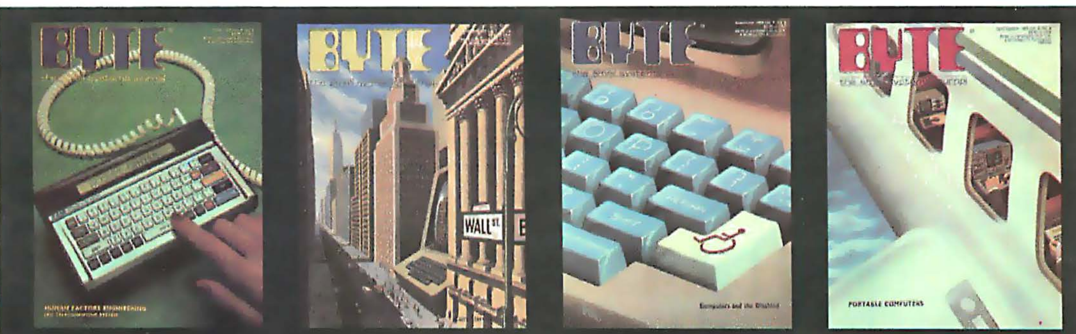
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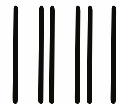
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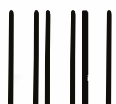


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I get a lot of letters, for which I thank you all. Please don't stop writing. However: I can't answer *all* the letters I receive, either in the column or individually. I can't even answer all the *interesting* letters. Moreover, even if I select a letter for a reply, there may not be room in BYTE. I have tried in past times to send a copy of the proposed reply to everyone whose letter I selected, whether or not a self-addressed, stamped envelope was enclosed.

I can't do that any longer. If you can't send postage, then you can't; but addressing envelopes is eating up too much time. Please?

BORLAND COMPLAINTS

Dear Jerry,

I am writing because, although I believe that the phenomenon represented by Turbo Pascal and Borland is all to the good, I don't think the euphoria spread by you, among others, is altogether justified. My complaints follow:

The installation program for Turbo Pascal is enough to drive people like myself with a graphics card and green screen blind. The program tries to write in color and succeeds only in being illegible. There appears to be no way to turn this off. The installation program is a nuisance to use anyway. If you want to change the twenty-third item, you have to go through the previous 22. The defaults on Borland's editor make you use WordStar-type controls and I detest WordStar, so the installation was a fairly lengthy and unpleasant procedure.

The spreadsheet supplied as a sample program is useless. There appears to be no way to change a cell into a formula cell, which is the whole point of a spreadsheet. There is certainly no way documented, and after reading the code for a half hour, I still could see no way. I suppose it is churlish to complain about a free program, but anyway it is worth no more than I paid for it.

Nowhere is it mentioned in the ads that Sidekick is supplied on a double-sided copy-protected disk. So my copy of it is useless to me. I can't use it, and I can't even take it to my office and copy it onto single-sided disks.

Why does Borland International add a $15 charge for foreign orders? And why won't they accept credit-card orders from them? Other software houses accept credit-card orders on foreign orders and either add a small charge for the extra postage or don't even bother to do that. For example, Laboratory Microsystems treats foreign customers exactly the same as domestic. I actually purchased my Borland programs from Micro-Way Inc., which added a small postage charge.

You have often written about absurd software licenses. There is none worse than Borland's, which claims it is "illegal" to use their software without returning the license agreement. I have no intention of returning it under that kind of threat. On the other hand, I do feel bound not to give copies away.

MICHAEL BARR
Montreal, Quebec, Canada

Well, the "license agreement" is a bit silly; I've commented before about the absurdity of trying to cover your flanks with both license and copyright, since the rights conflict. Oh, well.

I've had other outlanders complain about the extra $15; Philippe Kahn of Borland tells me that it costs him that much to fill out all the paperwork in order to export this high-tech item; and he can't afford to pay that himself. I doubt that makes you feel better, but I have no remedy.

I still think Turbo Pascal is one of the best bargains in the business.—Jerry

MAYBE IT WAS DRACULA

Dear Jerry,

Your comments about the origin of bug and *le cafard* in the October BYTE (page 330) were very interesting.

I've often heard the story about the dead moth in the relay. It could have happened! But I've also wondered why faulty computers couldn't be "debatted."

In late 1962 or early 1963 the IBM 7010 computer was undergoing engineering tests before being released to production. It was being run 24 hours a day, seven days a week, in an attempt to make it fail (it did, numerous times, and fixes were incorporated in the design). Although I was one of the engineers on the design team, fortunately I didn't draw late-shift test duty. Therefore, I was among those who chuckled one morning when we read in the logbook that the guys on the graveyard shift had spent some time dodging a bat flitting around the machine room. We figured they hadn't been getting enough sleep.

Their reputations were restored several weeks later when the machine was being dismantled for shipment to the manufacturing plant or someplace. Inside the power supply, where it had apparently been electrocuted, was the rapidly decomposing corpse of a bat.

WALLACE B. RILEY
San Francisco, CA

I have heard Grace Hopper tell the story of the first bug—they actually Scotch-taped the moth into the logbook—but I have never heard of bats in the computer before!

When I was an undergraduate, a small bat flew into my room and made a home inside an old Zenith mahogany high-arch vacuum-tube radio my landlady furnished with the room. He—I think he, although with bats it's hard to tell—lived there all winter, eating mostly milk and table scraps and sometimes flying out the window, presumably to hunt insects. Come spring he left me.

If my bat would live in a radio, I suppose another might find a computer quite cozy . . .—Jerry

MAC AND LISA

Dear Jerry,

I just have to add my two cents to the MacDebate. As a computer user who is a systems engineer, a systems programmer, and a student of psychology (in particular ergonomics), I feel well qualified to comment on the subject of user-friendliness. However, the problem with the Mac (and with Lisa for that matter) is mostly one of nomenclature.

(continued)

It would be stretching the common definition of computer to call a Wang word processor or an arcade video game a computer, but they sure do need to compute to do their jobs. So it is with Mac and Lisa; they compute, but they are not computers. Perhaps we should call them productivity-enhancement tools.

As a programmer and engineer, I expect a lot of my machines. I expect them to do exactly what I want in exactly the way I want them to. Give me a twelfth-generation computer that reads my mind and formats output to my liking and I'll be happy. Until then, I'll probably program my own applications when I have the time. That is the main reason I don't like Mac and Lisa. They are not programmable devices. They don't seem to be designed for that.

If one accepts that these instances of the class electronica are not computers, then many of the complaints about them become moot. After all, I don't often worry that my secretary's word processor doesn't run BASIC or that my phone-answering machine doesn't understand the CP/M operating system. There is still the issue of friendliness, however.

My hands-on use of these machines has been limited to a demo, but it is enough to convince me that Apple will *never* make a decent keyboard. I can hear them now, "But with the mouse. . . ." Unfortunately, my experience with Apple mice has convinced me that I can generalize my last comment to include all physical input devices. A touch-typist keeps track of eight fingers and two thumbs on 50 keys on a typewriter, more on a terminal or other keyboard device. Does Apple really think that two buttons and two fingers would be confusing? It would also be nice if the mouse had enough mass to let you know it was there; it's just too cheap for my taste.

That's all I have to say that I haven't seen in print already. Two things in parting. First, you might be interested to know that this is being composed on my HP 110 using Memomaker and will be printed at my office in the morning using an IBM PC XT as a print spooler; I love this machine! Second, I came in during the second act; could you print a Cast of Characters on occasion (e.g., the part of Zorro is played by a Z-100, etc.)? Thanks and keep up the good work; I always enjoy your column.

CHRISTOPHER NELSON
Croton-on-Hudson, NY

UNIX AND S-100

Dear Jerry,

It may seem to you that there is a future for the computer hobbyist, but I fear I'm destined to join the dinosaurs even before I get my machine built. Because I'm not rich, and actually *enjoy* configuring a system on a board-by-board basis, that's the way I'm buying it. My interests lean toward artificial intelligence, and I want a machine with some horsepower on which I can run UNIX. (Yes, I know, UNIX is easy for newcomers to get lost in; I'll be naming my machine Twilight Zone.) Now's the dilemma: CompuPro, Dual, and others make terrific 80286- and 68000-based boards; I've yet to find a manufacturer or dealer that will bundle UNIX with an S-100 processor board. I even went so far as to call Microsoft to hear about the fabled XENIX, only

(continued)

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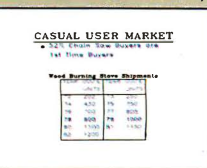
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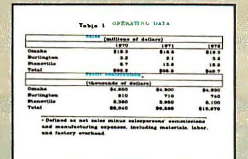
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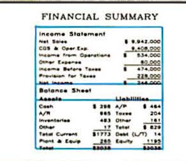
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to be told that it was sold to hardware manufacturers and vendors only and that I should contact a dealer with my needs. Sigh. I haven't found a dealer who will sell UNIX with a processor only.

I can't accept that my interests are so strict and narrow as to completely cut me out of the mainstream of the micro marketplace—there are just too many *whole* systems (68000 or 80286 running UNIX) available as business systems for those with the money to spend. What I can accept is that the market for do-it-yourself systems integrators is dwindling; people are buying more prepackaged systems and doing their own less. It is also far more lucrative to *sell* prepackaged systems and unbelievably easier to support the same.

It would be possible for me to finance the purchase of a PC AT and find UNIX for it, but I've no way of knowing what compromises were designed into it, nor would I know if the UNIX was just transported 8086 code or an honest rewrite to take advantage of the new features in the 80286. (My feelings on the PC are quite strong—the only thing IBM did was take a mediocre design and turn it into *the* standard for PCs. It could have done a *much* better job; I'd rather build my own.)

I could go on ad nauseam, but I'm sure you get the drift; we're a dying entity being replaced by the bundlers of PCs, Lotus and such. There *is* much being published on computing, but much on these *products*, rather than the internals of the machines themselves. It comes down to a definition of hobbyist.

MARK PILON
POB 105
Golden, CO 80402

You have quite a problem; I expect that Steve Ciarcia would be more help than I can be. Or maybe one of the readers can help.—Jerry

AWARD WINNER

Dear Jerry,

This gem accompanied the Pro-Digicalc spreadsheet program we recently bought. It's one of the more interesting software license provisions I've seen.

"You may not attempt to discern any of the software concepts or architecture from the software."

MICHAEL E. MACMILLAN

Ye gods: if the goal of Why Systems Inc. is to get people to ask "why?" on the theory that it will make their name memorable, they've succeeded. Herewith they receive my annual crumpled floppy award for the silliest license agreement yet. The rest of the agreement is standardly stupid; this provision is what wins for them.

Thanks.—Jerry

COMPUTER STORES

Dear Jerry,

Your sympathy for full-price computer store owners is misplaced. As long as computer stores hire teenage technobabblers, reject shoe salesmen, ham-handed repairmen, and other incompetents, and as long as it is cheaper and more cost-effective to get unassembled components in boxes via UPS than to lug

them home from a full-price computer store, they deserve to fail.

Other types of consumer businesses long ago developed into effective merchandisers. The result is that discounters, mail-order houses, and full-service retailers successfully coexist. When we pay full price for a stereo at DeLuxe Sound, it is because we receive value that Curbstone Discount does not offer, and it was worth the price difference. Often that difference is simply the knowledge that our needs were met by an effective product combination in an appropriate price range backed by a reputation of quality service, and that the transaction was accomplished treating us as intelligent human beings rather than suckers to be bilked.

I am a consumer who has too often found that Compu-Bilk and their ilk fail to provide the services they accuse the discount stores of not providing. Often the discount stores and mail-order houses provide a level of service that I earnestly wish I could get at my local full-price store! As a long-term computer professional, who for a variety of reasons shops in camouflage, I can usually tell when computer store salespeople are simply trying to extort. The average consumer feels this too, no doubt, in an undirected uneasiness that translates into the behavior your commentary discusses and store owners deplore.

When full-price computer stores make it clear to consumers what they get for their money, and if that something is of value to the consumer, the full-price computer stores will survive. Too many computer-savvy people think that consumer marketing is easy and they can make a killing selling them. Evidence of this attitude is your own lament in the same article about product pricing. Add the observation that the inexpensive Borland products were available only by mail order, in spite of strong marketing, until they became hot items and the verdict is guilty. If they fail to repent, they will continue to go out of business.

The halt, lame, and starving of the world need our sympathy and good works. Let's not waste them on the smug and greedy who don't!

RICHARD L. SWANSON
North Bend, WA

It depends on the store, of course; I've written my share of diatribes against the smooth-talking imbeciles who don't know a ROM from a cable designation. However, when good stores do hire knowledgeable salespeople and try to provide full service, I'd like to see them succeed. Perhaps you're correct; I may have exaggerated the problem. I hope so.—Jerry

MORE ON COPY PROTECTION

Dear Jerry,

People discussing the justifications of copy protection often compare software to books. Proponents of copy protection argue that book owners hardly expect unlimited copying privileges or expect free replacements for lost or destroyed books, so why should software owners expect these privileges? What they say has an element of truth but misses an important point: books are rugged, and floppy disks are fragile. If you were to leave a book on the dashboard of your car in the hot sun for four hours, then take it out, drive over it once or twice, then dribble a little coffee on it, you could still curl up with it that night and have yourself a good read. A floppy disk would hardly fare as well under such abuse. Furthermore, if a word or two of a book were somehow smudged or made illegible, the remaining information in the book would scarcely be compromised, but a garbled byte or a bad sector on a disk could render the whole disk unreadable or ruin the program. Copy protection may or may not be defensible, but I don't think that the justification can be based on a comparison between floppy disks and books.

GARTH WARE
Encinitas, CA

Well said. I agree. Thanks.—Jerry

WORDSTAR TIPS

Dear Jerry,

You have mentioned that WordStar's global reformat command is grossly slow. There is no explicit global reformat command in WordStar (that I know of), so I presume you are using ^Q^Q^B to repeat the ^B (paragraph reform) command until interrupted by an <ESC> (or other keystroke). This is indeed quite slow, but part of the reason is that ^Q^Q<key> pauses between each execution of <key> to allow the user to observe the effects so far and decide whether/when to interrupt the repetition. If there are many short paragraphs, ^Q^Q^B spends much more time pausing than reforming.

However, a digit keystroke (1–9) following ^Q^Q^B adjusts the duration of the pause. A "1" gives no perceptible pause and speeds global reformatting quite a bit. (^OH is also needed to prevent hyphen-help from stopping the reformatting for hyphenation. I have patched my WordStar working copies to default to hyphen-help off to avoid this.) Global reformatting is still not blindingly fast because of the screen rewrites after many ^Bs. But since WordStar can handle a large document in a single file, no operator attention is needed. So when I need a global reformat, I just take a break while the computer does what it's best at! If you haven't tried the speed adjustment on the ^Q^Q^B, you may be in for a pleasant surprise.

KIRK A. MATHEWS

Thanks for the tips. WordStar is a pretty good editor; at least, WordStar 3.3 with Orchid's PCturbo 186 board really zings. I still use WRITE on 8-bit for most of my work, but when I do need to use the PCturbo 186 I've actually got sort of fond of WordStar. Thanks.—Jerry ■

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FastFinder

BY JOHN MARKOFF AND PHILLIP ROBINSON

If you want to be "in," introduce something that uses both a microcomputer and the Canon laser-printer engine. That inexpensive, high-resolution, fast, and silent descendant of the copying machine is popping up everywhere. Last spring Hewlett-Packard introduced its LaserJet printer—based on the Canon engine. In January Apple unveiled the Macintosh Office (see our article "The Macintosh Office" in the February BYTE, page 120) and its LaserWriter printer—based on the Canon engine. In the meantime, several other companies have announced laser printers for the IBM Personal Computer (PC) market based on—you guessed it. Plenty of people are betting that the laser printer will take a huge bite out of the daisy-wheel market.

Another, more expensive, way to be "in" is to find an application for the Sun Microsystems workstation. As we mentioned in the January BYTE West Coast ("Light Touches," page 415), that powerful 68010-based microcomputer has impressive graphics, windows, and speed.

So what would be the ultimate "in"? Right again—combine the Canon laser printer and the Sun workstation. Interleaf's Office Publishing System (OPS-2000) and Technical Publishing System (TPS-2000) do just that. Interleaf, based in Cambridge, Massachusetts, is . . . Wait a minute. Did someone say, "Cambridge isn't West Coast?" Well, we anticipated some such opportunistic heckling, and we have some answers.

Much of the Interleaf publishing package comes from right here in Silicon Valley. Ideas and components derive from Xerox Corporation—particularly its famous Palo Alto Research Center (PARC). Alto and Star features, such as icons, windows, and object-action processes, are fundamental to the Interleaf software. And we weren't the only ones to notice; at the Interleaf system demonstration in Menlo Park, we heard a potential customer muttering, "This looks more like Xerox than Xerox." Some of the folks at Interleaf came from Kurzweil Computer Products back east (responsible for the famous reading machine), but there's even a connection there. Xerox bought Kurzweil. Finally, we're fascinated by the competition that is shaping up between the Star clones: both inexpensive machines like the Macintosh and expensive machines like these Interleaf systems.

Interleaf introduced the OPS-2000 system in the summer of 1984 and is now showing off the new, more powerful TPS-2000 system. The TPS-2000 is built around the same hardware as the OPS-2000 but it has improved software. It features new I/O (input/output) support: an optional optical scanner (to convert images into bit-map displays for editing and printing) and a phototypesetter interface. Either system lets you create text and graphics, combine them into documents, and print them on a laser printer.

In general, the idea behind both the Interleaf and Apple systems is that you won't have to take office documents outside the office to typeset them. The print quality from the laser is high enough that you can use its output for forms, reports, proposals, and manuals. (Besides, the printer can produce eight pages a minute.) The Sun workstation screen displays 75 dots per inch; the laser printer prints 300 dots per inch; and a phototypesetter produces 1000 dots per inch or more.

Does office publishing sound like a narrow, specialized field? Interleaf believes that office publishing is a billion-dollar industry that will grow to 8 billion dollars by 1988.

HARDWARE

The Sun workstation with the Sun 2 processor card runs the Interleaf shell (which is written in C) under Berkeley 4.2 UNIX. The shell has its own windows and doesn't let you run other applications concurrently. However, to run another program all you have to do is get back to UNIX. That's easy. In fact, even without any help, the system

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did it several times during the demonstration.

A three-button optical mouse is used to control most of the work on the 19-inch diagonal screen. The 900- by 1152-pixel screen yields the high (75 dots per inch) resolution and a high spoilage factor. What's spoilage? That's what you feel when you play with a superb, expensive machine like this and then have to go home to a bare-bones Kaypro.

The basic Sun workstation has 2 megabytes of RAM (random-access read/write memory) and ROM (read-only memory) and is accompanied by a 42-megabyte hard disk. If the two terminals you can attach to the 42-megabyte system aren't enough, buy the 130-megabyte disk; then you can attach as many as 15 terminals (if you can afford them). Each Sun workstation costs about $22,000. The OPS-2000 system with software, one workstation, printer driver, printer, and lots of support and instruction runs about $52,000. The scanner and scanned-image editing option costs $40,000. The digital-typesetter interface that sets type and produces camera-ready pages (supporting Monotype, Compugraphic, Autologic, and Information International typesetters) begins at $7500, the laser printer at $14,500.

Although Interleaf specializes in turnkey systems, the company is happy to discuss other deals—particularly if you already have a Sun workstation. If you want to use other computers, a simplified version of the OPS-2000 software is available now for Apollo systems—both the bit-slice and the 68000 versions. According to Interleaf software engineer Roch Skelton, ports to other systems are in the works.

The Imagen printer controller accepts fonts, bit maps, and ASCII (American Standard Code for Information Interchange) characters from the Sun workstation and *rasterizes* them. That is, it converts them into one big bit map for the Canon printer. Skelton notes that the rasterization software is Imagen's, but "We're helping them develop and fix their software." Imagen, by the way, is another one of the many companies populated by refugees from Xerox.

The Imagen printer-controller box has about the same volume as the Canon printer but is shorter and longer. Inside it is a 68000-based computer and 1.25 megabytes of memory. It also interfaces with the new Ricoh Corporation laser-printer engine. Its specifications are about equivalent to the Canon's, but, according to Interleaf, Ricoh has a stronger market in Europe.

By summer 1985 we should see laser printers capable of 600- to 800-dot-per-inch resolution. Interleaf is using such a printer with its own systems. This resolution approaches that

at the low end of typesetting. Interleaf will use a Toshiba printer engine with a Dataproducts controller to produce up to 24 pages a minute by next year. Interleaf hopes to create its own printer controller, which it calls RIP, for Rasterizing Image Processor.

SOFTWARE

Both the OPS-2000 and the TPS-2000 accept text from IBM PCs, Wang word processors, WordStar, Scribe, Nroff, and Troff—in fact, just about any ASCII file. Interleaf has filter programs to massage text that doesn't arrive in usable condition. Documents within the Interleaf systems are saved as standard UNIX files and you can transfer them between UNIX systems using standard utilities. The attributes that dictate the document's format are stored in a separate *dot file*. Except for a leading period, the dot file has the same name as the ASCII file. The OPS-2000 also directly accepts Lotus 1-2-3 spreadsheet data via a special RS-232C connection and a communications program that are available from Interleaf.

The fonts occupy 2.5 megabytes of disk space and the software occupies another 5 megabytes. The basic OPS-2000 shell takes up 600K bytes of the internal memory; having it in RAM speeds up document formatting. Even 2.5 megabytes of font storage contains only two fonts: a serif style (called Classic) and a sans-serif style (Modern). And the font sizes only go up to 24 point. Future versions will include 36- and 72-point sizes, light and condensed fonts, and other improvements.

Interleaf claims to be ready to support color when the workstation and printer hardware can handle it. "It's an evolving product" was a sentence we heard repeatedly. Skelton kept referring to the many new features in the March software release—more fonts, new paint capacities, section numbering, document indexing, etc.

The OPS-2000 discriminates between four types of graphics: business graphics (charts and graphs that the OPS-2000 software produces), scanned images (input through the special optical scanner that Interleaf sells), simple created graphics (boxes, lines, circles), and Calcomp 960 plotter graphics. Eventually, all of these will be interchangeable. However, the older version of the OPS-2000 has limitations for each. For example, scanned images can't be rotated and Calcomp 960 plots can't be *filled* because the software doesn't recognize the edges of the figures as continuous. The Adobe PostScript/Apple LaserWriter combination and the Interleaf OPS-2000 are clearly different in that the former can print anything you draw on the screen, the latter cannot.

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The OPS-2000 includes clip art and a wish book. The clip art is a library of diagrams, mathematical symbols, and graphics that you can use directly or modify. The wish book contains examples of 50 types of business charts that the system can use as a model for your own graphics. You can add your own chart types to it.

The OPS-2000 lets you size, duplicate, move, fill, and rotate images. It uses the same cut-and-paste scheme that the Macintosh employs. The TPS-2000 adds features for typesetting such as multiple-column capability and scaling. Two of the fonts are vector fonts that can be rotated and sized along with other diagramming objects. Scanned images can be positioned, cropped, sized, rotated, shaded, blended, merged, airbrushed, silhouetted, textured, or overlaid with text.

The Interleaf system uses a series of fixed and floating rectangular windows called frames. [*Editor's note: These frames should not be confused with artificial-intelligence frames.*] A *fixed* frame is tied to a particular spot in the text stream and moves on the page when the text is edited. A *floating* frame is tied to a particular location on the page called an anchor. This frame stays put and the text flows around it. The user interface depends on object-action processes: you select an object—text or graphics—and use the pop-up menus to manipulate it.

We're Not Done Yet

Will Interleaf's expensive, powerful system win the hearts of office publishers? You can have many but not all of its *special* features for much less money in the Apple Macintosh Office. To some extent, you can even duplicate the scanner with peripherals such as the Thunderware image digitizer described in our February BYTE West Coast ("What's Next?" page 371). Still, for now the Interleaf systems are more complete and much faster than anything based on the Mac. What happens when the Macintosh gets some publishing software more powerful than MacWrite? We'll wrestle with that question in next month's BYTE West Coast when we look at Aldus Corporation's electronic paste-up and composition program, PageMaker.

FastFinder: A Macintosh Programmers' Workshop

The Apple Macintosh software architecture is based on the concept of a visual shell that insulates you from many of the nuts and bolts of a traditional operating system. Most people are now familiar with the widely copied, mouse-driven, bit-mapped desktop display that Apple claims offers "radical ease of use." However, much of the criticism of the Macin-

(continued)

tosh design has focused on this visual interface. While it protects you from operating-system complexities, it also strips away some powerful features, such as batch operations and macros.

All of this might be forgiven if the visual shell were faster than it is; however, to date, lack of speed appears to be the Macintosh Achilles' heel. If the Macintosh has a design flaw, it is that the goal of user/computer interactivity is often thwarted by performance bottlenecks that force long waits for certain operations.

The Finder, a system program that controls the Macintosh desktop, mediates user interaction with the system and displays a visual, icon-based version of files and folders. The Finder *launches* a program when you point at it and double-click the mouse button. Its lack of speed comes, in part, from not being coresident; each time you exit an application, the Finder must be reloaded. It also spends a lot of time recalculating the location of documents on the desktop each time it displays. These combine to make the process of switching between applications cumbersome on the Macintosh.

Although Apple hasn't chosen to improve the Finder yet, there is now an alternative. Michael Lehman has developed FastFinder, another desktop for the Macintosh, which is text-oriented rather than graphics- or icon-oriented. Lehman is a software developer and the author of Pascal/MT+. His company, MT Microsystems, was purchased a number of years ago by Digital Research. Lehman worked there for three years until leaving last year to once again form his own company, Tardis Software.

Lehman wrote FastFinder out of frustration with the Finder while developing an application for the Macintosh.

Written in Mac C from Consulair Corporation, FastFinder includes some Mac C run-time libraries that Lehman has specially *tweaked*. It offers a standard Macintosh display with a series of windows and a menu bar across the top of the screen. Within each window you have access to a line-oriented command processor that you can access either by typing at the keyboard or by selecting options from the pull-down menus.

Although Lehman refers to FastFinder as an "expert's alternative" and includes with it a number of features oriented toward Macintosh programmers who want to automatically link operations in the process of program development, it also should appeal to anyone who wants a faster Macintosh. Lehman claims that FastFinder runs "up to five times faster" than Apple's Finder and that it adds a number of features such as fast disk ejection. FastFinder's greater speed is evident in its ability to both load programs slightly faster and reload several times faster after exiting a program. Additionally, Lehman will soon release a desk accessory called FastLauncher to be installed with FastFinder. FastLauncher lets you select a new program while still operating in another one and then lets you go directly to the new program without returning to the desktop.

To use FastFinder you must do without the Macintosh graphical interface. (Lehman says he has a graphical version in mind.) FastFinder directories appear as text-only in a list of those files that you can scroll in their individual windows. You can install programs as special menu items and then launch them by dragging the mouse down and clicking on menus; however, you must also give up the Macintosh document and folder metaphor for organizing files.

If you are doing program development on the Macintosh, FastFinder has a series of UNIX-like utilities that you can access from the menu or command line. Many of these commands are already available as small utility programs for the Macintosh; however, FastFinder makes them easier to use because you don't have to leave the desktop to use them. Others, such as combine, compare, and list, are not currently available.

FastFinder includes a scripting capability that you can call with the do command. The do command executes a series of FastFinder commands that can be created with a text editor or a special record command and then stored in a text file. FastFinder can also link applications under script control.

Now that he has finished FastFinder, Lehman is writing a Macintosh application generator for novice and expert programmers. ■

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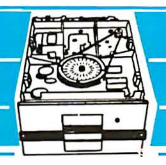
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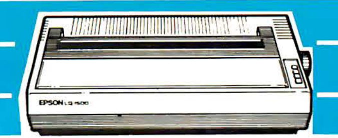
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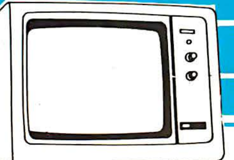
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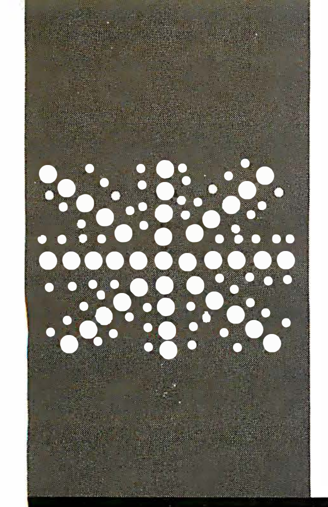
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New Database Ideas

Frame theory used in a database generator

BY DICK POUNTAIN

All the research done so far in artificial intelligence (AI) points to the conclusion that if computers are to even begin to approach the capabilities of the human brain, they must store and retrieve huge amounts of context data. In humans this data appears to be a combination of innate and learned knowledge.

No one seriously suggests any longer that an intelligent computer can be realized purely algorithmically. Rather, the process will be a long and painstaking one that involves stuffing more and more facts into a machine. Some of these will be facts about the world we live in, while others will be rules about those facts. In short, the emphasis will be at least as much on smart data storage and retrieval as it is on computation and calculation.

These ruminations are prompted by a recent encounter with I.D.E.A.S. (Inference Driven Evolutionary Applications Software) from AI Software Ltd., a commercial database-generator package that uses a novel approach influenced by Marvin Minsky's theory of frames. It runs on mainframes, minicomputers, and microcomputers such as the Sage IV and the TDI Pinnacle. You can use it to create accounting, payroll, costing, stock control, and other commercial applications that use a shared database.

FRAMES

In the article "Database Types" by Rich Krajewski (October 1984 BYTE, page 137) there is a summary of six main categories of existing database software. Here's a recap of the three main types: A simple *file-management system* enables you to build files out of records. Records are self-contained parcels of data structured into fields that are the same for every record. In an address-book application each record would contain a complete name and address, with fields called Name, Street, City, and Phone Number, for example. However, information held in different files is totally separated and can't be related.

At a higher level of sophistication are the *relational* and *hierarchical* types. In a relational database, you can relate records from different files assuming that they have at least one field in common. If you have one file of customer names and addresses and another file with their names and credit balances, you can combine the information using Name as the common field and extract records containing name, address, and credit balance for a particular person. In other words, the links between different sets of data are made via the contents of the files, and you can define new relations while you're using the database by using the command JOIN.

In a hierarchical database, you can predefine a tree-like structure of relationships between different files that doesn't depend at all on the record contents. For instance, a file called Customers could *own* subfiles called Address and Credit Balance. A more complex form of this database allows any file to own any other, so the result looks more like a network than a simple tree.

The I.D.E.A.S. program doesn't fit comfortably into any of these categories. Data is related neither by the contents of data fields nor by a predefined file structure, but by a system of coordinates abstracted from the structure of the real world.

I.D.E.A.S. was conceived about five years ago by a group of commercial programmers who happened upon Minsky's 1974 paper "A Framework for Representing Knowledge," dealing with the AI problem of computer vision. Impressed by the methods expounded there, the group decided to try to set up such a framework for the world of commerce and manufacturing.

In a nutshell, Minsky's *frame* is a data structure for representing a state of affairs or an activity. The frame has *slots* that are filled with specific instances, while the frame itself represents the archetypal state. For example, a frame describing a house might have

(continued)

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Table 1: *The prime dimensions used by* I.D.E.A.S. *to distinguish one piece of data from another.*

1) Time. A date or time of day.
2) Financial. A relationship to the accounting system.
3) External trading. A relationship with someone or something *outside* the enterprise.
4) Batch identity. An identifier for a particular batch of products.
5) Commodity. An identifier of a particular product type.
6) Internal organization. An identifier of a particular department or other subgroup *inside* the enterprise.
7) Personnel. The people involved.

slots called Living Room, Bathroom, Kitchen, Garage, etc. The contents of these slots might also be frames; the Kitchen frame could have slots Stove, Sink, Waste Disposal, and Freezer. To describe a particular house you fill in these slots with specific makes of appliances and furniture. Equally important, slots can have default values, so partial descriptions can be allowed and reasonable guesses made in the absence of complete information. Groups of frames can share slots, thus relating different classes of objects (as in the relational database); as an example, an Office frame might share the slots Table and Chair with the House frame.

PRIME DIMENSIONS

The authors of I.D.E.A.S. studied their previous accounting, stock control, payroll, and other programs to see if they could create a frame that would describe all the various kinds of data used. Through trial and error they identified a set of seven *dimensions* that they claim effectively define any piece of data used in a commercial/manufacturing enterprise. *Define* in this sense means that a set (between one and seven) of these types (or dimensions) is sufficient to distinguish one piece of data from another. The prime dimensions are shown in table 1.

To see how this works let's look at some examples. You can uniquely define a product's list price using only the commodity dimension (the product code). However, if you have different price lists for different kinds of customers, you need to specify both the external and the commodity dimensions (customer name or code and product number). If prices change

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frequently, you might want to date price lists, adding the time dimension, too.

Take another example. The value of an item dispatched could involve the external (who is the customer?), financial (how is it accounted for?), commodity (what product?), batch id (what order number?), and time (what is the date of dispatch?) dimensions. In a large company the department (internal) could be relevant, too.

Prime elements are those data elements for which only one dimension is relevant (e.g., a customer code, a product code). They behave more or less like keys in a conventional database, but they are special because you can organize them into hierarchical sets. For example, Customer codes can be made a subset of County codes, which are themselves a subset of Region codes. So Fred Bloggs can be situated in Yorkshire, which is situated in Northern England. More than one superset can also exist; Customer code can come under Industry code as well, allowing Fred Bloggs to belong in Heavy Chemicals.

When you create a new data element (e.g., Value of Item) in the I.D.E.A.S. data dictionary, you must fill in a primitive frame that identifies which prime dimensions are relevant for this element. In addition you must specify whether the dimension is fixed—constant data that goes into the dictionary—or floating—data provided at run time. For instance, the name of the department that makes widgets is fixed (unless there's a major company reorganization), but the customer's name is floating (you want to search for customers at run time).

Once you define such a frame, then I.D.E.A.S. knows where to store that type of item. In other words, you can represent every different kind of data object by a point in seven-dimensional space, or if you prefer, you can map individual records into eight-dimensional space—the eighth being an implicit record number. In physical terms, I.D.E.A.S. uses a multitude of single-key indexed-sequential files to represent this multidimensional space, but these files are completely hidden; indeed, the concept of a filename doesn't exist in I.D.E.A.S. The advantage of this sort of organization is that relationships between data items follow automatically; only data items that share *at least* one prime dimension can be related at all, and the relationship is forged as soon as the items are defined.

When the database is in use, the slots in the frames are filled with real instances of customer names, product numbers, etc., just as the fields of a record would be in a more conventional database.

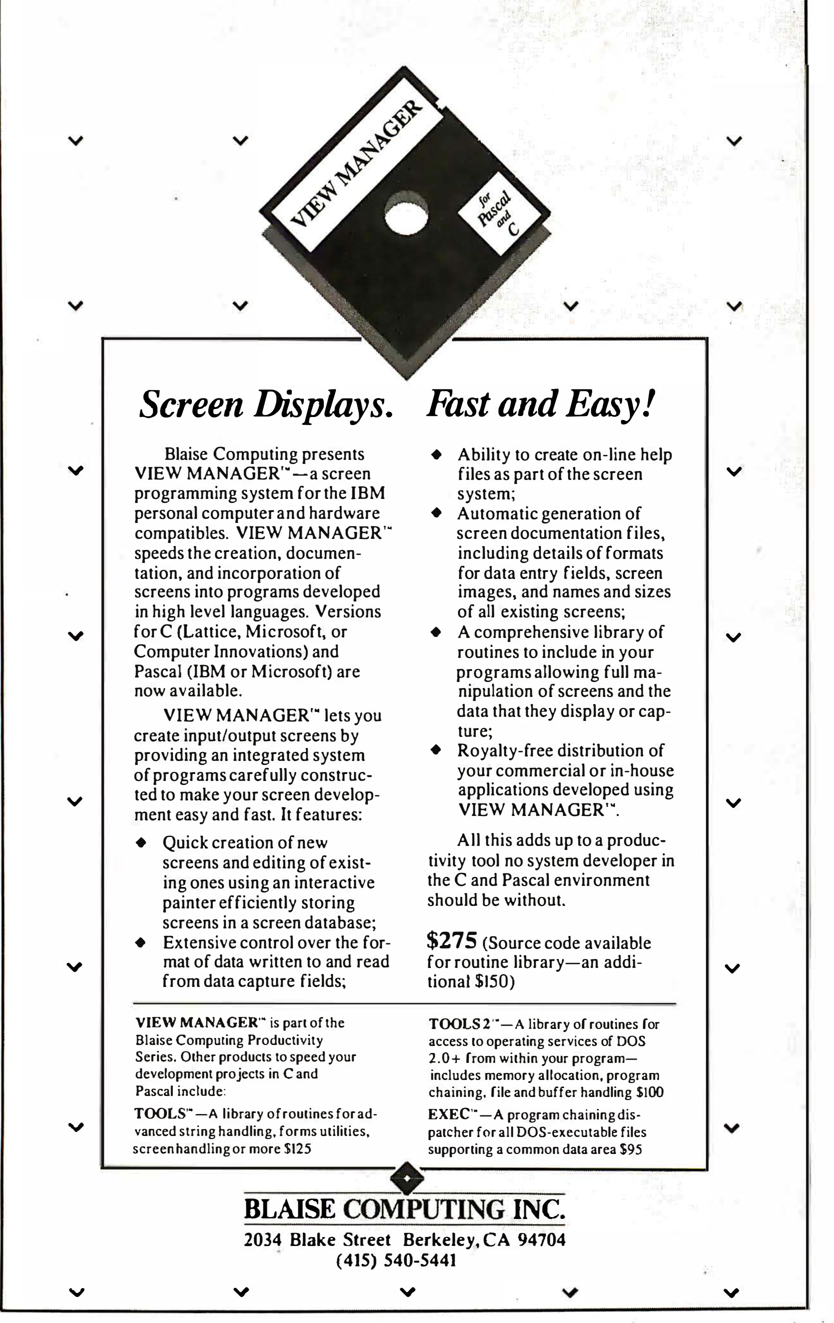
This approach seems to me to have

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tremendous virtues. The structure of the database is formed by factors relating to the real-world domain being dealt with, not by machine- or program-related constraints of the computer. Though I.D.E.A.S. was designed to reflect only the world of commerce and manufacturing, a different set of prime dimensions could easily adapt the concept to another domain. In fact, if you study the I.D.E.A.S. prime dimensions carefully, you'll find that, renamed to be more general in scope, they apply rather well to other activities already. Could a computer scientist prove theorems about the number of dimensions needed for a given domain, or is that to usurp the role of philosophy? How about a database manager called K.A.N.T.?



PROCEDURE FRAMES

If you want to actually do something with the data stored in I.D.E.A.S., you must define some elements called *procedural frames*. They are equivalent to programs written in a command language but are produced by an integral program generator after an interactive question-and-answer session.

To produce, for example, an invoicing or stock-control system, you need a collection of data elements and a collection of procedural frames to work on those elements. Typical procedures might be Add Customer Orders or Update Stock Levels. The primitive operations available for use in procedural frames are all prefixed by a $ sign and called $commands. They include commands for formatting input and output screens, repetition and branching, conditionals and subroutine calls—in fact all the elements you'd expect to find in a database command language.

The most important $commands are $LOCATE and $SCAN. These are the high-level instructions that actually traverse the complex network of database relationships and retrieve items for you. Let's say that we have defined a data element called Customer Order that requires a customer code (external), an order number (batch id), and a product code (commodity). If you give $LOCATE those three constraints, it will find a unique order. If you give it only a product code, it will find the first order by any customer that includes this product, and $SCAN will then retrieve all orders by all customers that include that product. $LOCATE and $SCAN issued without any constraints at all simply retrieve all customer orders.

$LOCATE really emphasizes the power of the prime-dimensions concept. Since every piece of data *knows* how it relates to the others, you can do a lot with very little; if, for example, you use $LOCATE to find a date, you can pull out everything that hap-

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pened on that day. An Order system with *parts explosion* is merely a matter of a couple of $LOCATE and $SCAN commands in a loop.

The $NEWLVL and $OLDLVL commands allow you to move up and down between children and parents in a hierarchical set. $CALL allows one procedure to call another, and control returns automatically when the called procedure finishes. Calls can be nested in up to nine levels. And calculation is possible in a procedure, although it's currently restricted to four-function arithmetic on 11-digit floating-point numbers.

Since I.D.E.A.S. is an interactive system, you can create new procedures at any time, or modify existing ones, without necessarily altering any data element definitions at all. This makes testing and maintenance a fairly straightforward proposition. Built-in utilities provide cross-referencing of both procedure calls and data-element references by procedures.

THE I.D.E.A.S. SYSTEM

I tested I.D.E.A.S. running on a TDI Pinnacle microcomputer with a Wyse WY-50 terminal. This new machine is similar in many ways to the Sage IV—it's a single-box 68000-based machine with 512K bytes of memory, one 800K-byte floppy-disk drive, and a 21-megabyte Winchester. It runs its 68000 at 12 MHz with no wait states and is normally supplied with a multiuser version of the UCSD p-System and on-board support for up to seven terminals. It's like having a mainframe on your desk, which is just as well since I.D.E.A.S. was born on a mainframe and needs plenty of memory and disk space. The version I tested runs under the alternative multiuser BOS (basic operating system) and is written in RM COBOL. You can port it to any operating system that compiles RM COBOL, which includes MS-DOS and CP/M.

The system consists of three modules, the data dictionary, solution generator, and run-time interpreter, all of which are menu-driven. These modules are entered from a main menu so you never need to exit to the operating system.

In the dictionary you create new data elements or inspect existing ones. When you enter a new name, the system presents you with a blank frame, dimension by dimension, to fill in with float, fix, or irrelevant. And you can list all the elements that use a particular combination of prime dimensions with a menu selection called *frame analysis*. When searching for existing data elements in the dictionary, you can type part of a name and the system will show you all the entries containing that part.

Data names can consist of up to 20 characters (including spaces), which allows you to use readable English. You may also have several names for one object (aliases) so different departments can employ their own uses; for example, the machine shop and the accounting department might have different terms for talking about batches. The system keeps track of such aliases and prevents them from clashing with the names or aliases of other data items.

You can define a data item as numeric, text, or date type, and you can give it a class. The classes are Journal, Ledger, Property, and Transaction, and they determine what you can do to such an item. For instance, if you declare an item as Journal class then you can never delete or alter it, but you can annul it by a later entry, thus preserving a coherent audit trail. You can add to or subtract from Ledger entries but you cannot overwrite them. Properties are ordinary data items with no use restrictions.

In the generator you create procedural frames by first naming them and then roughing them out in the form of comments using an integral editor. When given the generate command, the generator goes through this script, line by line, asking for the details of the $commands and their parameters, labels, jump destinations, and so on. When this is done, it generates the code.

The run-time module is the interpreter from which you use an I.D.E.A.S. application. You run procedures by typing in their names.

I'd like to report that the implementation is as advanced as the principle upon which it's based, but it's not. The program betrays its mainframe origins in a user interface that is decidedly unfriendly by the standards of

modern microcomputer software.

In addition to trivial but irritating details like its refusal to accept menu selections in lowercase, I.D.E.A.S. is designed around a Teletypewriter-style terminal, with a crude line editor for procedural frame construction and no support for modern terminal facilities like cursor addressing or screen highlighting. Much of this is probably due to COBOL's limitations.

The difficulties I had using the program had more to do with this spartan user interface than with the system's underlying concepts. On-line help is minimal and the menus tend to be phrased in I.D.E.A.S. jargon, which is less than clear to a first-time user. And the documentation had few examples, although it is being revised.

There are also some gaps in the specification at the moment, most notably in the area of sorting. There is no provision for lexical or numeric sorting in the procedure generation module. This is not as big a problem as it might appear because I.D.E.A.S. holds and retrieves data already sorted on the prime dimensions. However, it would be better if you could override this with an explicitly requested order in some cases.

I should point out that AI Software doesn't consider I.D.E.A.S. static and is working on a variety of extensions, including a query language (independent of the procedures) and a graphics module. A rewrite (in C) for UNIX systems is also planned; this should provide an opportunity to polish the user interface a little. It is important to note that I.D.E.A.S. is being sold as a tool for systems houses to produce applications for sale on a license basis. It was never intended as an end-user system.

CONCLUSIONS

The concept underlying I.D.E.A.S. seems to me to be a fruitful one. The notion of using dimensions abstracted from the problem domain to structure a database, rather than relationships suggested by the form of data representation (often chosen more by the computer than the user), seems very much in line with the new directions being explored in declarative programming languages.

It would be very interesting to see how well the I.D.E.A.S. concept would translate into Prolog; I suspect that it would go rather simply, since equivalents of $LOCATE and $SCAN are built-in functions of Prolog. I doubt, however, that Prolog is sufficiently known or accepted yet in commercial programming circles for such an experiment to be attractive. ■

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The Fifth Generation in Japan

ICOT

The Hitachi S-810 supercomputer

Software development

BY WILLIAM M. RAIKE

The International Conference on Fifth Generation Computer Systems was held in Tokyo in early November 1984. Over 900 participants, representing 32 countries, each paid about $400 for the privilege of attending. Researchers from all over the world presented 62 research papers, and there were a couple of interesting panel discussions in addition to a highly informative nontechnical lecture by Ezra Vogel ("The Changing Nature of Information Societies").

The objectives of the conference were twofold: to provide an international forum for the exchange of information, ideas, and research in areas related to "new-generation computing," and to present to the world a summary of the achievements of the Japanese government-sponsored Institute for New Generation Computer Technology (ICOT) at the end of the first of its three phases. The second phase of the 10-year project will last four years and the third phase, three years.

To gain perspective on what the Japanese have thus far accomplished in their fifth-generation efforts, you first have to look at the objectives for the project. Note that the buzzwords "fifth-generation computing" and "new-generation computing" are recent additions to computer jargon; they're catch-all terms that include such topics as parallel computer-hardware architectures, artificial intelligence, so-called "expert systems," and "logic programming"—a term used to refer to programming languages such as Prolog.

Started by the Ministry of International Trade and Industry three years ago, ICOT is headed by soft-spoken but intense Dr. Kazuhiro Fuchi. He provides something of a bridge between ICOT's highly technically oriented people, who live in abstract worlds of "parallel data-flow architectures" and "OR-parallel functions of the KL1 kernel language," and the bureaucrats in the Ministry who fund ICOT's research.

Members of the Ministry support such general objectives as giving computers a more direct role in "improving management decision making" as opposed to "mere data processing," providing more "user-friendly interfaces" (including natural-language processing), and "automating software development," etc. They stress the importance of office automation (word processing, filing, etc.), in which Japan lags behind the U.S. by several years (despite its first-class, inexpensive hardware), and would like to see applications of computers in the medical field, which are nearly unheard of here in Japan. These worthy objectives are not tied exclusively to the Fifth Generation Project, but it is important to note that they have been pursued actively outside Japan for years (and not just by computer scientists). Operations-research specialists and "quantitative-management" people were emphasizing these themes as far back as the 1960s. The Japanese computer industry seems remarkably oblivious to the progress that's been made in such areas, principally in software, over the last 15 years; I'll say more about this observation later.

Dr. Fuchi's views on the priorities of ICOT are more illustrative of what is actually going on at the Institute. He insists that the Fifth Generation Project is not intended to produce commercial benefits—a claim that is met with skepticism by just about everyone. In his opinion, ICOT's focus is on basic technological research and development over the long range—10 to 20 years. He doesn't deny that individual companies might spin off segments of the technology before then, but he disavows that as a goal. He says that ICOT has "no intention of getting involved in the artificial-intelligence *business*," although ICOT's close relationship to AI and expert systems is clearly the basis for the choice of a language like Prolog, a so-called "logic programming" language, as the point of departure for the "kernel language" of the Fifth Generation Project.

The kernel language, which is *not* supposed to be viewed as a user language, pro-

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William M. Raike, who holds a Ph.D. in applied mathematics from Northwestern University, has taught operations research and computer science in Austin, Texas, and Monterey, California. He holds a patent on a voice scrambler and was formerly an officer of Cryptext Corporation in the United States. In 1980, he went to Japan looking for 64K-bit RAMs. He has been there ever since as a technical translator and a software developer.

vides both the theoretical and practical interface between the fifth-generation hardware and software. For the first of ICOT's three phases, the kernel language (called KL0) is implemented as a macro language called ESP (extended self-contained Prolog). On one hand, it provides a specific machine language used to define the capabilities of specific fifth-generation hardware. On the other hand, ESP, best described as a macro assembly language for KL0, has been used to write the operating system for the "sequential inference machines" (dubbed PSI machines, for "personal sequential inference machines") that the ICOT researchers will use as basic building blocks to experiment with parallel machine architectures during the second phase of the project. The operating system, called SIMPOS (sequential inference machine programming and operating system), is still incomplete, although enough exists to provide a practical demonstration and research tool.

Interestingly enough, although the PSI machines (six of them exist now, and another dozen or so are scheduled to be completed) are also intended to be used as primary software-development tools for the parallel inference machine (which will be the focus of ICOT's second phase), software development to date has been done on a DEC 2060 and assorted VAX-11 machines.

Dr. Fuchi is concerned about widespread misunderstanding of the role of Prolog (versus LISP) as the basis for the kernel language; he emphasizes that the concept of a kernel language is distinct from that of a user language, and that, while he feels the decision to go with Prolog has been justified by the first-phase results, there is no need to view that choice as static. In fact, one of the outcomes of the research so far has been to point out areas in which Prolog needs to be extended and modified. ESP is one of the results of that process. When I asked Dr. Fuchi whether he felt ICOT's commitment to Prolog-like languages might have been too narrow and whether there would be any changes in that commitment in the future, he replied that, if anything, there would be an expanded effort in that direction. The kernel language for the "parallel inference machine" under development in the second and third phases of ICOT is called KL1; it's going to be based on Concurrent Prolog.

It's never easy to evaluate the results of basic research and development projects. By the time the dust settles, it's hard to remember what was new, what was useful, and what just

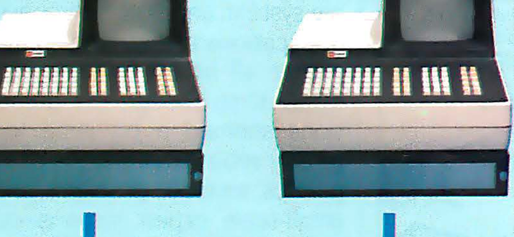
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didn't work. I can see two notable successes, though, for the first phase of ICOT's efforts. No matter where the research goes from here, it's plain that a lot of new hardware, a new operating system, and some demonstration applications are up and running together, all based on logic programming. Even though the demonstrations seemed a bit lame to me—mostly rehashed versions of various puzzles, textbook problems, and very-small-scale expert systems—no one can say "It'll never get off the ground." The other success, easy to overlook, is that Japan, often criticized for copying, adapting, and perfecting existing technology instead of starting something of its own, has made the world sit up and take notice of the fifth-generation project. Efforts like the European Economic Community's ESPRIT (European Strategic Program for Research in Information Technologies) project, Great Britain's Alvey project, and projects in West Germany and France, not to mention the defense-oriented U.S. Strategic Computing program, have all been undertaken and funded in response to the Japanese initiative.

Another remarkable aspect of the Japanese program is that it's being done in the open, accessible to the rest of the world. With the exception of the U.S., all of the representatives of the various international fifth-generation computing projects urged greater international research cooperation. (The U.S. has strongly oriented its efforts toward goals framed in terms of its national security, and even the budget figures since 1982 are not in the public domain.) Whether this cooperation will amount to anything remains to be seen; the U.S.'s David Brandin, former president of the Association for Computing Machinery, quipped: "Everyone's talking about it, but they all want the other guy to go first." Be that as it may, the Japanese, simply by having held this conference, have set an example of openness that deserves to be imitated.

During the week following the conference, ICOT held an open house for participants at its headquarters in Mita, in central Tokyo. The atmosphere at the open house was much less formal than the conference sessions. We were able to ask the ICOT staff about specific details in their specialties, although we had a few language problems because of the low skill level of the Japanese-English interpreters who were available.

During the open house one of the demonstrations of the PSI machine revealed an interesting aspect of Japanese computerdom. This particular demonstration was intended to illustrate a limited English-language parsing (grammatical-analysis) system. Rather than using the keyboard to type in the sample sentence to be analyzed, the operator used a mouse to select individual words from among 30 or so choices that appeared on a menu. One of the reasons the Japanese are so interested in mice is that few of them ever learned to type—in English or Japanese—except for professional typists and the rapidly expanding ranks of word-processor operators.

Conference participants were also invited to participate in "technical visits" to the facilities of various computer and electronics manufacturers in and around Tokyo. A group of us visited the Hitachi Central Research Laboratory (located in the middle of several acres of beautiful woods near Kokubunji on the western fringe of the Tokyo megalopolis), where we got a close look at the Hitachi S-810 supercomputer.

In contrast to the Fifth Generation Project, the S-810 is Hitachi's entry in the commercial competition for the fastest very-large-scale scientific computer. The S-810 has a peak processing rate of over 600 megaflops (million floating-point arithmetic operations per second), somewhat faster than the U.S.'s mammoth Cray-1. It achieves its speed by using a "pipeline" architecture, in which certain operations can be carried out simultaneously on large volumes of data. The Central Research Laboratory uses the S-810 mainly for VLSI (very-large-

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scale integration) circuit-design studies and for large-scale simulation studies in solid-state physics.

The software for the S-810, however, is pathetically unsophisticated. Other than assembly language, the only language available at the laboratory is FORTRAN. Now, I don't want to put down FORTRAN; it was the second computer language I ever learned (back in the days of FORTRAN II), and it is still one of the best tools around for handling complex numbers and other kinds of heavy-duty number crunching. And there are some fine optimizing compilers for FORTRAN (largely because of some of the main weaknesses of the language, like its lack of structure). But since the supercomputer group is supposed to be on the leading edge of the push for improvement in software productivity, I asked the Hitachi researchers what kinds of software tools were used to speed up program development and improve maintainability. I got blank stares. I then asked if they used something like a RATFOR (Rational FORTRAN) preprocessor. I got more blank stares. I was obviously talking about something completely unknown to them. RATFOR is a preprocessor whose use is essentially free; the source code appears, for example, in the book *Software Tools* by Brian W. Kernighan and P. J. Plauger, and the actual preprocessing is very fast, even on personal computers. The benefits, in terms of development speed and program maintainability and readability, are enormous. Even more to the point, such programs have been available and widely known in the U.S. and elsewhere for more than 10 years.

Despite the existence of what was supposed to be an "optimizing vectorizing" compiler that would produce machine code to take the best advantage of the S-810's parallel architecture, the Hitachi research lab people admitted that if they simply ran the same FORTRAN code used previously on their M-280 mainframe, a fast but conventional computer, the supercomputer was no faster! To gain any significant speed advantage from the S-810, they needed to manually "tweak" the code. The conclusion from this and other similar experiences: The Japanese computer industry doesn't yet have its act together in the software department and won't, unless a lot more people in the industry sit up and take notice of how to get things done.

Coming Up

Next month I'll tell you about IBM Japan's test production of 1-megabit dynamic RAM chips and about several new computers on the market here. ■

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Conducted by Steve Ciarcia

Steve on MOVs

My Circuit Cellar article in the December 1983 BYTE, "Keep Power-Line Pollution Out of Your Computer," generated a large number of questions relating to various applications of metal-oxide varistors (MOVs). While letters I've answered in BYTE have addressed some of these specific questions, it seems worthwhile to present some additional information.

I chose the Radio Shack MOV because it was easily obtainable, but there are several other sources. The V130LA10A is manufactured by General Electric and should be available from any local GE parts distributor or electronic parts supply house. In addition, General Instrument and Panasonic manufacture similar units. The equivalent Panasonic part number is ERZ-C14DK201 and is available from a local Panasonic stocking distributor or from

Digi-Key Corporation
Highway 32 South
POB 677
Thief River Falls, MN 56701
(800) 346-5144
The part number is P7063.

The General Instrument equivalent, part number S14K130, is available from

Active Electronics
POB 8000
Westborough, MA 01581
(800) 343-0874

The V8ZA1 MOV shown in the article is designed for 5-volt DC circuits; the V130LA10A is designed for 130-volt AC circuits.

The maximum continuous AC or DC voltage rating of an MOV should be about 10 percent greater than the line or system voltage for which suppression is desired. A general rule is to select the lowest-value MOV that is equal to or greater than the maximum line voltage. For example, if the line voltage is 120 volts AC, $120 \times 1.1 = 132$ volts, and a 130-volt MOV should be the value selected. This is true for line-to-line, as well as line-to-ground, applications. Remember, if a possibility exists that any line connections can be made backward, they will (Murphy's law), so consider this in your selection. Also, the V130LA10A MOVs mentioned in my article can be used for the common mode clamping (line-to-ground) on a 220-volt AC line (providing that a polarized plug is used to ensure proper connections) but will be underrated for the differential mode clamping (line-to-line). A General Electric V250LA20A, or equivalent, is a suitable unit.

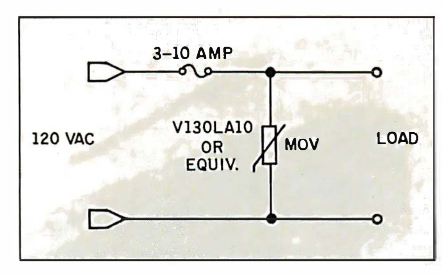


Figure 1: A *fuse can help prevent a failed* MOV *from exploding.*

The energy rating for an MOV should be as high as practical and is often limited by physical space or economic considerations. When surges beyond their ratings are impressed, MOVs usually fail by short-circuiting. If there is no current-limiting protection, large amounts of energy are absorbed, and the MOV can explode. This potential hazard can be minimized by the addition of a fuse, as shown in figure 1, and physically shielding the MOV from surrounding circuits. The fuse should be placed to open the circuit when the device fails, so that loss of transient protection is known.

Devices that connect across the power line at the service entrance to reduce the amplitude of large transients and lightning surges are available. They are two-pole, three-wire units that are designed for 120/240-volt single-phase service and are designed to mount in a ½-inch knockout in the service entrance box or at the weatherhead. Such devices are available at local electrical supply houses and are in the $20 range. They clip at voltages higher than the MOVs described in my article, so the MOVs should still be used. The General Electric Home Lightning Protector GE Thyrite 9L15BC002, Square D Model J9200-10, and Delta Lightning Arrestor (POB 1084, Big Spring, TX 79720, (915) 267-5268) are suitable units.

All of the sockets on the power strip are in parallel, so it does not make any difference where the MOVs are placed. They can be placed across one socket or spread out for ease of assembly. Should a transient appear on the line, the MOVs will clamp it to a safe level. The important thing is to keep the lead length short so that the clamping voltage is not compromised.

If your power strip contains a line filter, it is desirable to place the MOVs downstream (equipment side) of the filter. The filter will attenuate some transients and may possibly extend the life of the MOV. Several companies manufacture power-line filters that are suitable for such applications. They include

Corcom Inc.
1600 Winchester Rd.
Libertyville, IL 60048
(312) 680-7400
Type 5VK1 or 5VK3

Cornell-Dubilier Electronics
150 Avenue L
Newark, NJ 07105
(201) 589-7500
Type APF511L

Delta Electronic Industry USA
1355 Yosemite Way
Hayward, CA 94545
(415) 785-5231
Type 05DBAG5

Potter Company
POB 337
Wesson, MS 39191
(601) 643-2215
Type 600A5

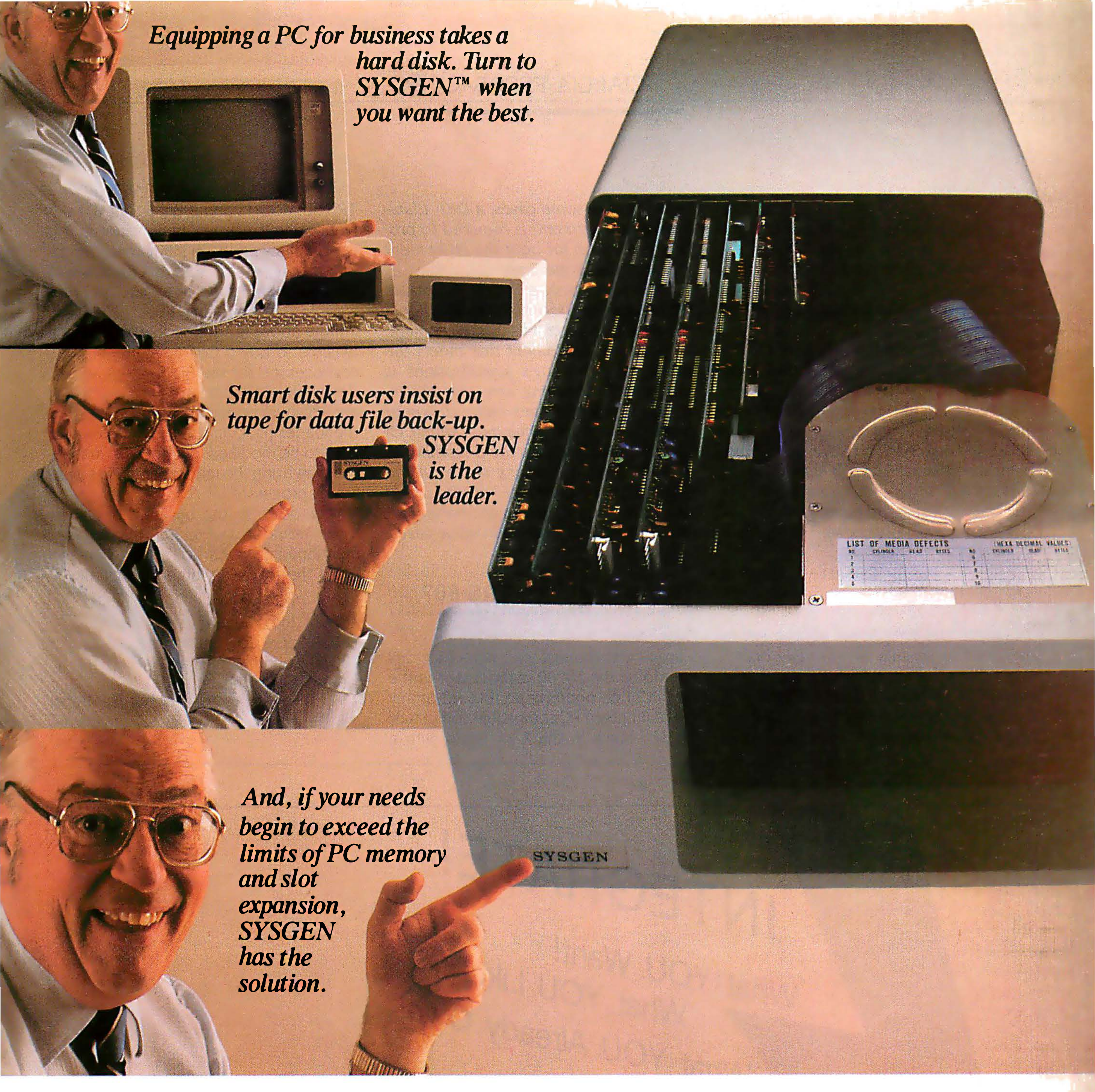
These filters are equivalent to the Radio Shack part number 273-100 listed in my article, which is no longer being stocked. Write the manufacturers for additional information and the address of your nearest supplier.—Steve

Telephone-Line Protection

Dear Steve,

I enjoyed your article on the musical telephone bell greatly (July 1984). It's a

(continued)



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nice project, and I plan to construct one.

Two questions: You mentioned that the telephone company occasionally puts a 200-V test signal on the line. Doesn't this have an adverse effect on modems and electronic equipment such as Demon Dialers?

Also, as a practical matter, what are the risks from lightning to equipment connected to the telephone system? Again, I'm concerned about modems and electronic dialers. I have seen protection devices marketed for telephone equipment, but I don't know if they're really needed and if they really work.

Thanks for the information. I always look forward to your articles as the highlight of BYTE!

CHARLES J. OKSTEIN
Willimantic, CT

Commercial telephone equipment is designed to survive all normally occurring voltages on the telephone line. In the case of the Whimsi-Bell, the TCM1520A has the protection built into it, and none of the other components are connected to the line. In some cases, a DAA (data-access arrangement) is required to provide protection for both the equipment and the telephone lines.

The telephone company incorporates lightning protection into the telephone-line system to protect its own equipment, so customer equipment that meets the telephone company's specifications is pretty safe. Lightning arrestors are installed where the lines enter customer buildings to protect equipment within. Of course, there is always the possibility of damage from a lightning strike on the lines in your immediate vicinity. Local protection in addition to the normal arrestors might be justified in some cases. —Steve

TRUMP CARD FOR TRS-80?

Dear Steve,

I read with interest your pair of articles on adding the Z8000 coprocessor to the IBM PC. I do not have an IBM PC or any of the umpteen PC-compatible computers. I'm still stuck in the 8-bit world with a TRS-80 Model I and a Big Board II. I was wondering if you would consider (if it is possible) rewriting the loader program for Z80 machines. I am sure that there would be a large market for the board and software in the 8-bit market.

If the above is not possible, would it be feasible to buy a Co-Power 88 (an 8088 coprocessor) for the Big Board II and redesign the Z8000 board a little for use in my STD bus connector? I would think that the loader program for the Z8000 would have to be modified, but not as extensively as rewriting the loader for use on a different processor.

Now, down to the business end. How much would it cost to buy the software mentioned in your article? And where can I find the following integrated circuits?

Z8001 Processor
Z8581 Clock Generator
Z8030 Serial Communications Controller
Z8036 Counter/Timer and
Parallel I/O Unit

MARK HAMPTON
Cocoa, FL

(continued)

Since the Trump Card articles appeared, I have had many requests to modify the Trump Card hardware and software to operate on different machines. Unfortunately, each system would require a slightly modified hardware and software interface. The hardware and software design time to do this would severely cut into my other Circuit Cellar projects, so I am making no plans to convert the Trump Card project to any other system.

The Trump Card has been tested on several PC-compatible systems using MS-DOS and has worked fine. Since the Co-Power 88 operates under MS-DOS, it is possible that the Trump Card software will work with the system. However, since I have never tried this configuration, I cannot guarantee that it will work.

Under my "Reward for Diligence" program discussed in the first part of the Trump Card article, I will send you the Trump Card software and the Trump Card manual for the cost of duplicating and mailing ($30), if you send me a picture of your Trump Card project.

The Zilog chips can be obtained from any of the Zilog distributors near you. In Florida, the Zilog sales offices are Dyne-A-Mark Corp. in Clearwater and Palm Bay and Technical Center-Zilog Corp. in Clearwater.—Steve

EMI

Dear Steve,

Because I live in a metropolitan area, EMI is a problem. Within a few blocks of my apartment are a 10-kW (100-kW ERP) FM transmitter, about six microwave relays, and possibly other transmitters. I want to retrofit an old TRS-80 Model I, printer, video display, and other peripherals. What regions of a computer are most susceptible to EMI? Would replacing LS ICs with HCT or HC ICs increase immunity to effects of EMI?

JAMES HAWKINS
Kansas City, MO

Electromagnetic-interference problems in microcomputer systems can come from any number of sources. Usually, electrical noise from an outside source is induced into cables that lead into (and out of) the computer. Sensitive circuits in the computer can also be affected if they are not properly shielded.

Since the subject of electromagnetic-interference elimination is too long to be properly discussed in a letter, I will refer you to an article I wrote that covers the subject in depth. The article, appropriately called "Electromagnetic Interference," can be found in the January 1981 BYTE.
—Steve ■

Over the years I have presented many different projects in BYTE. I know many of you have built them and are making use of them in many ways.

I am interested in hearing from any of you telling me what you've done with these projects or how you may have been influenced by the basic ideas. Write me at Circuit Cellar Feedback, POB 582, Glastonbury, CT 06033 and fill me in on your applications. All letters and photographs become the property of Steve Ciarcia and cannot be returned.

B·O·O·K·S R·E·C·E·I·V·E·D

ALGORITHM DESIGN FOR COMPUTER SYSTEM DESIGN, G. Ausiello, M. Lucertini, and P. Serafini, eds. New York: Springer-Verlag, 1984; 248 pages, 17 by 24 cm, softcover, ISBN 0-387-81816-2, $18.30.

APPLE HOME COMPANION, George Beekman and Dennis Corliss. Chatsworth, CA: Datamost, 1984; 360 pages, 13.3 by 20.8 cm, softcover, ISBN 0-88190-318-3, $19.95.

APPLE LISA: A USER-FRIENDLY HANDBOOK, Joseph Coleman. Blue Ridge Summit, PA: Tab Books, 1984; 320 pages, 18.8 by 23.5 cm, softcover, ISBN 0-8306-1691-8, $16.95.

APPLE MACINTOSH USER'S HANDBOOK, staff of Weber Systems. New York: Ballantine Books, 1984; 328 pages, 14 by 21.5 cm, softcover, ISBN 0-345-31840-4, $9.95.

APPLE THESAURUS, Aaron Filler. Chatsworth, CA: Datamost, 1984, 896 pages, 21 by 27.5 cm, softcover, ISBN 0-88190-346-9, $29.95.

APPLE IIE PROGRAMMING, BOOK ONE, Phil Robinson. Englewood Cliffs, NJ: Prentice-Hall, 1984; 64 pages, 21.5 by 28 cm, softcover, ISBN 0-13-038456-9, $10.95.

ASSEMBLY LANGUAGE PROGRAMMING FOR THE TRS-80 MODEL 16, Dan Keen and Dave Dischert. Blue Ridge Summit, PA: Tab Books, 1984; 196 pages, 13 by 21 cm, softcover, ISBN 0-8306-1649-7, $10.25.

THE BASIC EXPLORER FOR THE COMMODORE 64, Lee Berman and Ken Leonard. Berkeley, CA: Osborne/McGraw-Hill, 1985; 288 pages, 18.5 by 23.5 cm, softcover, ISBN 0-88134-139-8, $11.95.

BASIC FUNDAMENTALS AND STYLE, James S. Quasney and John Maniotes. Boston, MA: Boyd & Fraser Publishing Co., 1984; 480 pages, 21 by 27.5 cm, softcover, ISBN 0-87835-138-8, $25. Includes template.

BEGINNER'S GUIDE TO MICROPROCESSORS, 2nd ed., Charles M. Gilmore. Blue Ridge Summit, PA: Tab Books, 1984; 224 pages, 12.8 by 21 cm, softcover, ISBN 0-8306-1695-0, $9.95.

BUSINESS COMPUTING: A STRUCTURED APPROACH TO BASIC ON THE PDP-11 & VAX-11, James F. Peters III and Hamed M. Sallam. Reston, VA: Reston Publishing, 1985; 704 pages, 21.3 by 27.5 cm, softcover, ISBN 0-8359-0549-7, $21.95.

THE BUSINESS GUIDE TO THE XENIX SYSTEM, Jean L. Yates, Sandra L. Emerson, and Candice Basham. Reading, MA: Addison-Wesley, 1984; 496 pages, 18.5 by 23.5 cm, softcover, ISBN 0-201-08847-9, $19.95.

BUSINESS POWER FOR YOUR APPLE, Gregory R. Glau. New York: Van Nostrand Reinhold, 1984; 304 pages, 15.5 by 23.5 cm, hardcover, ISBN 0-442-22779-5, $32.95.

THE C-64 PROGRAM FACTORY, George Stewart. Berkeley, CA: Osborne/McGraw-Hill, 1985; 336 pages, 16 by 23.5 cm, softcover, ISBN 0-88134-150-9, $12.95.

THE COMAL HANDBOOK, 2nd ed., Len Lindsay. Reston, VA: Reston Publishing, 1984; 480 pages, 17.5 by 23.5 cm, softcover, ISBN 0-8359-0784-8, $18.95.

CATALOGUE OF ARTIFICIAL INTELLIGENCE TOOLS, Alan Bundy, ed. New York: Springer-Verlag, 1984; 180 pages, 16.5 by 24 cm, softcover, ISBN 0-387-13938-9, $17

COMMODORE 64 FUN AND GAMES, VOLUME 2, Ron Jeffries and Glen Fisher. New York: Warner Books, 1984; 188 pages, 21.3 by 27.5 cm, softcover, ISBN 0-446-38183-7, $12.95.

THE COMPLETE BOOK OF LISA, Kurt J. Schmucker. New York: Harper & Row, 1984; 352 pages, 15.5 by 23.5 cm, softcover, ISBN 0-06-669008-0, $17.95.

COMPUTER-BASED INSTRUCTION: METHODS AND DEVELOPMENT, Stephen M. Alessi and Stanley R. Trollip. Englewood Cliffs, NJ: Prentice-Hall, 1985; 432 pages, 17.5 by 23.3 cm, softcover, ISBN 0-13-164161-1-01, $21.95.

THE COMPUTER BUYER'S SURVIVAL MANUAL, C. Amos Johnson. Blue Ridge Summit, PA: Tab Books, 1984; 224 pages, 12.8 by 20.8 cm, softcover, ISBN 0-8306-1767-1, $9.95.

COMPUTER CARE, Herb Friedman. Englewood Cliffs, NJ: Prentice-Hall, 1984; 182 pages, 15 by 23 cm, softcover, ISBN 0-13-163833-5, $14.95.

THE COMPUTER ENTREPRENEURS, Robert Levering, Michael Katz, and Milton Moskowitz. New York: New American Library, 1984; 496 pages, 16 by 23.5 cm, hardcover, ISBN 0-453-00477-6, $19.95.

COMPUTER GRAPHICS AND APPLICATIONS, D. Harris. New York: Chapman and Hall, 1984; 184 pages, 15.5 by 23.3 cm, softcover, ISBN 0-412-25090-X, $19.95.

COMPUTER LITERACY, Warren Jones, Bobbie Jones, Kevin Bowyer, and Mel Ray. Reston, VA: Reston Publishing, 1983; 304 pages, 17.5 by 23.5 cm, softcover, ISBN 0-8359-0860-7, $16.95.

THIS IS A LIST *of books received at* BYTE *Publications. It is not meant to be exhaustive; its purpose is to acquaint* BYTE *readers with recently published titles in computer science and related fields. We regret that we cannot review all the books we receive; instead, this list is meant to be a monthly acknowledgment of these books and the publishers who sent them.*

COMPUTERS AND INFORMATION PROCESSING WORLD INDEX, Suzan Deighton, John Gurnsey, and Janet Tomlinson, eds. Phoenix, AZ: The Oryz Press, 1984; 640 pages, 22 by 30 cm, hardcover, ISBN 0-89774-116-1, $74.50.

COMPUTING FOR EXECUTIVES, J. W. Chadwick. Blue Ridge Summit, PA: Tab Books, 1984; 280 pages, 13 by 21 cm, softcover, ISBN 0-8306-1796-5, $12.95.

CONQUERING THE COMMODORE 64 KINGDOM, Bill L. Behrendt. Englewood Cliffs, NJ: Prentice-Hall, 1984; 192 pages, 17.5 by 23.5, softcover, ISBN 0-13-167917-1, $14.95.

COOKBOOK OF CREATIVE PROGRAMS FOR THE COMMODORE 64, Robert Rinder. New York: New American Library, 1984; 222 pages, 18 by 25.5 cm, softcover, ISBN 0-452-25571-6, $12.95.

CREATING THE PERFECT DATABASE USING DB MASTER, Trish McClelland. Glenview, IL: Scott, Foresman and Co., 1985; 256 pages, 19.3 by 23.5 cm, softcover, ISBN 0-673-18039-5, $17.95.

DATAPRO/MCGRAW-HILL GUIDE TO APPLE SOFTWARE, 2nd ed., Datapro Research Corporation. New York: McGraw-Hill, 1985; 362 pages, 21.5 by 28 cm, softcover, ISBN 0-07-015406-6, $22.95.

DATAPRO/MCGRAW-HILL GUIDE TO CP/M SOFTWARE, 2nd ed., Datapro Research Corporation. New York: McGraw-Hill, 1985; 400 pages, 21.5 by 28 cm, softcover, ISBN 0-07-015408-2, $22.95.

DATAPRO/MCGRAW-HILL GUIDE TO IBM PC SOFTWARE, 2nd ed., Datapro Research Corporation. New York: McGraw-Hill, 1985; 404 pages, 21.5 by 28 cm, softcover, ISBN 0-07-015407-4, $22.95.

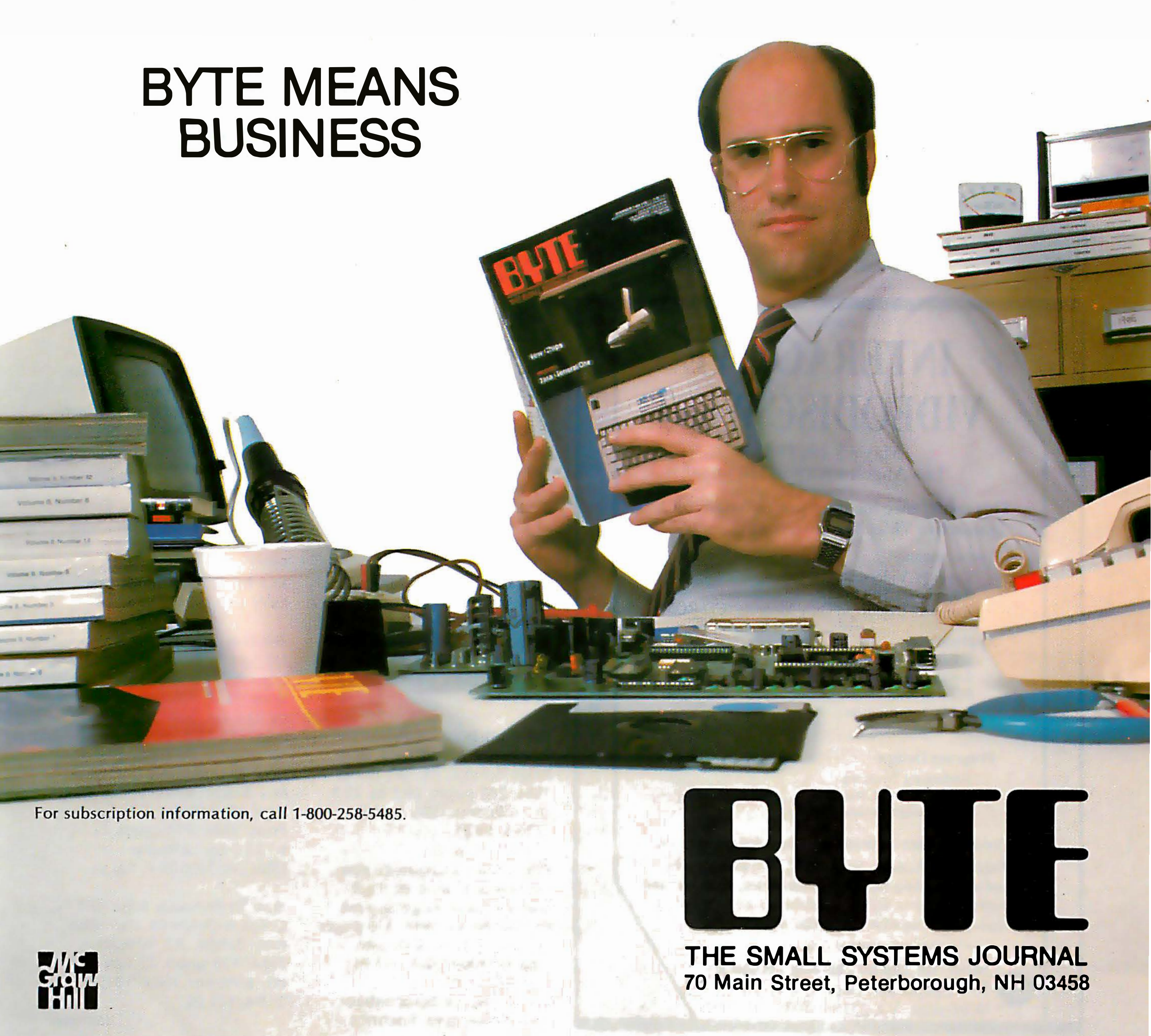
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THE DESIGNER'S GUIDE TO DISK DRIVES. Edward R. Teja. Reston, VA: Reston Publishing, 1985: 142 pages, 18 by 24 cm, hardcover, ISBN 0-8359-1268-X, $29.95.

DESIGNING APPLE GAMES WITH PIZAZZ! Greg Minter and John Ruffner. Chatsworth, CA: Datamost, 1984; 328 pages, 17.8 by 25.3 cm, softcover, ISBN 0-88190-387-6, $14.95.

DICTIONARY OF COMPUTING AND NEW INFORMATION TECHNOLOGY, A. J. Meadows, M. Gordon, and A. Singleton. New York: Nichols Publishing, 1984; 232 pages, 13.3 by 20.5 cm, hardcover, ISBN 0-89397-197-9, $24.50.

DIGITAL SYSTEMS, PRINCIPLES AND APPLICATIONS, 3rd ed., R. J. Tocci. Englewood Cliffs, NJ: Prentice-Hall, 1985; 608 pages, 18.3 by 24.3 cm, hardcover, ISBN 0-13-212374-6, $29.95.

DISCOVERING SCIENCE ON YOUR ADAM WITH 25 PROGRAMS, John Pellino, Mary Ellen Adamo, Sandra Dobrowlsky, and Donald P. LaSalle. Blue Ridge Summit, PA: Tab Books, 1984; 192 pages, 19 by 23.5 cm, softcover, ISBN 0-8306-1780-9, $9.95.

ESSENTIAL APPLICATIONS FOR THE IBM PC AND XT, Patrick Plemmons and the editors of *PC World*. New York: Simon & Schuster, 1984; 256 pages, 19 by 23.5 cm, softcover, ISBN 0-671-49279-9, $16.95.

FINANCIAL DECISION MAKING WITH YOUR TRS-80 MODEL 100, Leslie Sparks. Blue Ridge Summit, PA: Tab Books, 1984; 142 pages, 18.5 by 23.5 cm, softcover, ISBN 0-8306-1799-X, $9.95.

THE FIRST BOOK OF ADAM THE COMPUTER, Arthur Dent. Blue Ridge Summit, PA: Tab Books, 1984; 208 pages, 19.5 by 23.5 cm, softcover, ISBN 0-8306-1720-5, $9.25.

FUN, GAMES & GRAPHICS FOR THE APPLE II, IIE & IIC, Paul Garrison. Blue Ridge Summit, PA: Tab Books, 1984; 316 pages, 18.5 by 23.3 cm, softcover, ISBN 0-8306-1752-3, $13.95.

THE FUTURE OF SEMICONDUCTORS, COMPUTERS, ROBOTICS, AND TELECOMMUNICATIONS, editorial staff of Petrocelli Books. Princeton, NJ: Petrocelli Books, 1984; 264 pages, 16 by 24 cm, hardcover, ISBN 0-89433-259-7, $49.95.

GAMES & UTILITIES FOR THE TRS-80 MODEL 100, Ron Karr, Steven Olsen, and Robert Lafore. New York: New American Library, 1984; 204 pages, 18.5 by 23.5 cm, softcover, ISBN 0-452-25577-5, $16.95.

GETTING THE MOST FROM YOUR POCKET COMPUTER, Stephen F. Nowak. Blue Ridge Summit, PA: Tab Books, 1984; 236 pages, 13 by 21 cm, softcover, ISBN 0-8306-1723-X, $9.95.

GETTING STARTED IN PASCAL PROGRAMMING, J. Camara and F. Puccetti. Blue Ridge Summit, PA: Tab Books, 1984; 206 pages, 18.5 by 23.5 cm, softcover, ISBN 0-8306-0588-6, $12.95.

HANDBOOK OF BAR CODING SYSTEMS, H. E. Burke. New York: Van Nostrand Reinhold, 1984; 240 pages, 16 by 23 cm, hardcover, ISBN 0-442-21430-8, $42.50.

HIDDEN POWERS OF THE TRS-80 MODEL 100, Christopher L. Morgan. New York: New American Library, 1984; 254 pages, 18.5 by 23 cm, softcover, ISBN 0-452-25578-3, $19.95.

A HOBBYIST'S GUIDE TO COMPUTER EXPERIMENTATION, John D. Lenk. Englewood Cliffs, NJ: Prentice-Hall, 1985; 300 pages, 15.5 by 23.5 cm, hardcover, ISBN 0-13-392473-4, $23.95.

THE HOME COMPUTER WARS, Michael S. Tomczyk. Greensboro, NC: Compute! Publications, 1984; 318 pages, 14 by 21.5 cm, softcover, ISBN 0-942386-75-2, $9.95.

HOW TO COPYRIGHT SOFTWARE, M. J. Salone with Stephen Elias, legal ed. Berkeley, CA: Nolo Press, 1984; 256 pages, 21 by 27.5 cm, softcover, ISBN 0-917316-79-7; $21.95.

HOW TO PROGRAM YOUR IBM PC COLOR & GRAPHICS, Carl Shipman. Tucson, AZ: HPBooks, 1984; 320 pages, 21.5 by 27.5 cm, softcover, ISBN 0-89586-265-4, $21.95.

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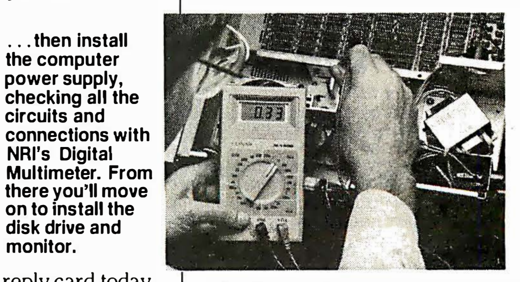
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HOW TO RUN YOUR BUSINESS WITH DBASE II, Richard H. Baker. Blue Ridge Summit, PA: Tab Books, 1984; 320 pages, 18.5 by 23.5 cm, softcover, ISBN 0-8306-1918-6, $16.95.

HOW TO WRITE A COMPUTER MANUAL, Jonathan Price. Menlo Park, CA: Benjamin/Cummings, 1984; 320 pages, 18.5 by 23 cm, softcover, ISBN 0-8053-6870-1, $21.95.

IBM CPU AND STORAGE ARCHITECTURE, Joe Leben and Jim Arnold. New York: John Wiley & Sons, 1984; 192 pages, 22.5 by 28.5 cm, spiral-bound, ISBN 0-471-80142-9, $49.95.

IBM PC BASIC, Ralph Vickers. New York: Harper & Row, 1984; 304 pages, 15.5 by 23.5 cm, softcover, ISBN 0-06-669013-7, $16.95.

IBM PC COBOL, William I. Atkinson Jr. and Paul A. DeSanctis. Reston, VA: Reston Publishing, 1985; 304 pages, 17.5 by 23 cm, softcover, ISBN 0-8359-3051-3, $19.95.

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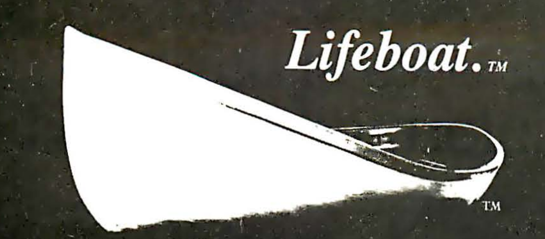
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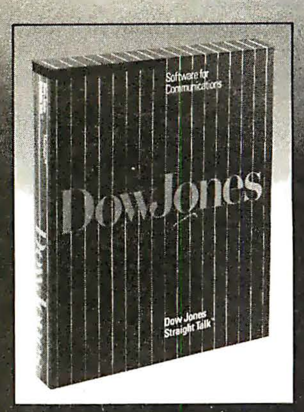
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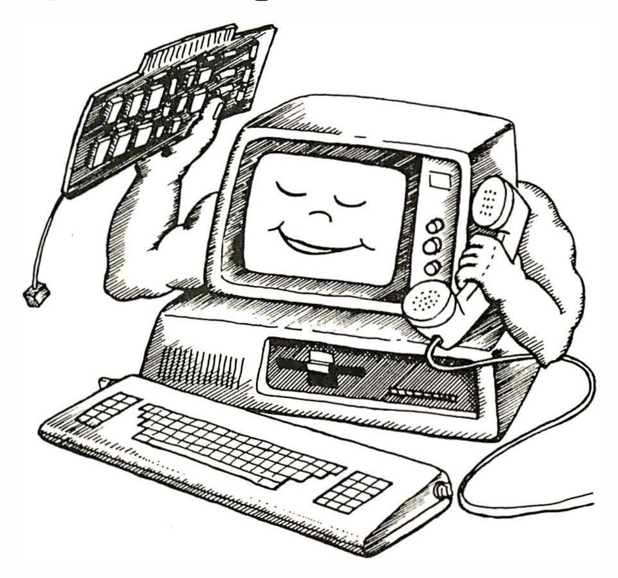
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LOAD ASSEMBLER ROUTINES FROM BASIC

BY DOUGLAS F. YRIART

This method enhances the maintainability of your programs

MICROSOFT BASIC-80, version 5.x for CP/M, includes a number of statements and functions for *calling* machine-language subroutines from BASIC and defining their starting addresses. It does not, however, include a statement for *loading* these subroutines. This article presents a way to automatically assemble and load them. BASIC-80 includes all the tools you need to reserve memory for your subroutines and to load them from the hexadecimal-format file put out by Digital Research's assembler, ASM.COM. The BASIC program doesn't need to know anything about the subroutine except the name of the .HEX file in which it is stored. This file contains all the necessary information for the load, including how much memory is needed.

With this method of loading assembly-language subroutines, you don't need to modify the BASIC program every time you change, add, or delete a few bytes in the assembly-language subroutine. In addition, you can use the same BASIC routine in numerous programs to load assembled subroutines. This method brings significant benefits in simplicity and maintainability.

ASSEMBLY-LANGUAGE SUBROUTINE

First, you need an assembly-language subroutine for the BASIC program to call. For example, TEST.ASM (see listing 1) draws an outline of the starship *Enterprise* and then returns control to the calling program. [*Editor's note: The unassembled source code for* TEST.ASM *is available from* BYTE*net Listings. The telephone number is* (603) 924-9820.] Two important points should be considered about the assembly-language subroutine. The first one is its origin. You need to start at as high an address in memory as possible so that the BASIC program will have sufficient room for its execution.

Second, the subroutine must exit through an RET instruction if you want control to return to the BASIC program. After you assemble the subroutine with ASM.COM, you don't need to make it into a machine-code file with LOAD.COM. The BASIC program works with the .HEX file. And, if you try to create a runnable .COM file, you will need a lot of disk space. LOAD.COM will attempt to create a file the size of the entire memory taken up by the subroutine, including any unused space below the origin.

Table 1 contains TEST.HEX, produced by assembling TEST.ASM. Notice in listing 1 that the program arbitrarily starts at location 9C40 hexadecimal (in the leftmost column on the line with the ORG statement). This same number appears in positions four through seven on the first line of table 1. LOAD.COM uses the first nine positions and the last two positions of each record or line of the .HEX file for its own purposes. The remaining pairs of hexadecimal digits are the instruction, operand, and data bytes you want to load into memory. The first two positions after the colon at

(continued)

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Listing 1: TEST.PRN, *a listing of the assembled routine,* TEST.ASM. *This test program is for use in developing a* BASIC *program to read and* POKE *the* .HEX *file of assembly-language routines into memory. This program draws a picture of the starship* Enterprise.

```
                ;-------------------------------------------------------------
                ; TEST.ASM   version 1.0          1/13/84
                ;
                ; by D. F. Yriart — January 1984
                ;
                ; Test program for use in developing BASIC program
                ; to read and poke HEX file of assembly-language
                ; routines into memory. This program draws a
                ; picture of the starship Enterprise.
                ;
                ;-------------------------------------------------------------
                ;
                ; EQUATES
                ;
0009 =          pbuff   equ     9       ;BDOS print buffer
0005 =          bdos    equ     5       ;location of BDOS
000D =          cr      equ     0dh     ;carriage return
000A =          lf      equ     0ah     ;line feed
0009 =          tab     equ     9       ;horizontal tab
                ;
                ; START OF PROGRAM
                ;
9C40                    org     40000d
                ;
                start:
9C40 114C9C             lxi     d,data  ;point to picture
9C43 CD479C             call    print   ;display it
9C46 C9                 ret             ;. . .done
                print:
9C47 0E09               mvi     c,pbuff ;get proper call in c
9C49 C30500             jmp     bdos    ;do it
                ;
                ; STORAGE AREA
                ;
                ; note: DATA: is made up of any printable or control characters
                ;         that will draw or write an appropriate display for user
                ;         to look at.
                ;
                ;         The display is "plain vanilla" characters that can be
                ;         found on any CP/M machine; no special screen control
                ;         or graphics characters are used for portability.
                ;
9C4C 0D0A0A0A0A data:   db      cr,lf,lf,lf,lf,lf,lf,lf,lf,lf,lf,lf
9C58 0A0A0A0A           db      lf,lf,lf,lf
9C5C 0909202020         db      tab,tab,'     ,------ * ------,'
9C81 0D0A               db      cr,lf
9C83 0909202020         db      tab,tab,'  ,-------------   '---  ------'
9CA6 270D0A             db      39,cr,lf
9CA9 0909202020         db      tab,tab,'      '---------  --',39,'      / /'
9CC6 0D0A               db      cr,lf
9CC8 0909202020         db      tab,tab,'  ,---',39,32,39,'-------/ /--,'
9CE7 0D0A               db      cr,lf
9CE9 0909202020         db      tab,tab,'        '---------------',39
9D07 0D0A0A             db      cr,lf,lf
9D0A 0909202020         db      tab,tab,'    THE USS ENTERPRISE --- NCC-1701'
9D2E 0D0A24             db      cr,lf,'$'
9D31                    end
```

the beginning of each record tell LOAD.COM how many bytes of data are in the record.

THE BASIC PROGRAM

Let's look at the BASIC program itself, READASM.BAS (see listing 2 or BYTEnet Listings (603) 924-9820). It accomplishes four tasks:

1. It finds out where to load the assembled subroutine and reserves enough memory for it.
2. It loads the subroutine.
3. It passes control to the subroutine, executing it—if instructed to do so.
4. It restores the subroutine's reserved memory for use by the BASIC program before ending. First, the program must find the top of the TPA (transient program area)—the area of memory available for user programs that is not taken up by CP/M—so that it can restore the full amount of memory to the BASIC program at the end of the run.

Figure 1 provides a memory map of CP/M-80 version 2.2. It is important to notice the number of bytes added to the address of the CCP (console command processor) to find the BDOS (basic disk operating system) and BIOS (basic input/output system) areas. (Addresses are hexadecimal.)

The address of the CP/M BIOS is

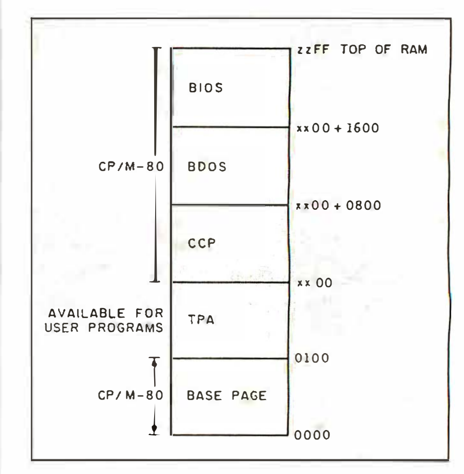


Figure 1: *Hexadecimal memory map of* CP/M. *The* xx *and* zz *are dummy arguments representing the most significant byte in an address that changes depending upon memory size.*

stored in bytes one and two of the base page (BP). Intel 8080 machine code stores the least significant byte (LSB) of the memory address first, followed in byte two by the most significant byte (MSB). Starting at line 140, the program captures this byte by executing a PEEK at location two. The beginning of the CCP is found by subtracting 16 hexadecimal from the MSB of the BIOS address.

In lines 150–170, the starting address of BDOS, the top of the TPA, is found by doing some *string arithmetic* on the MSB of the CCP address. The VAL() function evaluates strings that start with &H as hexadecimal numbers. The HEX$() function returns a character string containing the hexadecimal digits of the number evaluated. You can use this to build a string composed of &H, the MSB of the CCP address, and an LSB of 00. The VAL() function turns this character string into a number to be assigned to the variable TOP. By adding 800 hexadecimal to TOP, you have the address of the beginning of the TPA. The addresses found in high memory are numbers beyond the range of BASIC-80's valid integers. Therefore, you can't use integer variables to hold addresses in the program.

Reserving Subroutine Memory

To reserve memory for the assembled subroutine, you use the CLEAR, ADDRESS statement, which sets aside memory starting at the ADDRESS parameter. The CLEAR statement zeros all numeric variables and sets all string variables to null. Any value that you need to use after clearing memory must be saved in an area unaffected by the CLEAR, so that you can retrieve it later. In this example you need to save the name of the .HEX file, the value of TOP, and the loading address for the subroutine.

Lines 240–300 read the first record of the .HEX file and extract the address needed to load the subroutine. This starting address is in positions four through seven of the record (lines 280–300). Notice the use of string

(continued)

Table 1: TEST.HEX *is the hexadecimal-file output from assembling* TEST.ASM. *The table is annotated to show the various parts of the records. All data is hexadecimal.* ("|" *is inserted to show parts of the record.*)

```
Data bytes
in record
 |            Data bytes (two characters each)
 |  Load                /              \
 |  address            /                 \               Overhead
 |     |              /                    \                  |
 v  |  v  |          /                       \             |  v
:10|9C40|00114C9CCD479CC90E09C305000D0A0A0A|98
:10|9C50|000A0A0A0A0A0A0A0A0A0A0A09092020|3A
:10|9C60|00202020202020202020202020202020|F4
:10|9C70|0020202C2D2D2D2D2D2D2A2D2D2D2D2D|32
:10|9C80|002C0D0A09092020202C2D2D2D2D2D2D|B8
:10|9C90|002D2D2D2D2D2D2D202020602D2D2D2020|02
:10|9CA0|002D2D2D2D2D2D270D0A09092020202060|76
:10|9CB0|002D2D2D2D2D2D2D2D2D202D2D27202020|0E
:10|9CC0|002020202F202F0D0A0909202020202020|CD
:10|9CD0|002020202C2D2D2D2720272D2D2D2D2D2D|F5
:10|9CE0|002D2F202F2D2D2C0D0A09092020202020|7A
:10|9CF0|002020202020602D2D2D2D2D2D2D2D2D2D|A2
:10|9D00|002D2D2D2D2D2D270D0A0A090920202054|37
:10|9D10|00484520555353320454E54455250524953|BF
:10|9D20|0045202D2D2D204E43432D313730310D0A|46
:01|9D30|0024|0E
:0000000000         \
           \     Overhead (1 byte)
            \
       "End-of-file" record
```

Listing 2: READASM.BAS, *a program in Microsoft* BASIC-80 *to load and run assembly-language routines.*

```
10 '                <<<    READASM.BAS    >>>
20 PRINT
30 PRINT TAB(10);"ASSEMBLY-LANGUAGE FILE LOADER":PRINT
40 '
50 '       Demonstration of method to read and load assembly-
60 '       language programs from a HEX file for calling from
70 '       inside a BASIC-80, version 5.x, program.
80 '
90 '       by D. F. Yriart — January 1984
100 '
110 '       First find the beginning of BIOS — so full memory can
120 '       be restored after the program runs.
130 '
140        BIOS=PEEK(2)                          ' MSB of BIOS entry address
150        CCP=BIOS-&H16                         ' beginning of CCP
160        TOP=VAL("&H"+HEX$(CCP)+"00")          ' compute top of
170        TOP=TOP+&H800                         ' transient program area
180        PRINT "TOP OF TRANSIENT PROGRAM AREA = ";HEX$(TOP);
190        PRINT " HEX."
200 '
210 '       Open the HEX file and read the first line to get
220 '       starting address for the routine.
230 '
240        HEX.FILE$="TEST.HEX"        ' name of file to load
250        ON ERROR GOTO 1210          ' trap missing file error
```

(continued)

arithmetic to convert the text *number* to hexadecimal so the program can use it.

In order to protect the information needed after the CLEAR, you must store it somewhere outside of the BASIC program's normal workspace. This program uses the buffer area that CP/M uses for passing commands to the CCP. This buffer area begins at memory location 80 hexadecimal. Lines 370–470 build a 20-character string of data and use POKE to put it into the buffer area. You must store memory addresses as character strings because they are too large to store in a single byte.

Line 520 reserves the memory needed for the subroutine by doing a CLEAR of memory up to 1 byte below the subroutine's starting address. The data is retrieved from the CCP buffer in lines 570–650. Lines 670 and 680 serve the cosmetic function of trimming trailing blanks off the filename.

Subroutine Usage

The BASIC program reads the .HEX file one record at a time, captures the data from position 10 to 2 bytes from the end of each record, and uses a POKE to put 1 byte at a time into memory. This is accomplished by two nested WHILE/WEND loops. Two variables control the operation: BYTE contains the next address on which the POKE statement operates, and COUNT is the data-string position of the next byte to be extracted.

The outer loop (lines 790–940) reads records until it encounters the end of the file. Line 830 extracts the data portion of each record for processing by the inner loop (lines 860–920). The inner loop steps through the data string two characters at a time—two hexadecimal digits make up one byte. Line 880 converts the string data into values that can be put into memory with a POKE.

Once the BASIC program has read the last record from the .HEX file, the worst is over. The subroutine is in reserved memory above the BASIC work area. All that remains to be done is to test it out, restore the top of

```
260    OPEN "I",#1,HEX.FILE$
270    IF EOF(1) THEN 1170          ' test for empty file
280    LINE INPUT#1,A$              ' read the first record
290    CLOSE 1
300    START.ADDRESS = VAL("&H" + MID$(A$,4,4))
310    PRINT "Loading will start at ";HEX$(START.ADDRESS);
320    PRINT " hex."
330 '
340 '    Build a string out of the name of the HEX file, the
350 '    top of TPA address, and the loading address.
360 '
370    SAVE.IT$ = SPACE$(20)
380    MID$(SAVE.IT$,1,12) = HEX.FILE$
390    MID$(SAVE.IT$,13,4) = HEX$(TOP)
400    MID$(SAVE.IT$,17,4) = HEX$(START.ADDRESS)
410 '
420 '    Store the 20 bytes of data in the CCP buffer at 80h.
430 '
440    FOR I% = 1 TO 20
450              BYTE = ASC(MID$(SAVE.IT$,I%,1))
460              POKE &H7F + I%,BYTE
470    NEXT I%
480 '
490 '    Set top of memory available to BASIC 1 byte below
500 '    the loading point. CLEAR zeros all variables.
510 '
520    CLEAR,(START.ADDRESS - 1)
530 '
540 '    Recover the name of the HEX file, the top of TPA
550 '    address, and the starting address for loading.
560 '
570    SAVE.IT$ = SPACE$(20)
580 '
590    FOR I% = 1 TO 20
600              MID$(SAVE.IT$,I%,1) = CHR$(PEEK(&H7F + I%))
610    NEXT I%
620 '
630    HEX.FILE$ = MID$(SAVE.IT$,1,12)
640    TOP = VAL("&H" + MID$(SAVE.IT$,13,4))
650    START.ADDRESS = VAL("&H" + MID$(SAVE.IT$,17,4))
660 '
670    BYTE = INSTR(1,HEX.FILE$,CHR$(32))      ' trim blanks off
680    HEX.FILE$ = LEFT$(HEX.FILE$,BYTE - 1)  ' filename
690 '
700 '    Read in the HEX file one record at a time. Break it
710 '    into bytes and POKE them into memory.
720 '
730    PRINT HEX.FILE$;" is being loaded now."
740    OPEN "I",#1,HEX.FILE$
750    BYTE = START.ADDRESS          ' first address to POKE
760 '
770 '    Begin processing each record here.
780 '
790    WHILE NOT EOF(1)   ' as long as there is another record
800 '
810    LINE INPUT#1,A$               ' read a record
820 '
830    A$ = MID$(A$,10,LEN(A$) - 11)  ' just the bytes to POKE
840    COUNT = 1                      ' byte position in record
850 '
860    WHILE COUNT < LEN(A$)      ' while there are bytes
870              B$ = MID$(A$,COUNT,2)     ' get a "text" byte
880              VALUE = VAL("&H" + B$)    ' convert it to hex
```

```
890               POKE BYTE,VALUE
900               COUNT=COUNT+2 ' increment position
910               BYTE=BYTE+1        ' increment address
920      WEND     ' process another byte
930 '
940      WEND     ' loop back to process next record
950 '
960 '     The HEX file has been loaded into memory, now it
970 '     can be CALLed.
980 '
990 '            *** Real application would go here. ***
1000 '
1010     CLOSE 1
1020     PRINT BYTE-START.ADDRESS;"Bytes were loaded."
1030     INPUT "DO YOU WANT TO TRY CALLING THE ROUTINE"; A$
1040     IF A$="Y" THEN CALL START.ADDRESS ELSE GOTO 1110
1050     PRINT:PRINT
1060     PRINT "!!! IF YOU SEE THIS MESSAGE THINGS PROBABLY ";
1070     PRINT "RAN RIGHT !!!"
1080 '
1090 '     Restore top of memory and exit.
1100 '
1110     CLEAR, TOP
1120     PRINT TAB(10);"*** END OF DEMO ***"
1130     END
1140 '
1150 '     Error traps
1160 '
1170     PRINT "THE FILE IS EMPTY"
1180     CLOSE 1
1190     END
1200 '     Missing file
1210     IF ERR <> 53 THEN 1280
1220     PRINT HEX.FILE$;" IS NOT ON THE LOGGED DRIVE."
1230     PRINT "*** READASM SAYS GOODBYE ***"
1240     IF TOP = 0 THEN END
1250     CLEAR, TOP
1260     END
1270 '     All other errors
1280     PRINT "ERROR #";ERR;"OCCURRED IN LINE";ERL
1290     PRINT "*** READASM CAN'T CONTINUE ***"
1300     IF TOP = 0 THEN END
1310     CLEAR, TOP
1320     END
```

BASIC memory to its original contents, and exit gracefully. Line 1040 will call the subroutine. Whether you call the subroutine or not, the program exits via line 1110, which clears memory back up to the bottom of the BDOS. (You may come up a few bytes short since we calculated the address using only the MSB.)

The error traps beginning at line 1170 tell you when something goes wrong. But more important, they restore the top of memory before you exit the program.

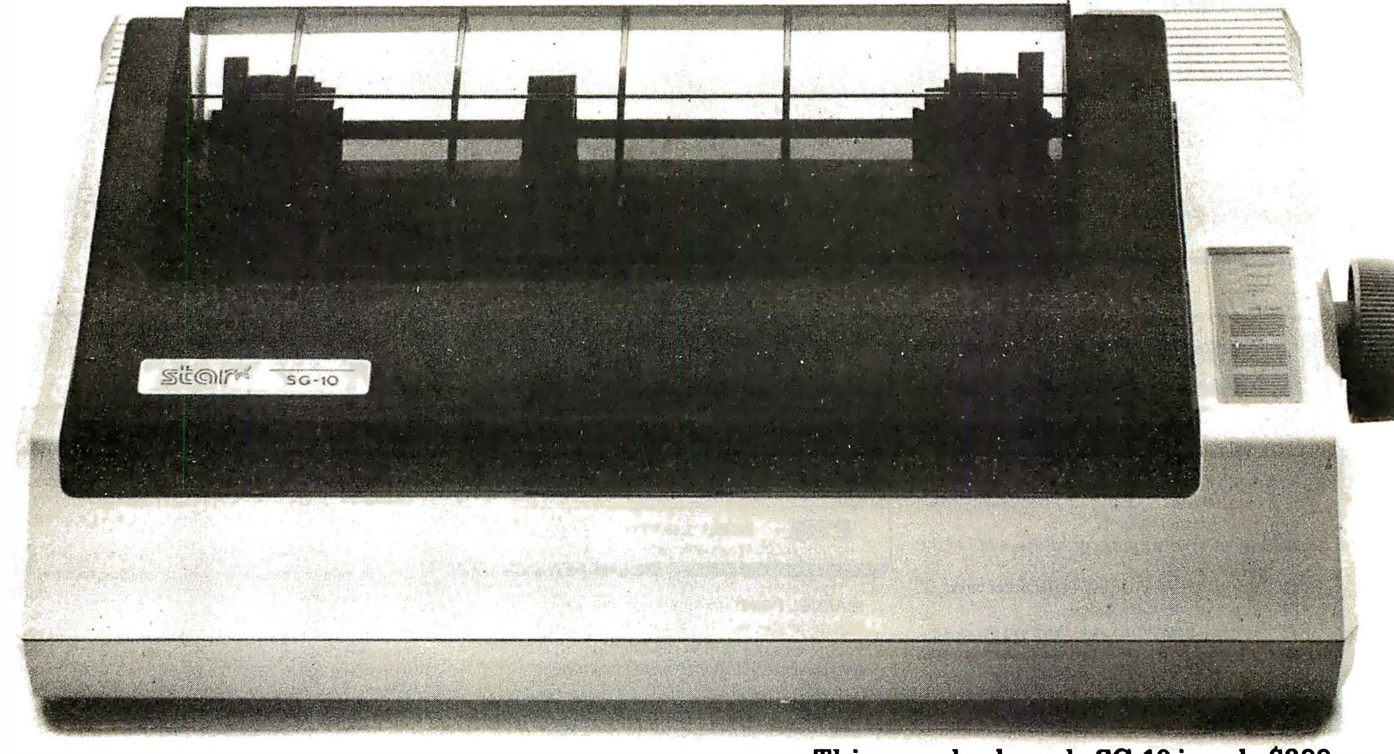
Summary

This article discusses an automated method for loading an assembly-language subroutine into memory where it can be called by a BASIC program, despite the fact that BASIC-80 version 5.x has no specific command to do this. The benefits of this method are simplicity and maintainability for both the calling BASIC program and the assembly-language subroutine. The BASIC program doesn't need to know anything about the subroutine until run time, when it reads the pertinent information from the assembled .HEX file. This provides you with the ability to modify the assembly-language subroutine without affecting the BASIC program that calls it. ■

REFERENCES

1. Hogan, Thom. *Osborne CP/M Users Guide*, 2nd ed. Berkeley, CA: Osborne/McGraw-Hill, 1982.

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sophistication in the manner that past Apple customers have. Hence, there is no reason to widely disseminate technical information to the customers.

The dominant theory in the industry during the last 18 months seems to be that the age of the hacker is over. I belong to this endangered species. I make just enough from software sales to pay for my computer habit. It seems to me that rather than my time being over, I am more important to Apple than at any time in the past. I have bought two Apple IIs in the last six months (the IIc personally and a IIe at work). I am often asked to advise people about what computer to buy.

In the past I have been able to recommend Apple because there was so little likelihood that my friends could possibly outgrow the company. They might become more accomplished hackers than I am, but they could not plumb the depths or exhaust the expansibility of their Apples. Every change in Apple policy that I have observed during the past year has made this less true.

JOHN R. RAINES, M.D.
St. Paul, MN

WHO PAYS FOR COPY PROTECTION?

As a composer of music that incorporates much synthesizer work, I have seen the development of MIDI as a real and practical boon. In my own studio I now use a microcomputer with a Passport MIDI interface (Apple-compatible version) to control Yamaha synthesizers (DX-9 and RX-15).

Frankly, the available software, and most specifically its copy protection, is working against its own benefits.

I use MIDI/4 from Passport as a sequence recorder and player. I would like to use DX-Pro from Yamaha (yes, it works after a fashion on the DX-9) as a patch editor and recorder. A session with both the other day proved unmanageable. Since both are severely copy-protected, to use one right after the other requires a cold boot for each. This takes time and requires powering down the computer. It seems to me that in the real, working world of synthesis it would be sensible if both programs could be copied onto the same disk (or hard drive or RAM disk) and accessed back and forth. Well, copy protection renders this impossible. The Passport software, by the way, comes with a backup disk. The DX-Pro from Yamaha does not! Disks do not hold up well to the rigors of travel, which means that one blown sector and...

There is a legitimate need for protecting the interests of software writers and vendors. However, if this occurs at the expense of the end users in the form of diminished usefulness, it is protecting the interests of no one.

I am frankly not interested in generating a long and philosophical debate on these issues. I am interested in getting my system up and running efficiently so I can get on with making music.

MICHAEL W. GILBERT
Amherst, MA

COMPUTER VS. HUMAN RESPONSIBILITY

The January BYTE editorial ("Autonomous Weapons and Human Responsibility" by Phil Lemmons, page 6) makes the important point that humans are responsible for the acts of their computers, including the act of computer-generated war. In this context, however, your strident attack on Walter Mondale—for his alleged ignorance or demagoguery in opposing "Star Wars" technology—is both surprising and unfair.

Because nuclear weapons in orbit around the earth could more rapidly reach their targets, the time for an offensive or defensive response would be reduced to a very few minutes. (Even if the initial space system is defensive in nature, it is naive to think that the inevitable countermeasure would not be an offensively oriented one.) The potential, then, for contemporaneous human intervention in the response decision—let alone for the somber human reflection most of us would wish for such a fateful decision—is effectively eliminated. In other words, and disregarding the responsibility issue for the moment, the act of making nuclear war from space would of necessity be relegated to computers.

None of this is to say that the computer would be "responsible" for the resulting devastation, a nuclear villain we should fear and abhor. As you stated, "Computers follow sequences of human instructions." But is it ignorant or demagogic to suggest that the nuclear hair trigger not be split to the point where only a computer has the time to effect, or avoid, our annihilation? I think not, and I think this was Mr. Mondale's well-taken point.

At the risk of sounding anticomputer, which I earnestly am not, a further point must be made about the reliability of computers. Computers, including lovingly attended micros and NASA's multi-million-dollar systems, do, at times, screw up. Chips do fail and programs do have bugs. Sometimes the things just shut down; other times, to our horror, they continue to run and produce spurious or confounding results. Sure, humans (designers or engineers or programmers or manufacturers or users) are again responsible. And certainly the politician who, knowing these unfortunate facts of technological life, consigned our fate to such systems could not deny culpability. But, again, is it ignorant or demagogic to oppose entrusting civilization to these all too fragile machines?

I agree that BYTE is not the place, and that neither I nor most BYTE readers are the people, to discuss the technical merits of the "Star Wars" proposal. But, similarly, I don't think BYTE is the place to dismiss concerns about this proposal as senseless computer phobia or worse.

It is ironic and unfortunate that you chose Walter Mondale as the object of your venom. For, indeed, it was Mr. Mondale who suggested that a human being remain directly, consciously, and personally *responsible* for the ultimate human decision. His notion that President Reagan's proposal, which would necessitate that this decision be made by a computer, endangers us is neither frivolous nor an abdication of human responsibility for computer actions. But it is both presumptuous and irresponsible when we, as computer devotees, assume a shrilly defensive posture that fails to acknowledge the limits of our technology or knowledge.

SEAN BLECK
New York, NY

Regarding your January editorial, I believe you have not given Mr. Mondale enough credit.

To make the Strategic Defense Initiative work, enemy missiles would have to be struck within the first five minutes of their launch, thus not leaving enough time to have the President decide whether or not to respond, for reasons I will be happy to detail at your request.

I for one am not ready to change the decision-making process on whether to start shooting at the Russians from a Conference of the President, SAC, and a Congressional Committee to a preprogrammed computer.

How can aerospace programmers "assume responsibility" for the decision that only the President of the United States should make? Even if they're "willing to," I for one am not willing to give them that responsibility, even if you are.

Further, the most brilliant programmers

working 1000 years could not possibly foresee all possible scenarios. Only human judgment has the flexibility to deal with all possible new original situations, at least at the present. A computer may be programmed by human beings, but a computer *is not* a human being. Human beings should use computers to aid calculation, information gathering, and for advice.

They should never turn control of their destiny over to computers, however, no matter how well programmed. In any event, we have not yet amended the Constitution to give aerospace-company programmers and computers the power to declare or initiate war. I for one am not in favor of any move to change it to let such happen.

DON SLAUGHTER
Seattle, WA

A very big WELL DONE to Phil Lemmons for his editorial on "Autonomous Weapons and Human Responsibility."

Phil pointed out that we must take responsibility for our decisions, even if it *appears* that a computer made the decision for us. This is an important lesson for all of us. We must not avoid responsibility for our decisions.

Beyond the specific issue addressed, I was delighted to see BYTE addressing moral and social issues as well as technical ones. During this past century, our technology has leapt far ahead of our morality. Vigorous dialogue in our journals is one good way to help close this gap.

BYRON WEBER-BECKER
Goshen, IN

Having heard Walter Mondale use the word "computer" in an attack on President Reagan, you snapped back a reply without having thought through Mondale's complaint. When liberals do this, it is called a "knee-jerk reaction."

Mondale's point was that for Reagan's "Star Wars" defense plan to work, incoming missiles would have to be shot down before they spew their multiple, independently targeted (MIRVed) nuclear bombs. Thus, there would be only a few minutes between detection, identification, and confirmation of the launch and the time when the decision to attack should be made or not. It would not be feasible to get this information to the president (*any* president) and have her analyze it and make an informed decision in time. The decision would have to be left up to the computers.

Why is this a problem? Not because computers can make mistakes. Perish the thought. (Has a computer really never made a mistake? Are electronic components really infallible?) Rather, human programmers make mistakes. The problem Mondale was pointing to about "Star Wars" (only one of many problems!) is that *programmed* computers make mistakes. Only a computer fanatic would have taken this as an attack on computer hardware as opposed to software.

The mistake you have made is similar to the following: Jane says, "We ought to have tough drunk-driving laws because weaving, lane-hopping cars can do terrible damage." Phyllis (editor of a major automobile magazine) replies, "There she goes again. Cars aren't malevolent. It's the people driving the cars that are at fault." But we all know that. Phyllis has simply missed the point.

(continued)

Finally, it is worth noting that the mistake Phil Lemmons and Phyllis have made is the same mistake made by those who say "Guns don't kill people; people kill people" as if that were disputed by those in favor of rational gun-control laws.

DAVID WEINBERGER
Assistant Professor of Philosophy
Chair, Peace and Conflict
Resolution Studies
Stockton State College
Pomona, NJ

Phil Lemmons replies:
It makes little sense to argue against orbital weapons on the ground that they would have to be controlled by computers. It makes much sense to reject orbital weapons because they put terrible destructive power only minutes from our cities. No control, human or artificial, could make us feel comfortable with devastation constantly poised above. Those who oppose orbital weapons should concentrate on resisting the weapons rather than the control system. Regardless of the components of the control system, humans would bear responsibility, including responsibility for computer malfunctions.

TRAVESTY IN B

My colleagues and I were interested to see the article "A Travesty Generator for Micros" by Hugh Kenner and Joseph O'Rourke (November 1984, page 129), since we've had a similar program running here for a couple of years, written not in Pascal but in the new language B. The interesting thing about the B version of the program is that it is only 24 lines long, compared with the 284 lines of Pascal. Consequently, we thought that other BYTE readers might like to see our version.

B is a very simple language, about as easy to learn as BASIC, but the big difference is that B has very powerful data types, and it's thanks to these that programming in B is so easy.

To understand the program you have to know a little about these data types: B has *texts*, which are strings of characters. For instance, "hello" is a text. There is no character data type; you just use a text of length one, such as "*a*" or "*b*." There are operators on texts: *a*^*b* joins the two texts *a* and *b*, *a*^^*n* repeats the text *a* *n* times, and *a*@*n* gives the tail of text *a* starting at the *n*th character.

B also has *lists*, which are sorted lists of elements. For instance, {"B"; "Pascal"; "Smalltalk"} is a list of texts, as is {"*a*"; "*b*"; "*c*"}, and {"*z*"}. { } is the empty list. You can insert a new element *e* in a list λ with INSERT *e* IN λ. Although lists are kept sorted (alphabetically in the case of texts), the program doesn't use this fact.

The program deals with what the original article calls *n-grams*; that is, groups of *n* letters from a text. The B program works by associating with each group of *n*−1 letters a list of letters that may follow it. Thus, when dealing with trigrams for the sentence "Nonsense imitation can be disconcerting," for the letters "*on*" you get the list {" "; "*c*"; "*s*"}, and for "*ns*" you get {"*e*"; "*e*"}. This association is done using the *table* data type, which is a generalization of arrays; in most other languages, you may index only arrays with integers (or similar), while in B you can use any type. In this program a table called *followers* is used, indexed by texts and giving lists of characters, so that with the above sentence you get followers["*ns*"] = {"*e*"; "*e*"} for instance. You can find out which indexes have been used for a table; "keys followers" gives the list of such indexes. { } is also the empty table.

Another interesting feature of the program is that it is trivial to modify so that it works with *words* instead of characters. For instance, UPDATE would remain identical.

B is an interactive language, and there are implementations for machines with UNIX available at the cost of the media, and shortly for the IBM PC. Anyone who would like to know more about B or its implementations is welcome to write to me.

STEVEN PEMBERTON
B Group
CWI
Postbus 4079
1009 AB Amsterdam
The Netherlands

Listing 1: A *Travesty program in B. The four lines at the bottom were produced from "Mary had a little lamb" as input, using 1-, 2-, 3-, and 4-grams, respectively.*

```
HOW'TO TRAVESTY document USING n GRAMS:
  PUT " "^^(n – 1), { } IN gram, followers
  FOR line IN document: ANALYSE \ Analyse each line in turn
  FOR count IN {1 . . 10}: GENERATE \ 10 lines of imitation
ANALYSE: \ Analyse one line
  FOR char IN line:
    UPDATE followers FOR gram WITH char
    APPEND char TO gram
  UPDATE followers FOR gram WITH " " \ Treat line end as space
  APPEND " " TO gram
GENERATE: \ Generate one line
  PUT 0 IN length
  CHOOSE gram FROM keys followers \ Choose a random start
  WHILE gram in keys followers AND (length<50 OR char<>" "):
    CHOOSE char FROM followers[gram]
    WRITE char
    PUT length+1 IN length
    APPEND char TO gram
  WRITE / \ Write a newline

HOW'TO UPDATE followers FOR gram WITH char:
  IF gram not'in keys followers: PUT { } IN followers[gram]
  INSERT char IN followers[gram]

HOW'TO APPEND char TO gram:
  PUT (gram^char)@2 IN gram

1: nhwaso ldm r ttvncd vetsvaen ryam wnMhuaaiaa lryulitlab
2: evere Mad ad ts go Mamb snts s s ad lamb flits it
3: ry hat Marywhery was was fleece that lamb ittleece
4: te as snow and everywhere that lamb was white as white
```

CIRCUIT-BOARD CATASTROPHE

I have become the victim of an event, totally beyond my control, that has nothing less than shut down my computer services.

I own an LNW Model II microcomputer—a powerful work-alike of the TRS-80 Models 1 and 3. In late June of this year my expansion board developed a problem, rendering the facilities on the board useless. This system-expansion circuit board includes half of the system memory, serial and parallel interfaces, floppy-disk controller, and clock circuits. Because the problem (I suspected the floppy-disk controller) developed and was reported less than one year after purchase, the computer was still covered by warranty.

On July 7, 1984, after telephoning LNW Research, I was given a "return authorization number." As instructed by Technical Services at LNW Research, removing the factory-built expansion board from the computer unit would not void my warranty. I then removed the circuit board, as instructed, and had it packaged and shipped to LNW Research via United Parcel Service. The "return authorization number" was clearly labeled on the package and also taped directly onto the circuit board.

After about 10 days and several follow-up telephone calls, LNW finally acknowledged receipt of my circuit board. I made repeated telephone inquiries (never receiving a reply) after that to check on the progress of the repair. Finally, after amassing a rather large telephone bill, about 2½ weeks ago I was told, rather unwillingly, that my expansion board had not been touched. I was also told that many of LNW's repair technicians had been on vacation and that repairs on units under warranty were backlogged. I was asked to call back in two to three weeks, or if I wanted my circuit board sent to Wilson Technical Services. Mr. Wilson, I was told, had formerly been employed by LNW Research and was doing part of LNW's warranty repair work. I elected to leave the circuit board with LNW.

After a two-week wait, I tried contacting LNW by telephone again but received no answer. I then called Wilson Technical Services and was told that LNW had gone out of business! All of LNW's warranty work, I was told, had been turned over to Wilson Technical Services. My expansion board, however, was not on the list of units turned over to them. Wilson Technical Services said that it would check further. I telephoned Wilson Technical Services again, and the woman to whom I spoke before confirmed that my expansion board was not on the list of units turned over to Wilson Technical Services.

No person seems to know the present location of my essential and relatively expensive circuit board. I, therefore, have found it necessary to contact the Attorney General's office of the State of California to begin proceedings against Wilson Technical Services and LNW Research (if it can be located). This is in addition to contacting all magazines and users groups that I can think of. I am also contacting the Better Business Bureau and the Chamber of Commerce of Tustin, California.

I am not the only LNW 80 computer owner involved in this aggravating situation. Wilson Technical Services informed me that I am only one of several in the same predicament. So here I sit, out of business, awaiting the outcome of due process.

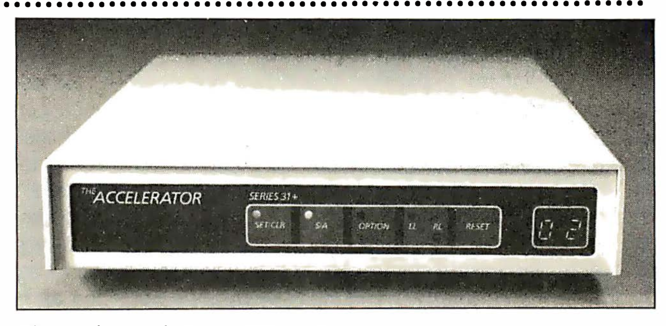
Jeffrey W. Cox
New Albany, IN

PERIPHERALS

Data-Compression Unit

The Accelerator Series 31 asynchronous data-compression unit from Telebyte can be installed in existing networks. The Accelerator provides 3-to-1 data acceleration and supports synchronous and asynchronous modems. It can handle terminal data rates up to 9600 bits per second and modem data rates up to 2400 bps.

During operation, encoded bit strings are transmitted between Accelerator units using a modified X.25 protocol. This method limits data errors and increases data security. Also, you can improve security by assigning a four-digit Network Security Code to each Accelerator in the network.



The Accelerator data-compression unit.

The Accelerator's front panel includes touch-sensitive keys, status lamps, and display digits so you can program permanent options from the front panel. The unit contains no internal DIP switches or jumpers.

Prices for the Accelerator Series 31 products range from $695 for a unit with a data-compression ratio of 2 to 1 and a modem data rate of 1200 bps to $1095 for the maximum configuration with a data-compression ratio of 3 to 1 and a modem data rate of 2400 bps. For more details, contact Telebyte Corp., 215 Oak St., Natick, MA 01760, (617) 653-3995.
Inquiry 615.

Mac Hard-Disk Drives

Davong supplies multiple-volume hard-disk drives for the Macintosh with four amounts of storage: 10, 21, 32, and 43 megabytes. Mac Disks are partitioned into two volumes and initialized when shipped. Each disk-drive system features Davong's Volume Manager software.

Average Mac Disk access time is 100 milliseconds with the 10- and 21-megabyte systems and 40 milliseconds with the 32- and 43-megabyte models. Mac Disk connects to either RS-422 port on the Macintosh.


Davong's Mac Disk hard-disk drive.

The Volume Manager program lets you add, delete, and activate volumes. It also can gather free space on Mac Disk so you can compress space to create an additional volume. This release of the software lets you connect Mac Disk to the Macintosh's modem or printer port for use in telecommunications.

Prices for the Mac Disk line depend on amount of storage: $1950 for 10 megabytes, $2795 for 21 megabytes, $3395 for 32 megabytes, and $3995 for 43 megabytes. For complete details, contact Davong Systems Inc., 217 Humboldt Court, Sunnyvale, CA 94089, (408) 734-4900.
Inquiry 617.

Hard-Disk System for the AT

Internal hard-disk drives specially designed for the IBM PC AT are available in 20-, 33-, and 117-megabyte models from PC's Limited. The disk-drive systems are compatible with DOS 3.0 and 3.1.

The full-height 5¼-inch hard-disk drives run off the IBM-installed PC AT controller. The units come complete with the necessary cables and mounting hardware, and they install easily, dropping directly into the existing PC AT box.

Prices for the hard-disk drives are $795 for the 20-megabyte model, $1195 for 33 megabytes, and $3995 for 117 megabytes. For further information, contact PC's Ltd., 7801 North Lamar #E-200, Austin, TX 78752, (512) 452-0323.
Inquiry 616.

PCjr Numeric Data-Entry Pad

Key Tronic's numeric data-entry pad for the IBM PCjr includes all mathematic function keys. It also features cursor-control, Tab, Backspace, and Enter keys. The user can convert the numeric pad to the function mode without returning to the PCjr keyboard. The keypad facilitates efficient data entry for number-intensive applications such as spreadsheets and accounting systems.

Suggested manufacturer's retail price for the IBM PCjr numeric keypad (model KB 5149jr) is $99.95. For more information, contact Key Tronic Corp., POB 14687, Spokane, WA 99214, (800) 262-6006; in Washington, (509) 928-8000.
Inquiry 618.

PERIPHERALS

3Server Network Server

A dedicated multifunction network server is available from 3Com. You can use 3Server with 3Com's Ethernet-based EtherSeries network products to combine personal computers and host systems in a local-area network (LAN). 3Server also supports communications over telephone lines for electronic mail and direct communication with IBM mainframes using SNA protocols.

The 3Server can accommodate up to 50 individuals in a network. It uses the Intel 80186 and the 82586 Ethernet controller with a 36-megabyte (formatted capacity) fixed-disk drive.

You can add a tape backup unit of 60 megabytes to the 3Server. You can also use up to six external disk-drive modules to expand disk storage to more than 250 megabytes per 3Server.

Suggested retail price for the 3Server is $7495. Add-on 36-megabyte disk drives cost $3995 each, and the 60-megabyte tape backup unit costs $2995. A $995 384K-byte memory option for expansion of disk cache will bring total memory to 896K bytes.

EtherShare, a 3Server software package that provides shared disk capabilities, costs $695. EtherPrint, a shared printing program, sells for $395, and EtherMail gives you electronic-mail capability for $995. Contact 3Com Corp., 1365 Shorebird Way, POB 7390, Mountain View, CA 94039, (415) 961-9602.
Inquiry 619.

ADD-INS

Memory Upgrade for the Mac

MicroGraphic Images has released the MegaMac, a memory upgrade for Apple's Macintosh. MegaMac hardware provides 1024K bytes of memory, partitioned into two sections: 512K bytes of core memory and 512K bytes used as a RAM disk.

Reportedly, the MegaRAM software package sold with the upgrade board lets you load any file or application program from the RAM disk into the core memory three to six times faster than from a disk drive.

The suggested retail price for the MegaMac upgrade board is $1395. (You must return the Macintosh's original 128K-byte motherboard to MicroGraphic Images.) The price for a complete 1024K-byte system including the Macintosh computer is $3495. For further technical information, contact MicroGraphic Images Corporation, 19612 Kingsbury Street, Chatsworth, CA 91311, (818) 368-3482.
Inquiry 620.

IBM PC UNIX Coprocessor

The Opus516 Personal Mainframe is a UNIX coprocessor subsystem that converts an IBM PC or plug-compatible to a 32-bit UNIX workstation. Opus516 consists of a complete port of AT&T UNIX System V (release 2.0) and a 32-bit coprocessor.

The UNIX coprocessor is based on National Semiconductor's 32016 processor and includes the 32082 memory-management unit and 32081 floating-point unit. On-board memory is expandable to 2 megabytes. Included with UNIX System V and its utilities are C and FORTRAN-77 compilers, an assembler, and a debugger. Opus516 supports UNIX and PC-DOS.

In OEM quantities, a 1-megabyte configuration is $3140 with a single-user object license. Multiuser licensing is available as an option. Contact Opus Systems, Suite 120, 960 San Antonio Rd., Los Altos, CA 94022, (415) 941-7201.
Inquiry 621.

Multiuser Database Environment

Sentinel Computer's SMX for the IBM PC, XT, or AT is a combination of a four-channel serial-interface board and a multiuser executive software package. Its multiuser database-oriented operating environment accommodates up to five terminals and five printers.

The interface board for SMX uses standard RS-232C serial ports. It supports port speeds ranging from 300 to 9600 bps.

The SMX-Executive software is menu-driven and has a help facility. It includes an integrated database manager, interactive on-line operations, multitasking, virtual memory, a print spooler, and multiple language/character capability.

SMX sells for $1495. For further details, contact Sentinel Computer Corporation, 9902 Carver Rd., Cincinnati, OH 45242, (513) 984-6622.
Inquiry 622.

RAM Card for the Chameleon

An expansion board for the Chameleon and Chameleon Plus portable is available from Seequa Computer. The Chameleon RAM Plus Card comes with 128K, 256K, or 384K bytes of RAM. The 384K-byte version gives you 640K bytes of total RAM, the maximum on the Chameleon or Chameleon Plus.

The Chameleon RAM Plus Card comes standard with a real-time clock and a print spooler. It lets you create a RAM disk as a third disk drive. The card requires DOS 2.0 and 256K bytes of RAM resident on the main logic board.

Prices for the Chameleon RAM Plus Card are $395 for the 128K-byte version, $595 for 256K bytes, and $795 for 384K bytes. For complete product specifications, contact Seequa Computer Corp., 8305 Telegraph Rd., Odenton, MD 21113, (301) 672-3600.
Inquiry 623.

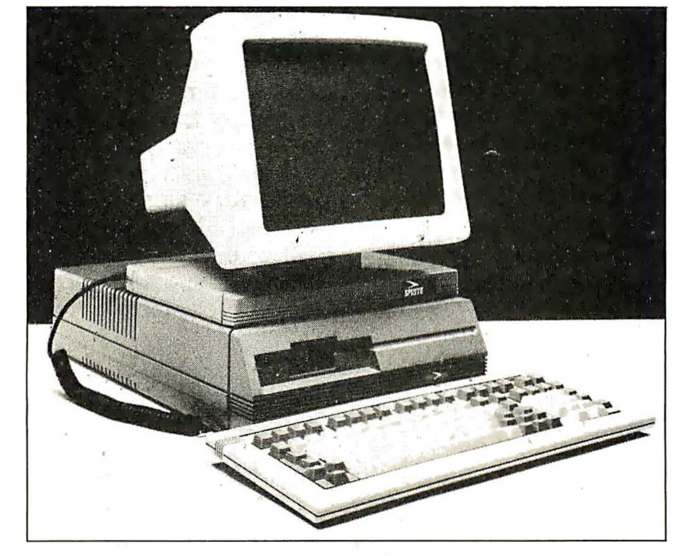
(continued)

NEW SYSTEMS

Sprite, a Multiuser System, Features the 80286

Jarogate Limited's Sprite is a multiuser microcomputer designed with Intel's 6-MHz 80286 microprocessor and featuring Digital Research's Concurrent CP/M 3.1 on its main processor and CP/M Plus on a slave. Ethernet capabilities are built in. Standard system hardware is made up of a 5¼-inch 790K-byte floppy-disk drive, a 21-megabyte hard disk, and a five-slot S-100 bus.

Sprite, which comes with a keyboard and a high-resolution green or amber monitor mounted on a tilt-and-swivel base, has its central processor, an interrupt controller, two serial and three parallel I/O bidirectional ports, and a socket for an optional 80287 mathematics coprocessor on its main printed-circuit board. Its serial ports have full handshaking and can operate at speeds of up to 38,400 bps. S-100 support logic and connectors for memory boards also reside on the main PCB.



Jarogate's Sprite has built-in Ethernet capabilities.

Sixty-four dynamic RAM chips of either 64,000 or 256,000 bits can be installed on the Sprite's memory boards, thereby offering RAM capacities ranging from 512K bytes to 2 megabytes. An 8027 memory-management unit polices operations while providing automatic refresh and full-speed memory access without wait states. The standard Sprite chassis can accommodate 6 megabytes of RAM.

The OWI, or outside world interface, board carries out high-speed disk I/O for the Sprite. The OWI board has a 6-MHz Z80B, 256K bytes of RAM, a hard- and floppy-disk controller, DMA, and the Ethernet controller with support logic and battery-backed real-time clock. The disk controller gives you a SASI (Shugart Associates Standard Interface) connection for your drives, and the RAM serves as an I/O buffer and cache memory.

The basic Sprite has two RS-232C serial ports for a pair of workers, and additional ports will expand Sprite for as many as 18 employees. Such options as IBM PC-compatible color graphics and an 8-port I/O board can be purchased. Many specialized S-100 boards from third-party vendors reportedly work with Sprite. UNIX System V and Concurrent DOS IV are planned.

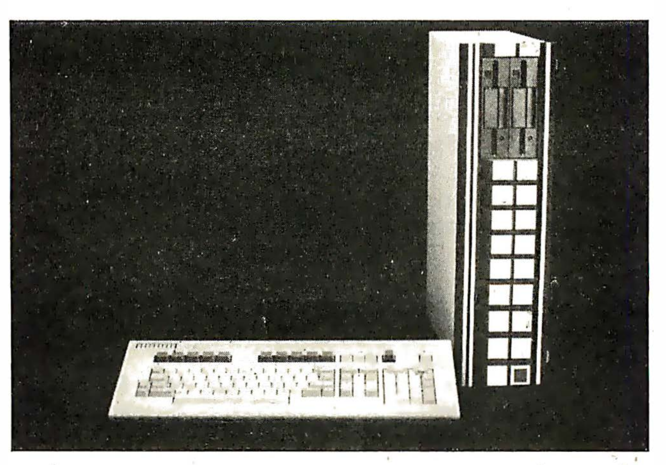
Pricing for the Sprite was unavailable at press time. For further information, contact Jarogate Ltd., 197-213 Lyham Rd., Brixton, London, SW2 5PY, England; tel: 01-671 6321; Telex: 8950094 JARO G.

Inquiry 624.

68000 Micros from England

U-Microcomputers, Warrington, England, has launched a line of microcomputers built on the 32-/16-bit 68000 microprocessor. The U-Man Series 1000 is centered around a basic 128K-byte microcomputer that features on-board RAM expansion to 1 megabyte, dual 800K-byte floppy-disk drives, monochrome and RGB outputs, and a 97-key keyboard.

Graphics resolution is said to be 270 and 680 pixels, depending upon operating mode and configuration. External connections comprise a pair of serial ports, a Centronics parallel port, a general-purpose 16-bit outlet, and a 10-bit A/D jack for joysticks. The U-Man Series 1000 also has a speech synthesizer, sound generator, and a 6809 chip to supervise I/O operation.



The Series 1000 can handle up to 1 megabyte of RAM.

Two operating systems, CP/M-68K and UCSD p-System, are offered. With CP/M-86K, the U-Man Series 1000 will support Digital Research's CBASIC, Pascal MT+, C, and 68000 assembler packages as well as SVC FORTRAN and Cambridge LISP. Pascal, BASIC, FORTRAN, and 68000 assembler work with the p-System.

A hard-disk option will be available. Pricing for the U-Man Series 1000 begins at £2499. Contact U-Microcomputers Ltd., Winstanley Industrial Estate, Long Lane, Warrington, Cheshire WA2 8PR, England; tel: (0925) 54117; Telex: 629279 UMICRO G.

Inquiry 625.

NEW SYSTEMS

HP 260: Line of Small Business Computers

Hewlett-Packard's HP 260 family of multiuser, small-business computers is presently made up of three models, the 15, 24, and 55. The Model 260 family, whose introduction represents the next step in the evolution of HP's Model 250 microcomputer, is fully compatible with hardware and software created for its primogenitor. It can handle HP plotters and the ThinkJet and LaserJet printers. The manufacturer says that the HP 260 is its first computer, other than its personal computers, to support these printers.

All units measure 29 inches tall, 15 inches wide, and 28½ inches deep. A 14-inch monitor and a keyboard are supported as a workstation alternative.

The entry-level HP 260 Model 15 has 256K bytes of RAM, a 15-megabyte hard-disk drive, and a 3½-inch microfloppy-disk drive. It lists for $10,500.

With 512K bytes of RAM, a 24-megabyte hard disk, and streaming-tape backup, the Model 24 can be expanded to provide 190 megabytes of disk storage. Pricing begins at $16,300.

The top-of-the-line Model 55 can be enhanced to support as many as 18 users. It comes with the same amount of RAM as the Model 24, a streaming-tape backup, and 55 megabytes of hard-disk storage. The Model 55 begins at $20,500.

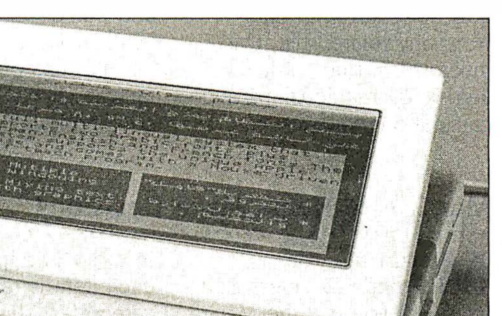
For more information, contact your local Hewlett-Packard sales office.
Inquiry **626**.

SOFTWARE • APPLE

Mix Arabic, English, and Graphics on IIc

A multilingual word-processing system for the Apple IIc has been created through the joint efforts of DIWAN Science and Information Technology and Attar Computers Limited. The system uses the IIc's bit-mapped display to print Arabic and English text in either high resolution (40 columns) or double high resolution (80 columns).

Supplied utility programs let you mix high-resolution graphics with text. Graphics can also be manipulated and enhanced with Apple's Mousepaint program. Arabic and English texts can have independent windows, each of which supports independent scrolling.


Windows, English, and Arabic displayed on the IIc.

This word processor supports two Arabic fonts as well as English, French, and German fonts. It's supplied with both Arabic fonts and the English font, a bilingual notepad program, an address program, and Imagewriter bilingual driver rouines. The Arabic text supports full vowel points and fully conforms with the ASMO 449 standard.

The word processor is £295. Contact DIWAN Science and Information Technology, London House, 271 King St., London W6 9LZ, England; tel: (01) 741 8011; Telex: 261507 MONREF G (quote reference number 2785).
Inquiry **627**.

Personal Income Planning Set

A set of programs for the Apple IIc and IIe, Plan Ahead comprises applications that help you plan your retirement income, life-insurance coverage, and college-fund savings. Published by Advanced Financial Planning, Plan Ahead modules are designed to work alone or in conjunction with one another.

Each module lets you account for inflation and print out its various components, such as budget statements and year-by-year itemizations. Financial data can be swapped between modules, all of which are menu-driven and fully documented.

The Retirement Planning module helps you create a total retirement plan in light of your particular circumstances. It details the inflation rate applicable to your budget, the funds that will be required at retirement, the amount of your retirement fund covered by your current assets, and other data. This program can analyze your plan, determine if changes are necessary, and suggest where changes might be made.

Life Insurance Planning aids in the determination of the amount of insurance needed to provide for your family in the event of your sudden death. It considers such expenses as daily living, college fees, and funeral charges and ciphers them with hoped-for income from Social Security, current assets, and the projected income of your spouse.

College Funding calculates savings in two ways: lump-sum investment in the first year or yearly amounts to accumulate the necessary funds.

Single modules are $29.95. Two together are $49.95, and the entire set is $59.95. Contact Advanced Financial Planning, 20922 Paseo Olma, El Toro, CA 92630.
Inquiry **628**.

(continued)

SOFTWARE • APPLE

Compiled Logo Runs on Mac

A compiled version of the Logo language, ExperTelligence's ExperLogo is available for Apple's Macintosh microcomputer. ExperLogo uses the Mac's user-interface conventions and has been enhanced with such features as array processing and data-file handling. The publisher says that it is the only compiled version of Logo available and that it is the first Logo to process items and lists using arrays.

ExperLogo's turtle graphics reportedly operate at speeds up to 100 times faster than that of other Logos. Its Bunny Graphics feature gives you bunnies that move about the screen in three-dimensional space. The bunnies respond to such navigation commands as yaw, roll, and pitch, and they can reside in cubes and spheres.

Its data-file handling abilities lets ExperLogo programs create and read their own files. Programs can be accessed from other applications through the Mac's standard text and graphic interfaces. A few of the list-processing features are said to be adapted from LISP.

ExperLogo programs are not limited to 128K bytes of RAM because of a feature known as load-on-call. This means that procedures are stored on disk and automatically loaded when called if they are not already present in memory.

The suggested retail price is $149.95. A French version of ExperLogo is available. Contact ExperTelligence Inc., 559 San Ysidro Rd., Santa Barbara, CA 93108, (805) 969-7874.
Inquiry 629.

Full Database Lets You Customize Applications

Helix, a data-based information-management and decision-support system, gives your Apple Macintosh full database capabilities and allows you to customize applications development. This program performs traditional database-management tasks, such as filing, sorting, and data retrieval, yet it can be used for complex data analyses and task modeling.

Helix lets you devise your own task-specific applications. Data needs only to be entered once for use with a variety of jobs, and database structures are easily modifiable. Helix works with both text and numbers.

The Helix user interface employs icons for each of its functional operations. You can link the icons together in a flowchart with data from any related file. This gives you a quick way of setting up relationships and calculations that you can tailor to specific applications. All the Mac's user-interface conventions, including the mouse, windows, and pull-down menus, are used by Helix.

Helix runs on 512K-byte Macintoshes and Lisas equipped with an external disk drive or a hard disk. With a demonstration disk and tape, sample applications, and manual, Helix is $395. Contact Odesta Corp., 3186 Doolittle Dr., Northbrook, IL 60062, (312) 498-5615.
Inquiry 630.

MacChoice Helps Make Decisions

MacChoice from Superex Business Software lets you use the Macintosh for making comparisons. MacChoice lets you compare and rate two, three, or four items simultaneously using as many as 20 categories. Categories are listed in order of importance, and each item is rated by its categories. This program tabulates each individual item's ratings and displays the results in a bar graph. The chart provides a visual representation of each item's ratings, which simplifies your decision-making process.

MacChoice costs $49.95. For more information, contact Superex Business Software, 151 Ludlow St., Yonkers, NY 10705, (800) 862-8800; in New York, (914) 964-5200.
Inquiry 631.

SOFTWARE • IBM PC

Database Manager for Applications Development

A database-management system designed for applications development, Progress is intended to replace traditional languages and the development methods built around them. The system consists of five key components: a data dictionary, an application language, a screen and report formatter, a procedure editor, and a relational database manager.

The Progress language has a library of operators and functions, including square root, logarithm, concatenation, and string-matching operations. The syntax-checking editor positions the cursor on the incorrect word or phrase, and a help facility provides error explanations and access to definitions in the data dictionary.

The relational database manager supports databases of more than 5 billion bytes, and up to 1000 files and indexes can exist in each database. Each record can contain an unlimited number of fields within a maximum record size of 2000 bytes. Because all fields occupy only the number of bytes needed to hold the data, the vendor said, storage requirements on disk are generally reduced 30 to 60 percent.

Progress for the IBM PC costs $695; versions for UNIX machines range from $2450 to $4450. For more information, contact Data Language Corp., 5 Andover Rd., Billerica, MA 01821, (617) 663-5000.
Inquiry 632.

SOFTWARE • IBM PC

Have a Talk with Your Computer

Racter is a program that engages in conversation ranging from serious discussion to small talk. The program also tells jokes and stories and can recall and refer to conversations it has had. (Racter is reportedly the first program to author a book. *The Policeman's Beard Is Half Constructed*, published by Warner Books last year, is a collection of stories, poems, essays, and limericks created by Racter.)

According to the developers, Racter never repeats itself because, unlike programs like Eliza, it contains no stock responses and has its own "eccentric personality." The vendor touts the program as a mix of educational and entertainment software and notes that Racter is being used as a tool to sharpen the interviewing skills of psychiatric interns. No technical knowledge is needed to use the program.

For the IBM PC and compatibles, Racter is $69.95. Apple and Commodore versions are in the works. Contact John D. Owens Associates Inc., 12 Schubert St., Staten Island, NY 10305-2999, (718) 448-6283.
Inquiry 633.

Large Print for the Visually Impaired

Computer DiskCourse has developed several programs for people with poor vision. Lyon Large Print is a screen-review package that provides nine print sizes, three space settings, and, on color machines, 16 foreground and background colors for applications software running on the IBM PC and compatibles. You can generate large-print hard copy with an IBM dot-matrix printer. Lyon Large Print is designed to work with other packages for the visually impaired, including the PC Talking Program. The software costs $490 and includes a text editor; a demo disk costs $20.

WordLyon is a specially configured large-print version of WordStar. Letters range in height from 2 to 4½ inches. The program costs $150.

LargeLotus, an interactive large-print driver for Lotus 1-2-3, costs $200.

The company will customize other software to work in large-print format. Contact Computer DiskCourse, 4546 John St., Vancouver, British Columbia V5V 3X2, Canada, (604) 876-1287.
Inquiry 634.

SOFTWARE • CP/M/MS-DOS

Three for Digital Research Products

CBC Tools is a function library for use with Digital Research's CBASIC compiler. It has more than 100 functions to perform string manipulation, sorting, radix conversion, bit and byte manipulation, and interfacing with the operating system. Most of the program was written in assembly language; you can develop libraries of your own in compiled CBASIC. CBC Tools is available for CP/M-80 and CP/M-86 at a price of $100 (plus $5 for shipping).

CBCXREF is a cross-reference utility for the CBASIC compiler. Its user options let you set page length and width and sort output. The utility can find unreferenced variables and labels and identify unused variables and labels. CBCXREF is available for CP/M-80 and CP/M-86 at a price of $80 (plus $3 shipping).

MBPASLIB is a replacement library for PASLIB (used with Pascal MT+). According to the vendor, programs using MBPASLIB are typically 4K to 5K bytes smaller and up to 100 percent faster than those using PASLIB. The library is available for CP/M-80 and costs $75 (plus $3 shipping). Contact Minnow Bear Computers, POB 2233, Station A, Champaign, IL 61820-8233, (217) 398-6883.
Inquiry 635.

Artificial Intelligence at Home

Dynamic Master Systems has developed an AI programming system for CP/M and MS-DOS environments that gives home computer users the tools to create their own expert systems. TOPSI is a native-code version of OPS-5, a high-order language for development of expert programs. To make TOPSI efficient on its microprocessor hosts, DMS has added several enhancements to the OPS-5 language definition and placed a few restrictions on the sizes of data structures.

TOPSI, which costs $75 (plus $5 shipping), is available for most Z80 CP/M systems with 65K-byte memory and most IBM PC-compatibles with at least 128K bytes. Contact Dynamic Master Systems Inc., POB 566456, Atlanta, GA 30356, (404) 565-0771.
Inquiry 636.

Business-Applications Language

A high-level language for business applications, Lucid is reportedly easier to learn and use than conventional programming languages because it has special business features and a database system built in. Functions include data conversion, string manipulation, form input, screen handling, report generation, and math operations. Programmers can define their own functions, and the language supports all C statements except GOTO.

Lucid can read dBASE files directly. It can access data from Framework, Symphony, Lotus 1-2-3, and all spreadsheets.

A version for the IBM PC and compatibles sells for $295. UNIX and XENIX versions are available under OEM and licensing agreements. Contact Lucid Software Corp., 3080 Valmont Rd., Boulder, CO 80301, (303) 442-4981.
Inquiry 637.

(continued)

SOFTWARE • CP/M/MS-DOS

Database Management System

Datamaster is an information system designed to provide on-line information retrieval and update of single or multiple database sources. Through its modules and submodules, you can make or modify a record structure or a data-screen entry and generate reports to your specifications.

The program allows mixed fields on the same screen from a single or multiple database. You can retrieve relative information from one or several databases and update one or more databases from the same screen. You can also link screens from one to another; the vendor claims there is no limit to the number of screens you can link.

Datamaster operates on most computers running under CP/M, MP/M, MS-DOS, TurboDOS, ITT-DOS, and Oasis. Suggested retail price is $495. Contact C.D.A. International Software Corp., Suite 330, 14900 Ventura Blvd., Sherman Oaks, CA 91403, (818) 986-3233.
Inquiry 638.

Half-Duplex Communications

Intended primarily for use with the existing radio telephone network, HCOM is a half-duplex communications package for PC-DOS, MS-DOS, and CP/M-80 systems. The program provides all the logic necessary to support CRC 16 error checking, half-duplex link control, and user-configurable help screens and menus. Remote-site or mobile users can log on to any HCOM system and send or receive files.

HCOM can also be used in full-duplex mode and still support all the services provided in half-duplex mode. Additionally, it can be used as a terminal emulator to access bulletin-board systems or other non-HCOM systems. XON/XOFF protocol is supported. On dedicated links, HCOM operates at up to 9600 bps.

The software costs $425 (Canadian). The AT&T 202-compatible modem, the CD-2, sells for $625. Contact Crafield Digital, 107 Abadan Crescent NE, Calgary, Alberta T2A 6P1, Canada, (403) 273-9738.
Inquiry 639.

SOFTWARE • OTHER COMPUTERS

Screen Dump from MBC 550

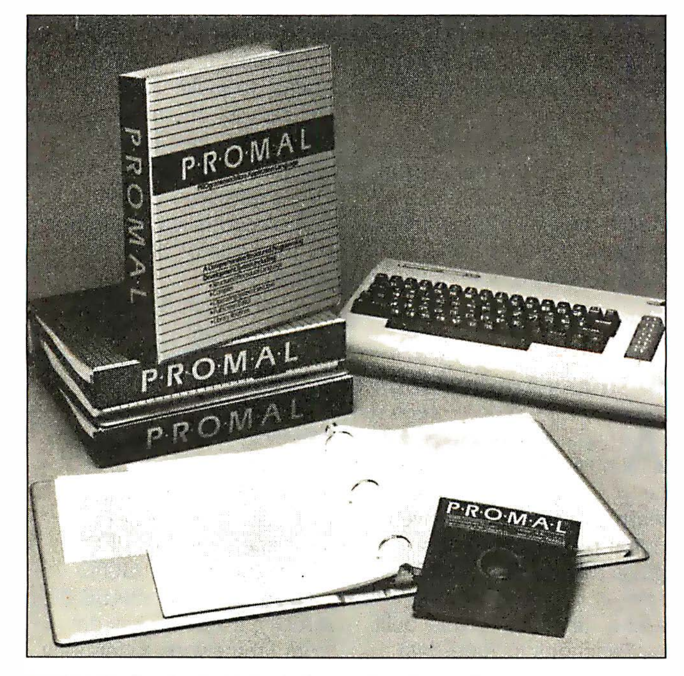
Snapshot allows Sanyo MBC 550 screen dumps at any time. It also lets you zoom in on smaller areas of the screen. It has three operating modes: character, color graphics, and high-resolution black-and-white graphics. The character mode can be used for fast printing of screen data; the color-graphics mode prints a side view of the screen with colors shown as distinguishable dot patterns.

Snapshot works with any dot-matrix printer with graphic capabilities and a parallel port. Horizontal and vertical scaling, color-to-dot pattern representation, and the keystrokes used to invoke its operations can be modified. Snapshot is preconfigured for various printers. It runs on versions of MS-DOS that occupy under 2.5K bytes of main memory. It costs $34.95, plus $1 shipping. Contact Key Software Products, 440 Ninth Ave., Menlo Park, CA 94025, (415) 364-9847.
Inquiry 640.

Structured Programming Language Released for Commodore

A high-level, structured programming language similar to C and Pascal, PROMAL runs on the Commodore 64. Systems Management Associates says that PROMAL's fast compiler and a highly efficient run-time environment let you write applications for the Commodore 64 in a high-level language, where once such programs had to be written in assembly language.

PROMAL (Programmer's Micro Applications Language) comes with a one-pass compiler, a full-screen editor, a command executive, and a library of predefined utilities. The PROMAL executive provides file, memory, and program management as well as I/O redirection. A full-screen, cursor-driven editor helps you enter and edit your source program rapidly.



PROMAL *for the* C-64 *is similar to* C *and* Pascal.

The library of machine-language subroutines supports the PROMAL run-time environment with optimized routines for file I/O, string handling, formatted output, and data conversion. Benchmarks that reportedly show PROMAL to be from 70 to 200 percent faster than BASIC, COMAL, FORTH, and Pascal are available from the manufacturer.

PROMAL is $49.95 factory-direct. A developer's version with an umlimited run-time distribution license is $99.95. Contact Systems Management Associates, 3700 Computer Dr., POB 20025, Raleigh, NC 27619, (919) 787-7703.
Inquiry 641.

SOFTWARE • OTHER COMPUTERS

Communications Software for Portable

Geneva Connection is a ROM-cartridge telecommunications program that lets users of Epson's Geneva portable computer communicate directly with external storage units or by modem with other computers. It can handle communications with remote computers by means of add-on or external modems and through acoustic couplers. Data can also be sent or retrieved from a floppy disk, RAM disk, or microcassette.

Geneva Connection offers two means of transferring files: XON/XOFF flow control and a block protocol with error detection and correction. It works with either pulse or tone dialing and is capable of automatic dialing.

Other features are English-language command structures, automatic-answer capability for preset time periods, full range of communication speeds, and selective filtering and replacement of characters for such applications as file transfers between word processors.

The retail price for the Geneva Connection is $79. Contact Epson America, 2780 Lomita Blvd., Torrance, CA 90505, (213) 539-9140. **Inquiry 642.**



Geneva Connection is a communications package for the Epson portable.

Utilities for LaserJet

JetSet, a pair of utilities for Hewlett-Packard's LaserJet printer, runs on the HP 150 touch-screen computer, the IBM PC, and PC-compatibles. Both utilities interface transparently with each other and can be used with any text editor or word processor.

SetLaser, the first utility, executes a string of commands that initialize the LaserJet and direct its output to the communications port. It provides access to the LaserJet's formatting capabilities, including typefaces, lines per inch, number of copies, and page length. Multiple formats can be saved for use with different documents.

The second utility is Runoff. It lets you set tab stops, margins, and page feeds from within the document being printed. It can be used for generating headers, footers, and page numbers and underlining portions of text.

JetSet is $79. Contact Datamate Co., Suite 128, 4135 South 100 East Ave., Tulsa, OK 74146, (800) 262-7276; in Oklahoma, (918) 664-7276. **Inquiry 644.**

CP/M Plus for Cromemcos

Super Bios Plus is a revised version of CP/M Plus for Cromemco computers said to incorporate a memory-management method that uses interbank memory moves and banking of disk drivers to achieve a 60K-byte program area. Its file system features hashed directory access, record buffering, and multisectored disk I/O.

Super Bios Plus is upward-compatible with CP/M 2.2 for applications programming, and it supports up to 16 hard disks.

Console I/O redirection utilities are available for applications programming transparency. Extended system utilities include programs that list file directories and transfer files. A batch facility is provided.

A CDOS emulator for running Cromemco software under CP/M and MP/M. Expand is a supplied system extension. Super BIOS Plus also incorporates a component that allows Cromemcos to read data disks created on the IBM PC.

Super BIOS Plus with Expand costs $375. It supports single- or double-sided, single- or double-density 5¼- and 8-inch disks. Source code and copy and disk-formatting programs are supplied. Contact Micro Applications & Hardware, 15 Princess St., Sausalito, CA 94965, (415) 331-6422; east of the Rockies, (314) 434-1896. **Inquiry 643.**

WHERE DO NEW PRODUCT ITEMS COME FROM?
The new products listed in this section of BYTE *are chosen from the thousands of press releases, letters, and telephone calls we receive each month from manufacturers, distributors, designers, and readers. The basic criteria for selection for publication are: (a) does a product match our readers' interests? and (b) is it new or is it simply a reintroduction of an old item? Because of the volume of submissions we must sort through every month, the items we publish are based on vendors' statements and are not individually verified. If you want your product to be considered for publication (at no charge), send full information about it, including its price and an address and telephone number where a reader can get further information, to New Products Editor,* BYTE, POB 372, *Hancock,* NH 03449.

MSX Source Code Manual

Qest Publishing has released a complete BIOS manual for the MSX standard.

MSX BIOS: The Complete MSX BASIC I/O Listing contains the full source code for MSX BASIC. This softcover book retails for $69.95. Contact Qest Publishing Inc., Suite 800, 39 West 32nd St., New York, NY 10001, (212) 564-0749. **Inquiry 645.**

Inquiry 410

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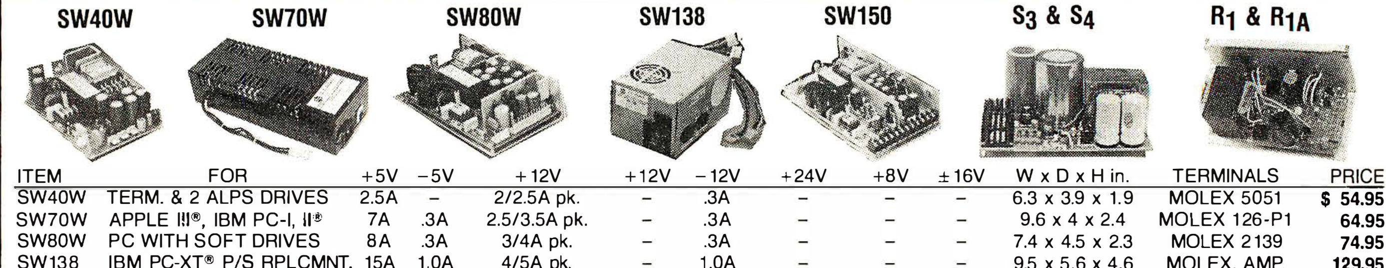
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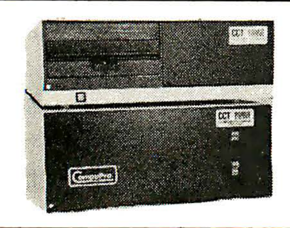
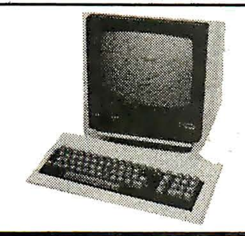
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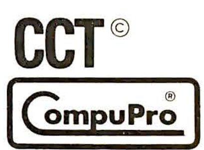
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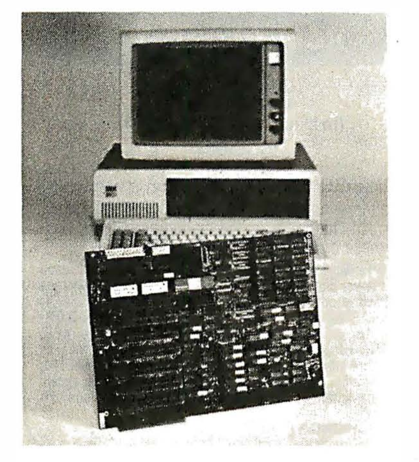
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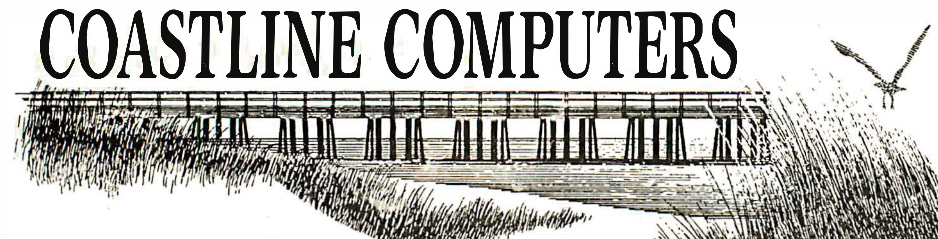
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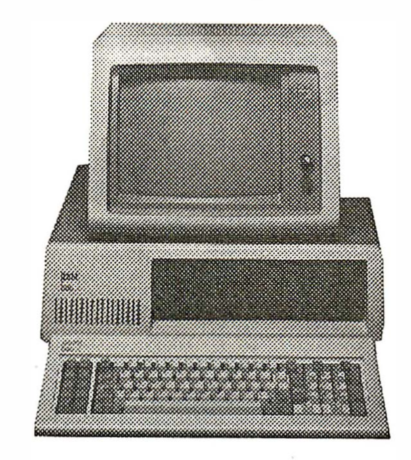
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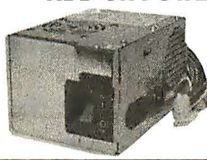
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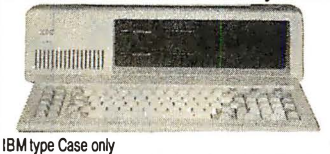
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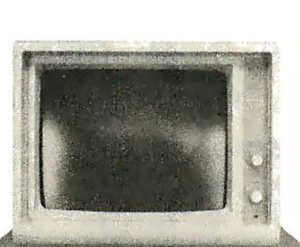
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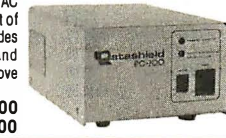
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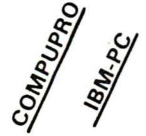
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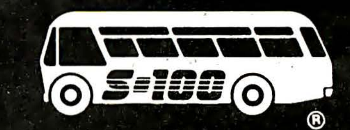
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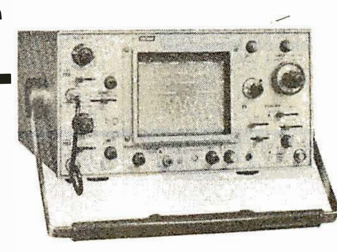
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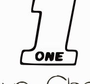
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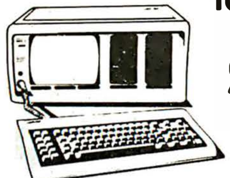
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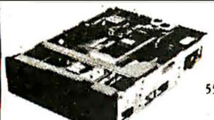
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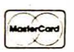
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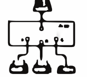
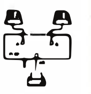


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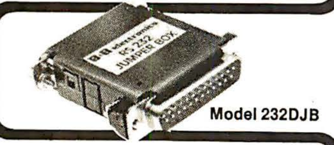
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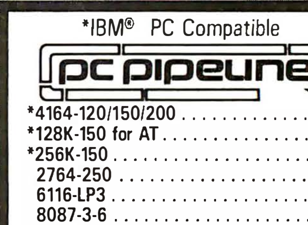
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I*U*CO is the International Union of Computer Owners, an organization designed to protect the interests of computer owners and users against those who would take their money...and then deliver less than they promised.

Here's an overview of some of the vital services I*U*CO provides:

1. Access to the lowest priced, reputable vendor for nearly every computer related need; and,
2. Protection from the rip-off artists, vaporware specialists, false advertisers and other creepy, crawly creatures who have been attracted to the computer industry by the scent of your money; and,
3. Constantly updated information on software and hardware releases, bug reports, fixes and other data individually tailored to your needs through I*U*CO's exclusive Computer Registry; and,
4. Finally, a chance to get even with those characters out there who promise a lot, take your money and then deliver less than they promised.

I*U*CO: a lynch mob with a purpose.

Every computer owner has been ripped off at least once.

Or maybe a dozen times might be a more appropriate number.

In any event, we've all been victimized by the computer industry.

And it wasn't accidental: today's computer industry is filled with hypesters, rip-off artists, vaporware specialists and others whose sole function in life is to part you from your money...while delivering less than you bargained for.

The rip-off might have been a computer that wasn't quite as "compatible" as claimed. Or a computer that didn't quite get delivered at the same time as the "hundreds" of new programs that would support it.

Or it might have been a software package that didn't quite live up to its advertising hype. Possibly, you've been had by a software manufacturer who continuously upgrades their software...charging you a pretty penny for an updated version that simply gets rid of the bugs that shouldn't have been there in the first place.

In a few cases, it might even have been a vendor who took your money...and never quite got around to delivering what you paid for.

In any event, owning a computer has been an open invitation to getting ripped-off in one way or another.

Until now.

I*U*CO means protection.

I*U*CO subscribes to some very ancient wisdom: in numbers, there is strength.

Labor unions learned it a long time ago.

An individual worker had no bargaining power. All the workers in a factory, however, have a lot of muscle.

Automobile owners learned it early on. The American Automobile Association was originally organized to bring motorists together in order to lobby for new roads and highways.

Even the computer industry has learned it: computer manufacturers, software publishers and others in the industry have now banded together in order to get legislative approval for their meaningless "disclaimers" and to restrict your right to copy the software you've purchased.

I*U*CO is designed to be what every collective organization is: a means to protect the special interests of its members.

And, in this case, the members are the victims...the people who own and use personal computers.

The people who, until now, have been powerless.

First of all, I*U*CO means low prices.

The first benefit an I*U*CO member gets is the opportunity to save money.

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I*U*CO protects you.

Of course, buying mail order can get you more than low prices.

It can also get you a lot of problems in delivery.

So, along with the low price quotation, you also get I*U*CO member evaluations and reports about the vendor...and, to make sure that you'll be happy with the product, a bibliography of reviews, articles and letters to the editor about the product or service you want to buy!

In short, as an I*U*CO member, you not only find the lowest price...but you might also find out that you don't really want to spend the money in the first place!

These are the first steps in I*U*CO's program:

1. Getting you the lowest possible prices.
2. Giving you an assessment of the potential vendor.
3. Providing information on the actual use value of the product. *(An awful lot of products sound better in their advertising than they are in reality. That's why so few companies offer a money-back guaranty.)*

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Then, as updates are announced, problems are discovered, fixes released and so on, you automatically get this information.

No more finding out a year after the fact that the current version of your program is 3.14...not the Version 1.7 program you've been using. Likewise, you might find out that the mysterious system error messages you've been getting aren't just your problem, but rather wide spread.

(As a personal note, this I*U*CO service is invaluable.

In the early days of personal computers, hardware, software and peripheral manufacturers used to be pretty good about sharing information.

Today, they're not.

In the last few weeks, I personally have learned: a) my MacIntosh 512K Upgrade is defective and won't work with MacPaint under certain circumstances; b) the ROMS in my Anadex printer have been upgraded; c) the ROMS in my IOMEGA Bernoulli box have been upgraded; d) MicroPro eliminated the copy protection on my version of Wordstar 2000 Plus; e) MicroPro had a bug in InfoStar for more than 18 months...and didn't tell anyone.

I*U*CO membership would have avoided these unpleasant surprises.)

With I*U*CO, you get the information you need on an individualized basis...and you get it fast.

You don't have to tear your hair out wondering about a problem. You might even find out about the problem before you encounter it!

I*U*CO: the iron fist.

The best part of I*U*CO has been saved for last.

Yes, I*U*CO will get you lower prices and will give you solid information about the integrity and usefulness of products and vendors.

But, more importantly, your membership in I*U*CO gives you the power of belonging to a community...a community of computer owners and users who need to protect their rights.

For instance, a group of software publishers recently managed to get the Louisiana legislature to pass a law "legalizing" the non-warranties they provide with their software. (You know, "this software is sold without any representations that it will work".)

I*U*CO will fight that kind of nonsense by lobbying against it.

Likewise, when a company...even a major company...announces vaporware, I*U*CO will use the same tools to fight back...to prevent publishers and dealers from getting us all aglow about a new machine or a new piece of software that won't be delivered for months. (For instance, how many people would have bought the MacIntosh a year ago had they known that the "hundreds" of programs to be "shortly available" simply didn't exist?)

Finally, when the situation demands it, I*U*CO will be ready to sue. For example, what do you do in a situation where you run out and buy Wordstar 2000 Plus...only to find out later that its files are not compatible with the original Wordstar? (If you read the advertising, it doesn't say a word about it. You find out after you've laid your dollars on the table!)

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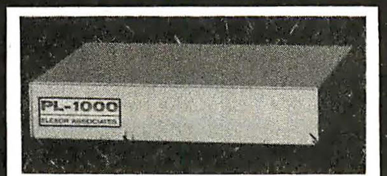
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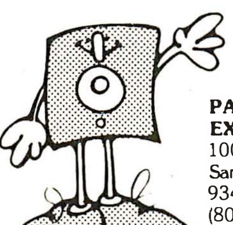
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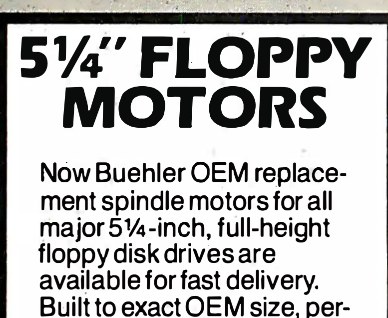
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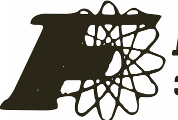
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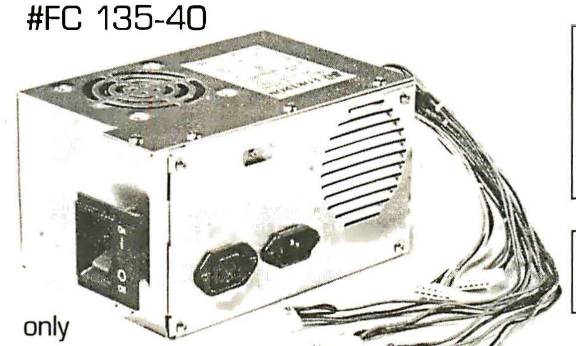
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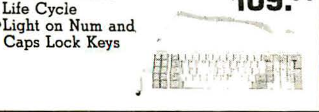
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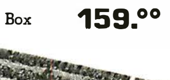


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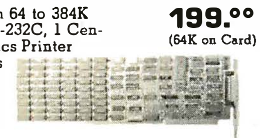
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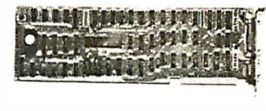


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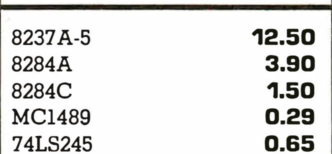
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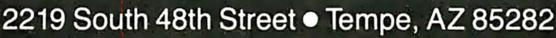
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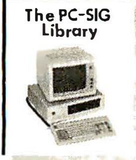
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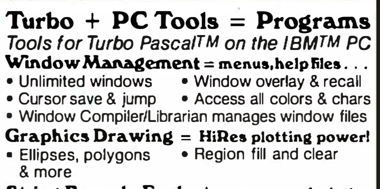
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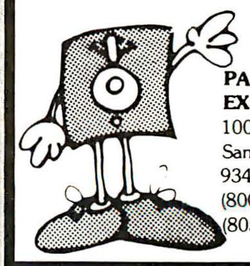
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74LS40	.24	74LS168	1.70	74LS378	1.13
74LS42	.48	74LS169	1.70	74LS379	1.30
74LS47	.74	74LS170	1.45	74LS385	1.85
74LS48	.74	74LS173	.68	74LS386	.44
74LS49	.74	74LS174	.54	74LS390	1.15
74LS51	.24	74LS175	.54	74LS393	1.15
74LS54	.28	74LS181	2.10	74LS395	1.15
74LS55	.28	74LS189	9.90	74LS399	1.45
74LS63	1.20	74LS190	.88	74LS424	2.90
74LS73	.38	74LS191	.88	74LS447	.38
74LS74	.34	74LS192	.78	74LS490	1.90
74LS75	.38	74LS193	.78	74LS624	3.95
74LS76	.38	74LS194	.68	74LS640	2.15
74LS78	.48	74LS195	.68	74LS645	2.15
74LS83	.59	74LS196	.78	74LS668	1.65
74LS85	.68	74LS197	.78	74LS669	1.85
74LS86	.38	74LS221	.88	74LS670	1.45
74LS90	.54	74LS240	.94	74LS674	9.60
74LS91	.88	74LS241	.98	74LS682	3.15
74LS92	.54	74LS242	.98	74LS683	3.15
74LS93	.54	74LS243	.98	74LS684	3.15
74LS95	.74	74LS244	1.25	74LS685	3.15
74LS96	.88	74LS245	1.45	74LS688	2.35
74LS107	.38	74LS247	.74	74LS689	3.15
74LS109	.38	74LS248	.98	74LS783	23.95
74LS112	.38	74LS249	.98	81LS95	1.45
74LS113	.38	74LS251	.58	81LS96	1.45
74LS114	.38	74LS253	.58	81LS97	1.45
74LS122	.44	74LS257	.58	81LS98	1.45
74LS123	.78	74LS258	.58	25LS2521	2.75
74LS124	2.85	74LS259	2.70	25LS2569	4.20

CRT CONTROLLERS

6845	11.95	6275	28.95
68B45	16.95	7220	38.95
HD46505sp	11.95	CRT5027	16.95
6847	10.95	CRT5037	26.95
MC1372	6.90	TMS9918A	36.95
58047	23.95	DP8350	48.95

DISC CONTROLLERS

1771	14.95	2797	54.95
1791	21.95	6843	33.95
1793	25.95	8272	16.95
1795	21.95	UPD765	16.95
1797	21.95	MB8876	23.95
2791	49.95	MB8877	25.95
2793	49.95	1691	6.95
2795	54.95	2143	6.95

UV ERASERS

QUV-T8/1 $49.95

ECONOMY Model



- Erases 15 EPROMS in 20 minutes
- Plastic Enclosure

6500

1 MHZ		2 MHz	
65022	4.90	6502A	5.90
6504	6.90	6520A	5.90
6505	8.90	6522A	9.90
6507	9.90	6532A	10.90
6520	4.30	6545A	12.90
6522	4.90	6551A	10.90
6532	9.90	**3 MHz**	
6545	9.90		
6551	9.90	65026	7.90

6800

1 MHz		68B00 2 MHz	
6800	2.90		
6802	7.90	68B00	9.90
6803	17.90	68B02	11.90
6808	12.90	68B09	11.90
6809E	8.90	68B09E	11.90
6809	6.90	68B10	5.90
6810	2.90	68B21	5.90
6820	4.30	68B40	16.90
6821	2.90	68B45	16.90
6828	13.90	68B50	5.90
6840	11.90		
6843	33.90	**68000**	
6844	24.90		
6845	11.90		
6847	10.90	68000-8	34.90
6850	2.90	68047	23.90
6852	5.90	68488	16.90
6860	7.90	68652	14.90
6862	10.90	68661	9.90
6875	6.90	68764	17.95
6880	1.90	68766	19.95
6883	21.90		

8000

8031	14.90	8253	6.90
8035	5.90	8253-5	7.90
8039	5.90	8255	4.45
INS-8060	19.90	8255-5	4.90
INS-8073	29.90	8257	7.90
8080A	3.90	8257-5	8.90
8085	4.90	8259	5.90
8085A-2	11.90	8259-5	6.90
8086	24.90	8271	69.90
8087-3 (5 MHz)	159.90	8272	19.90
8087-2 (8MHz)	279.90	8274	28.90
8088	19.90	8275	28.90
8089	59.90	8279	6.90
		8279-5	7.90
8100		8282	6.45
		8283	6.45
8131	2.90	8284	4.90
8155	6.90	8286	6.45
8155-2	7.90	8287	6.45
8156	6.90	8288	12.90
8185	28.90	8289	44.90
8185-2	38.90	8292	12.90

8200

8202	23.90
8203	38.90
8205	2.90
8212	1.75
8214	3.75
8216	1.75
8224	2.20
8226	1.75
8228	3.45
8237	12.90
8237-5	14.90
8238	4.45
8243	4.45
8250	9.90
8251	3.90
8251A	4.45

8300

8303	2.90
8304	1.90
8307	2.90
8308	2.90
8310	3.90
8311	3.90

8700

8741	28.90
8748	19.90
8749	28.90
8755	23.90

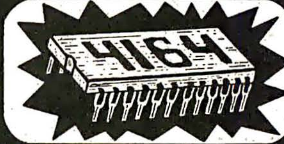
80000

80186-6	99.90
80188	89.90

Z-80

2 MHz			
Z80-CPU	1.95	Z80A-SIO/0	9.95
Z80-CTC	1.95	Z80A-SIO/1	9.95
Z80-DART	6.95	Z80A-SIO/2	9.95
Z80-DMA	7.95	Z80A-SIO/9	9.95
Z80-PIO	1.95	**6 MHz**	
Z80-SIO/0	8.95		
Z80-SIO/1	8.95	Z80B-CPU	7.95
Z80-SIO/2	8.95	Z80B-CTC	8.95
Z80-SIO/9	8.95	Z80B-PIO	8.95
		Z80B-DART	18.95
4 MHz		Z80B SIO/0	26.95
Z80A-CPU	2.45	Z80 SIO/2	26.95
Z80A-CTC	2.45		
Z80A-DART	7.95	**ZILOG**	
Z80A-DMA	8.95	Z6132	29.95
Z80A-PIO	2.45	Z8671	38.95

MEMORY EXPANSION KIT



4164 200ns

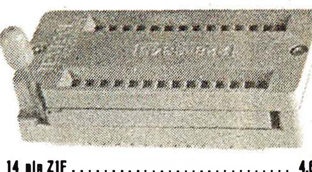
9 for $19.98

DIP SWITCHES



4 POSITION	.79
5 POSITION	.85
6 POSITION	.85
7 POSITION	.89
8 POSITION	.89

ZIF SOCKETS



14 pin ZIF	4.69
16 pin ZIF	4.69
24 pin ZIF	5.89
28 pin ZIF	6.89
40 pin ZIF	9.89

ZIF = TEXTOOL (Zero Insertion Force)

IC SOCKETS

(1 to 99)

8 pin ST.	.12	8 pin WW.	.58
14 pin ST.	.14	14 pin WW.	.68
16 pin ST.	.15	16 pin WW.	.68
18 pin ST.	.19	18 pin WW.	.98
20 pin ST.	.28	20 pin WW.	1.04
22 pin ST.	.29	22 pin WW.	1.34
24 pin ST.	.29	24 pin WW.	1.44
28 pin ST.	.39	28 pin WW.	1.64
40 pin ST.	.48	40 pin WW.	1.94

ST = Soldertail WW = Wirewrap

CRYSTAL CLOCK OSCILLATORS

PART NO.	FREQUENCY	PRICE
1.000	1.0000 MHz	6.99
1.843	1.8432 MHz	6.99
2.000	2.0000 MHz	6.99
4.000	4.0000 MHz	6.99
6.000	6.0000 MHz	6.99
10.000	10.0000 MHz	6.99
16.000	16.0000 MHz	6.99
18.432	18.4320 MHz	6.99
19.660	19.6608 MHz	6.99
20.000	20.0000 MHz	6.99
32.000	32.0000 MHz	6.99

CRYSTALS

1.0000 MHz	2.69	6.0000 MHz	1.95
1.8432 MHz	2.69	10.0000 MHz	1.95
2.0000 MHz	1.95	10.7386 MHz	1.95
2.0972 MHz	1.95	12.0000 MHz	1.95
2.4576 MHz	1.95	14.3182 MHz	1.95
3.2768 MHz	1.95	15.0000 MHz	1.95
3.5795 MHz	1.95	16.0000 MHz	1.95
4.0000 MHz	1.95	17.4300 MHz	1.95
4.1943 MHz	1.95	18.0000 MHz	1.95
4.9160 MHz	1.95	18.4320 MHz	1.95
5.0000 MHz	1.95	19.6608 MHz	1.95
5.0688 MHz	1.95	20.0000 MHz	1.95
5.1850 MHz	1.95	22.1184 MHz	1.95
5.2429 MHz	1.95	32.0000 MHz	1.95
5.7143 MHz	1.95	36.0000 MHz	1.95
6.0000 MHz	1.95	48.0000 MHz	1.95
6.1440 MHz	1.95	49.4350 MHz	1.95
6.4000 MHz	1.95	49.8900 MHz	1.95
6.5536 MHz	1.95		

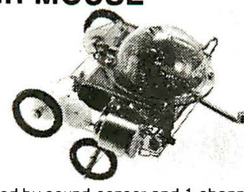
32.768 KHz...... .99

VOLTAGE REGULATORS

7805T	.74	7905T	.84
78M05C	.34	7908T	.84
7808T	.74	7912T	.84
7812T	.74	7915T	.84
7815T	.74	7924T	.84
7824T	.74	7905K	1.44
7805K	1.34	7912K	1.44
7812K	1.34	7915K	1.44
7815K	1.34	7924K	1.44
7824K	1.34	79L05	.78
78L05	.68	79L12	.78
78L12	.68	79L15	.78
78L15	.68	LM323K	4.90
78H05K	9.90	UA78S40	1.90
78H12K	9.90		

C,T = TO-220 K = TO-3 L = TO-92

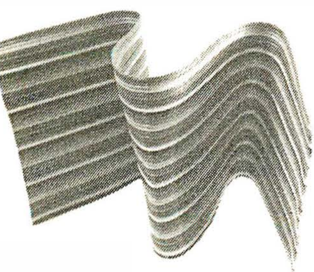
ROBOT KITS!
PIPER-MOUSE



Controlled by sound sensor and 1-channel electronic circuit. Use the whistle in this kit and Piper-Mouse follows your commands, turning left or right, stopping and starting. Uses 2 AA and 1 9V battery (not included).

MV-915 $44.95

RIBBON CABLE



	SINGLE COLOR		COLOR CODED	
CONTACTS	1'	10'	1'	10"
10	.45	4.30	.78	7.20
16	.50	4.70	.95	8.70
20	.60	5.60	1.15	10.90
25	.70	6.50	1.22	11.50
26	.70	8.50	1.27	11.50
34	.93	8.50	1.55	14.40
40	1.27	11.50	1.82	16.70
50	1.28	12.00	2.40	21.90

RESISTORS

¼ WATT 5% CARBON FILM
ALL STANDARD VALUES
FROM 1 OHM – 10 MEG OHM

50 PCS 1.25
100 PCS 2.00
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Checkmate Technology, Inc.

APPLE IIe Special

Extended 80-Col. VIDEO CARD

$69.95

★ 64K to 128K ★

ULTIVIEW 80/160 249.00

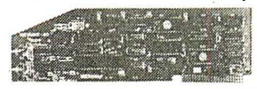
0-160 columns with any monitor!

- Screens: 80x24, 80x32, 80x48, 96x24, 132x24, 132x30, 160x24
- On-screen BOLD and Underline
- Reverse scrolling
- Easy-to-read *Wide-angle* mode
- Apple II and IIe compatible
- Prompt lines
- Upper & lowercase letters



APPLE & IBM ACCESSORIES

80 Column Apple II+ ... 149.95
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VIEWMAX-80 149.95

80-Column card for Apple II series

- Video Soft Switch
- Inverse Video
- VIDEX's Videoterm compatible



VIEWMAX-80e 119.95

80-Column extended video card for Apple IIe

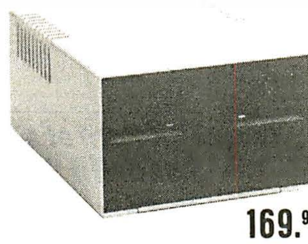
- 64K RAM, expandable to 128K
- Double High-resolution circuit
- Compatible with Pascal & CP/M

PRINTMAX 59.95

Parallel printer card, Apple II series

- Centronics compatible
- Variable print widths
- Up to 5000 characters/second

APPLE & IBM Compatible DISK DRIVES



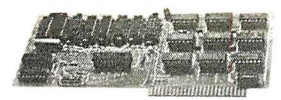
169.95

- Shugart mechanism, made in U.S.A.
- Directly replaces Apple Disk II
- Fully compatible with Apple Controller or other Apple compatible controllers.
- One Year Warranty

FULL or ½-Height

16K RAM Card – Apple II+

- 2-Year Warranty



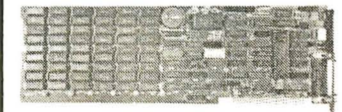
Assembled & Tested 39.95

APPLE or IBM JOYSTICK

$29.95

Compatible for either:
APPLE II and APPLE IIe
OR
IBM-PC, JR., & IBM-XT

MULTIFUNCTION CARD



- 64K to 384K RAM
- Parallel Port
- Serial Port
- Clock Calendar
- Software Included
- 1-Year Warranty

$249.95

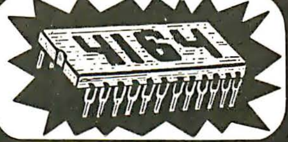
MEMORY CARD



- Expandable to 512K
- Fully compatible with IBM software
- Fully compatible w/IBM diagnostic utilities
- Serial Port Available
- 1-Year Warranty

$199.95

MEMORY EXPANSION KIT



4164 200ns
9 for $19.98

DISKETTES 5¼"

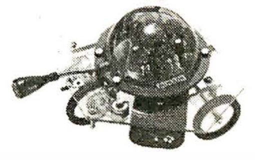
ATHANA: (SOFT SECTOR w/HUB RING)
25 per package
SS/DD ...... 29.75 or 1.19 ea.
DS/DD ...... 34.75 or 1.39 ea.

LIFETIME WARRANTY ON ALL ATHANA DISKETTES

NO LABEL: (SOFT SECTOR w/HUB RING)
25 per package
SS/DD ...... 24.75 or .99 ea.
DS/DD ...... 29.75 or 1.19 ea.

2-YEAR WARRANTY ON ALL BULK DISKETTES

ROBOT KITS!
PEPPY

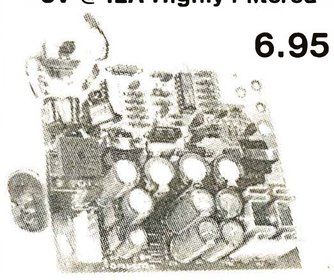


2-way sensor detects noise or solid objects in its path. When front sensor contacts an obstacle or hears a loud noise (hand-clap), Peppy automatically turns to the left.
Uses 2 AA and 1 9V battery (not included).

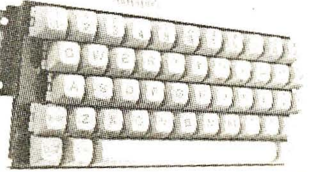
MV-916 $24.95

Reg. Power Supply
Model 4A/PS (99/4)
3 DC Outputs:
12V @ .4A, +5V @ 1.1A
−5V @ .2A Highly Filtered

6.95



KEYBOARD (99/4)



48 keys 4" x 10" 6.95

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NEC RGB COLOR MONITOR $259



The NEC JC-1401D is a 13" medium/high resolution RGB monitor suitable for use with the Sanyo MBC-550/555 or the IBM/PC. The monitor features a resolution of 400 dots by 240 lines. Colors available are Red, Green, Blue, Yellow, Cyan, Magenta, Black and White.
These monitors are currently being used in applications far more critical than microcomputers.
The NEC monitor carries the Litton-Monroe label and was originally scheduled for use in their "Office of the Future" equipment. A change in Monroe's marketing strategy has made these units excess inventory which were sold to California Digital. We are offering these prime "new" RGB monitors at a fraction of their original cost. Sanyo compatible NEC-1401/S; IBM/P/C Computer compatible NEC-1401/PC

MONITORS

BMC 12A green phosphor 15 MHz composit video	BMC-12A	7895
BMC 12" high resolution, 20MHz	BMC-12EN	119.00
Amdek 300G 12" green phosphor	AMK-300G	128 95
Amdek 300A 12" amber phos., hi-resolution	AMK-300A	138 95
Amdek 310A designed for IBM/PC, amber	AMK-310A	15895
Zenith ZVM122 Amber Phosphor 12" 40/80 column switch.	ZTH-122	8995
Zenith ZVM123 green phosphor 12" 40/80 column switch.	ZTH-Z123	89.95
NEC JB1201 green phosphor 18 MHz composit video	NEC-JB1201	15900
NEC JB1260 commercial grade composit	NEC-JB1260	119.00
Conrac 9" open frame requires horz sync & 12v supply	CON-BW9	59 00

COLOR

NEC JC1401D Medium/High 13" RGB	NEC-1401/X	25900
BMC AU9191U Color composit video with sound	BMC-9191	23895
BMC 9191M RGB designed for use with the IBM computer	BMC-9191M	37900
NEC JC1203DM, RGB color monitor	NEC-1203	699.00
NEC JC1215 color composit	NEC-JC1215	339.00
Zenith ZVM135 RGB & composite suitable for IBM PC	ZTH-Z135	47500
Amdek Color I 13" compositvideo	AMK-100	299.00
Amdek Color II - 13" RGBhi/resolution	AMK-200	419.95
Amdek Color III - 13" RGB, medium resolution	AMK-300	35995
Princeton HX-12 RGB IBM/PC compatible	PRN-HX12	478 95

PRINTERS

MATRIX PRINTERS

Star Gemini-10X 120 char/sec	STR-G10X	24900
Star Gemini-15X, 100 char/sec 15" paper	STR-G15X	36500
StarGemini Delta 10, 160 Char/sec	STR-D10	35900
Toshiba P1351, 192char/sec, letter quality	TOS-1351	1495.00
Okidata82A serial & parallel 9½" paper	OKI-82A	299.00
Okidata92A parallel interface, 160 char/sec	OKI-92A	37900
Okidata 83A & parallel 15" paper	OKI-83A	549.00
Okidata 84A & parallel 15" paper	OKI-84A	929.00
Epson RX-80 10" 120 Char/sec	EPS-RX80	23900
Epson RX-80/FT friction & tractor	EPS-RX80FT	27900
Epson FX80FT, 10" 160 char./sec with graphtrax	EPS-FX80	39900
Epson FX100FT 15" 160 char./sec with graphtrax	EPS-FX100	599.00
Epson LQ1500, 15" corespondence quality	EPS-LQ1500	1079.00
EpsonJX80 Color printer	EPS-JX80	579.00
Prowriter 8510 parallel 9½" paper	PRO-8510P	32900
Prowriter II, parallel 15" paper, graphics	PRO-2P	599.00
Dataproducts B-600-3, band printer 600 LPM	DPS-B600	698500
Printronix P300 high speed printer 300 lines per minute	PTX-P300	399500
Printronix P600 ultra high speed 600 lines per minute	PTX-P600	5795.00

WORD PROCESSING PRINTERS

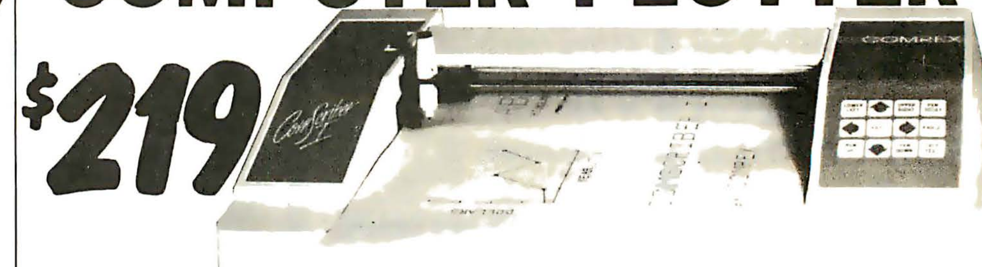
Starwriter F10 parallel, 40char/sec	PRO-F10P	499.00
NEC8810 55char/second, serial interface	NEC-8810	165900
NEC8830 55char/sec, par'l interface	NEC-8830	165900
NEC3550 popular printer designed for the IBM/PC	NEC-3550	1599.00
NEC2050 designed for IBM/PC 20 char/sec, par'l.	NEC-2050	689.00
Silver Reed EXP500, 14 char/sec, par'l interface	SRD-EXP500	31900
Silver Reed EXP550 17 Char/sec par'l interface	SRD-EXP550	42900
Diablo 630 40char/sec serial	DBL-630	156900
Diablo 620, proportional spacing, horz & vert tab 20 cps	DBL-620	76900
Juki 6100, 18 char./sec.	JUK-6100	39900
Juki 6300, 40 char/sec	JUK-6300	699.00
Comrex CR2, 5k buffer, proportional spacing, par'l	CRX-CR2P	395.00

TERMINALS

Freedom 100, split screen, detatchable keyboard	LIB-F100	495.00
Qume 102 green phosphor terminal	QUM-102	539.00
Ampex Dialogue 125 green screen.	APX-D125G	675.00
Ampex Dialouge 175 amber screen, two page, func. keys	APX-D175A	719.00
Wyse 50, 14" green phosphor	WYS-50	59500
Wyse 300, Eight color display, split screen.	WYS-300	1159.00
Zenith 29 terminal, VT52 compatible detatchable keyboard.	ZTH-Z29	765.00
Televideo 910 Plus, block mode	TVI-910P	575.00
Televideo 925, detatchable keyboard, 22 function keys	TVI-925	759.00
Televideo 950, graphic char., split screen, 22 func.	TVI-950	950.00
Televideo970, 14" green, 132 column, European	TVI-970	109500

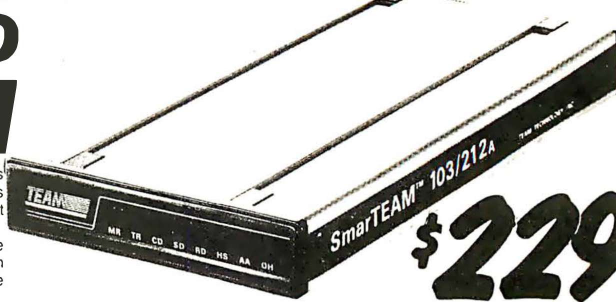
COMPUTER PLOTTER

$219



The Comrex Comscriber I is the ideal solution to make short work of translating financial and numeric data into a graphic presentation.
Many ready to run programs such as Lotus 1-2-3, Visi-on and Apple business graphics already support this plotter.
The Comscriber I features programmable paper sizes up to 8½ by 120 inches, 6 inch per second plot speed and 0.004" step size.
Easy to implement Centronics interface allows the Comscriber I immediate use with the printer port of most personal computers.
The Comscriber I is manufactured for Comrex by the Enter Computer Corporation. The plotter is marketed by Heath Kit and also sold under Enters own "Sweet P" label. This is your opportunity to purchase a graphic plotter which was originally priced at $795 for only $219.
Also available is a support package which includes demonstration software, interface cable, amulticolor pen assortment and a variety of paper and transparency material.

1200 BAUD MODEM



The Team 212A offers all the features of the Hayes Smart Modem 1200 for a fraction of the price. Now is your opportunity to purchase a 1200 baud modem at the price of a 300 baud modem.
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PROMETHEUS ProModem 1200

$319



The Prometheus Promodem 1200 is best value that we have seen in a 300/1200 baud modem. This Hayes compatible modem features completely unattended operation, auto answer/auto dial and even includes "redial number when busy". Internal diagnostics makes the Promodem 1200 an easy modem to install. Help commands, real time clock and internal speaker add to the ease of use of this unit.
An optional processor accessory allows battery back up, extra memory space for storing additional phone numbers, messages received, and can act as a transfer buffer when exchanging programs.
The Alphanumeric display option allows messages saved to be displayed when they were received, diagnostic test results, numbers in the directory, as well as modem status.

MODEMS

Team 1200 Hayes Compatible	TEM-SM1200	229.00
CTS 212AH 1200 baud, autodial	CTS-212AH	299.00
Terminal software for CTS 212AH	CTS-212SFT	35.00
Prometheus 1200 super features	PRM-P1200	319.00
Prometheus 1200B internal PC	PRM-P1200B	279.00
Signalman Mark 12, 1200 baud, Hayes compatible	SGL-MK12	23900
Signalman Mark 1, direct connect with terminal cable	SGL-MK1	75.00
Hayes Smart Modem 1200 baud, auto answer, auto dial	HYS-212AD	429.00
Hayes 1200B for use with the IBM/PC, 1200 baud	HYS-1200B	399.00
Hayes Smartmodem 300 baud only, auto answer auto dial	HYS-103AD	229.00
Hayes Micromodem II, 103 Apple direct connect	HYS-MM2	279.00
Hayes Chronograph, time & date	HYS-CHR232	199.00
U.S. Robotics 212A 300/1200 baud, autodial/answer	USR-212A	439.00
Penril 300/1200 industrial quality	PEN-12AD	495.00
Universal Data 103LP, line power, answer & originate	UDS-103LP	169.00
Universal Data 202, 1200baud, half duplex only	UDS-202LP	219.00
Universal Data212LP, full 1200 baud duplex, line power	UDS-212LP	359.00
Novation J Cat, direct connect, auto answer	NOV-JCAT	115.00

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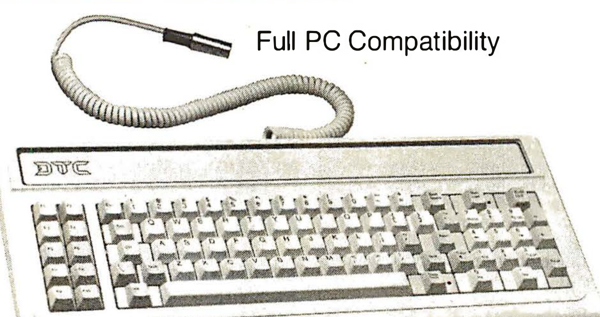
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2114L-4	1024x4	(450ns)(LP)	8/12.95
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7404	.19	7490	.35	74176	.89
7405	.25	7491	.40	74177	.75
7406	.29	7492	.50	74178	1.15
7407	.29	7493	.35	74179	1.75
7408	.24	7494	.65	74180	.75
7409	.19	7495	.55	74181	2.25
7410	.19	7496	.70	74182	.75
7411	.25	7497	2.75	74184	2.00
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7413	.35	74105	1.14	74189	2.99
7414	.49	74107	.30	74190	1.15
7416	.25	74109	.45	74191	1.15
7417	.25	74110	.45	74192	.79
7420	.19	74111	.55	74193	.79
7421	.35	74116	1.55	74194	.85
7422	.35	74120	1.20	74195	.85
7423	.29	74121	.29	74196	.79
7425	.29	74122	.45	74197	.75
7426	.29	74123	.49	74198	1.35
7427	.29	74125	.45	74199	1.35
7428	.45	74126	.45	74221	1.35
7430	.19	74128	.55	74246	1.35
7432	.29	74132	.45	74247	1.25
7433	.45	74136	.50	74248	1.85
7437	.29	74141	.65	74249	1.95
7438	.29	74142	2.95	74251	.75
7439	.79	74143	4.95	74259	2.25
7440	.19	74144	2.95	74265	1.35
7442	.49	74145	.60	74273	1.95
7443	.65	74147	1.75	74276	1.25
7444	.69	74148	1.20	74278	3.11
7445	.69	74150	1.35	74279	.75
7446	.69	74151	.55	74283	2.00
7447	.69	74152	.65	74284	3.75
7448	.69	74153	.55	74285	3.75
7450	.19	74154	1.25	74290	.95
7451	.23	74155	.75	74293	.75
7453	.23	74156	.65	74298	.85
7454	.23	74157	.55	74351	2.25
7460	.23	74159	1.65	74365	.65
7470	.35	74160	.85	74366	.65
7472	.29	74161	.69	74367	.65
7473	.34	74162	.85	74368	.65
7474	.33	74163	.69	74376	2.20
7475	.45	74164	.85	74390	1.75
7476	.35	74165	.85	74393	1.35
7480	.59	74166	1.00	74425	3.15
7481	1.10	74167	2.96	74426	.85
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4027	.45	74C14	.59
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4050	.35	74C95	.99
4051	.79	74C150	5.75
4052	1.99	74C151	2.25
4053	.79	74C154	3.25
4060	.89	74C157	1.75
4066	.39	74C160	1.19
4068	.39	74C161	1.19
4069	.29	74C162	1.19
4070	.35	74C163	1.19
4071	.29	74C164	1.39
4072	.29	74C165	2.00
4073	.29	74C173	.79
4075	.29	74C174	1.19
4076	.79	74C175	1.19
4077	.59	74C192	1.49
4078	.29	74C193	1.49
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4082	.29	74C200	5.75
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74HC: Operate at CMOS logic levels and are ideal for new, all-CMOS designs.

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74HC08	.59	74HC195	1.09
74HC10	.59	74HC238	1.35
74HC11	.59	74HC240	1.89
74HC14	.79	74HC241	1.89
74HC20	.59	74HC242	1.89
74HC27	.59	74HC243	1.89
74HC30	.59	74HC244	1.89
74HC32	.69	74HC245	1.89
74HC51	.59	74HC251	.89
74HC74	.75	74HC257	.85
74HC75	.85	74HC259	1.39
74HC85	1.35	74HC273	1.89
74HC86	.69	74HC299	4.99
74HC93	1.19	74HC367	.99
74HC125	1.19	74HC373	2.29
74HC132	1.19	74HC374	2.29
74HC138	.99	74HC393	1.39
74HC139	.99	74HC4017	1.99
74HC151	.89	74HC4020	1.39
74HC153	.89	74HC4024	1.59
74HC154	2.49	74HC4040	1.39
74HC157	.89	74HC4049	.89
74HC161	1.15	74HC4050	.89
74HC164	1.25	74HC4060	1.29
74HC166	2.95	74HC4511	2.39
74HC174	.99	74HC4538	2.29

74HCT00

74HCT: Direct, drop-in replacements for LS TTL and can be intermixed with 74LS in the same circuit.

74HCT00	.69	74HCT175	1.09
74HCT02	.69	74HCT193	1.39
74HCT04	.69	74HCT194	1.19
74HCT08	.69	74HCT195	1.29
74HCT10	.69	74HCT238	1.49
74HCT11	.69	74HCT240	2.19
74HCT14	.89	74HCT241	2.19
74HCT20	.69	74HCT242	2.19
74HCT27	.69	74HCT243	2.19
74HCT30	.69	74HCT244	2.19
74HCT32	.79	74HCT245	2.19
74HCT51	.69	74HCT251	1.09
74HCT74	.85	74HCT257	.99
74HCT75	.95	74HCT259	1.59
74HCT85	1.49	74HCT273	2.09
74HCT86	.79	74HCT299	5.25
74HCT93	1.29	74HCT367	1.09
74HCT125	1.29	74HCT373	2.49
74HCT132	1.29	74HCT374	2.49
74HCT138	1.15	74HCT393	1.59
74HCT139	1.15	74HCT4017	2.19
74HCT151	1.05	74HCT4020	1.59
74HCT153	1.05	74HCT4024	1.79
74HCT154	2.99	74HCT4040	1.59
74HCT157	.99	74HCT4049	.99
74HCT161	1.29	74HCT4050	.99
74HCT164	1.39	74HCT4060	1.49
74HCT166	3.05	74HCT4511	2.69
74HCT174	1.09	74HCT4538	2.59

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EPROM ERASERS

	Timer	Capacity Chip	Intensity (uW/Cm²)	
PE-14		9	8,000	$83.00
PE-14T	x	9	8,000	$119.00
PE-24T	x	12	9,600	$175.00
PL-265T	x	30	9,600	$255.00
PR-125T	x	25	17,000	$349.00
PR-320T	x	42	17,000	$595.00

VOLTAGE REGULATORS

TO-220 CASE PACKAGE

7805T	.75	7905T	.85
7808T	.75	7908T	.85
7812T	.75	7912T	.85
7815T	.75	7915T	.85
7824T	.75	7924T	.85

TO-3 CASE PACKAGE

7805K	1.39	7905K	1.49
7812K	1.39	7912K	1.49
7815K	1.39	7915K	1.49
7824K	1.39	7924K	1.49

TO-92 CASE PACKAGE

78L05	.69	79L05	.79
78L12	.69	79L12	.79
78L15	.69	79L15	.79

OTHER VOLTAGE REGS

78M05C	5volt	½amp	TO-220	.35
LM323K	5volt	3amp	TO-3	4.95
LM338K	Adj.	5amp	TO-3	3.95
78H05K	5volt	5amp	TO-3	9.95
78H12K	12volt	5amp	TO-3	9.95
78P05K	5volt	10amp	TO-3	14.95
UA78S40	FAIRCHILD		DIP	1.95

LINEAR

LM301	.34	NE570	3.95
LM301H	.79	NE571	2.95
LM307	.45	NE590	2.50
LM308	.69	NE592	.98
LM308H	1.15	LM709	.59
LM309H	1.95	LM710	.75
LM309K	1.25	LM711	.79
LM310	1.75	LM723	.49
LM311	.64	LM723H	.55
LM311H	.89	LM733	.98
LM312H	1.75	LM741	.35
LM317K	3.95	LM741N-14	.35
LM317T	1.19	LM741H	.40
LM318	1.49	LM747	.69
LM318H	1.59	LM748	.59
LM319H	1.90	LM1014	1.19
LM319	1.25	LM1303	1.95
LM320	see7900	LM1310	1.49
LM322	1.65	MC1330	1.69
LM323K	4.95	MC1349	1.89
LM324	.59	MC1350	1.19
LM329	.65	MC1358	1.69
LM331	3.95	MC1372	6.95
LM334	1.19	LM1414	1.59
LM335	1.40	LM1458	.59
LM336	1.75	LM1488	.69
LM337T	1.95	LM1489	.69
LM337K	3.95	LM1496	.85
LM338K	3.95	LM1558H	3.10
LM339	.99	LM1800	2.37
LM340	see7800	LM1812	8.25
LM348	.99	LM1830	3.50
LM350K	4.95	LM1871	5.49
LM350T	4.60	LM1872	5.49
LM358	.69	LM1877	3.52
LM359	1.79	LM1889	1.95
LM376	3.75	LM1896	1.75
LM377	1.95	ULN2003	1.29
LM378	2.50	XR2206	3.75
LM379	4.50	LM2877	2.05
LM380	.89	LM2878	2.25
LM380N-8	1.10	LM2900	.85
LM381	1.60	LM2901	1.00
LM382	1.60	MPQ2907	1.95
LM383	1.95	LM2917	2.95
LM384	1.95	MC3487	2.95
LM386	.89	LM3900	.59
LM387	1.40	LM3905	1.25
LM389	1.35	LM3909	.98
LM390	1.95	LM3911	2.25
LM392	.69	LM3914	3.95
LM393	1.29	LM3915	3.95
LM394H	4.60	LM3916	3.95
LM399H	5.00	MC4024	3.95
NE531	2.95	MC4044	4.50
NE555	.34	RC4136	1.25
NE556	.65	RC4151	3.95
NE558	1.50	LM4250	1.75
NE564	2.95	LM4500	3.25
LM565	.99	RC4558	.69
LM566	1.49	LM13600	1.49
LM567	.89	LM13700	1.45

H=TO-5 CAN, K=TO-3, T=TO-220

RCA

CA3023	2.75	CA3083	1.55
CA3039	1.29	CA3086	.80
CA3046	1.25	CA3089	2.99
CA3059	2.90	CA3096	3.49
CA3060	2.90	CA3130	1.30
CA3065	1.75	CA3140	1.15
CA3080	1.10	CA3146	1.85
CA3081	1.65	CA3160	1.19
CA3082	1.65	CA3183	.99

TI

TL494	4.20	75365	1.95
TL496	1.65	75450	.59
TL497	3.25	75451	.39
75107	1.49	75452	.39
75108	1.49	75453	.39
75110	1.95	75454	.39
75150	1.95	75477	1.29
75154	1.95	75491	.79
75160	4.95	75492	.79
75188	1.25	75493	.89
75189	1.25	75494	.89

BI FET

TL066	.99	LF347	2.19
TL071	.79	LF351	.60
TL072	1.19	LF353	1.00
TL074	2.19	LF355	1.10
TL081	.79	LF356	1.10
TL082	1.19	LF357	1.40
TL083	1.19	LF411	1.29
TL084	2.19	LF412	1.99

TRANSISTORS

2N918	.50	2N3772	1.85
MPS918	.25	2N3903	.25
2N2102	.75	2N3904	.10
2N2218	.50	2N3906	.10
2N2218A	.50	2N4122	.25
2N2219	.50	2N4123	.25
2N2219A	.50	2N4249	.25
2N2222	.25	2N4304	.75
PN2222	.10	2N4401	.25
MPS2369	.25	2N4402	.25
2N2484	.25	2N4403	.25
2N2905	.50	2N4857	1.00
2N2907	.25	PN4916	.25
PN2907	.13	2N5086	.25
2N3055	.79	PN5129	.25
3055T	.69	PN5139	.25
2N3393	.30	2N5209	.25
2N3414	.25	2N6028	.35
2N3563	.40	2N6043	1.75
2N3565	.40	2N6045	1.75
PN3565	.25	MPS-A05	.25
MPS3638	.25	MPS-A06	.25
MPS3640	.25	MPS-A13	.40
PN3643	.25	MPS-A55	.25
PN3644	.25	MPU-131	.99
MPS3704	.15	TIP29	.65
MPS3706	.15	TIP31	.75
		TIP32	.79

IC SOCKETS

	1-99	100
8 PIN ST	.13	.11
14 PIN ST	.15	.12
16 PIN ST	.17	.13
18 PIN ST	.20	.18
20 PIN ST	.29	.27
22 PIN ST	.30	.27
24 PIN ST	.30	.27
28 PIN ST	.40	.32
40 PIN ST	.49	.39
64 PIN ST	4.25	CALL

ST=SOLDERTAIL

8 PIN WW	.59	.49
14 PIN WW	.69	.52
16 PIN WW	.69	.58
18 PIN WW	.99	.90
20 PIN WW	1.09	.98
22 PIN WW	1.39	1.28
24 PIN WW	1.49	1.35
28 PIN WW	1.69	1.49
40 PIN WW	1.99	1.80

WW=WIREWRAP

INTERFACE

8T26	1.59
8T28	1.98
8T95	.89
8T96	.89
8T97	.89
8T98	.89
DM8131	2.95
DP8304	2.29
DS8833	2.25
DS8835	1.99
DS8836	.99
DS8837	1.65
DS8838	1.30

INTERSIL

ICL7106	9.95
ICL7107	12.95
ICL7660	2.95
ICL8038	3.95
ICM7207A	5.59
ICM7208	15.95

DATA ACQ.

ADC0800	15.55
ADC0804	3.49
ADC0809	4.49
ADC0816	14.95
ADC0817	9.95
ADC0831	8.95
DAC0800	4.49
DAC0806	1.95
DAC0808	2.95
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DAC1021	7.95
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MC1408L6	1.95
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EXAR

XR2206	3.75
XR2207	3.75
XR2208	3.75
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XR2240	3.25

9000

9304	.95
9316	1.00
9328	1.49
9334	2.50
9368	3.95
9401	9.95
9601	.75
9602	1.50
9637	2.95
96S02	1.95

SOUND CHIPS

76477	3.95
76488	5.95
76489	8.95
SSI-263	39.95
AY3-8910	12.95
AY3-8912	12.95
MC3340	1.49
SP1000	39.00

OPTO-ISOLATORS

4N26	1.00	MCA-7	4.25
4N27	1.10	MCA-255	1.75
4N28	.69	IL-1	1.25
4N33	1.75	ILA-30	1.25
4N35	1.25	ILQ-74	2.75
4N37	1.25	H11C5	1.25
MCT-2	1.00	TIL-111	1.00
MCT-6	1.50	TIL-113	1.75

I'm writing to thank you again for the out-standing spirit of service to customers with which you handled our telephone order today. The high level of service orientation you exhibit is rarely found these days. . . . It is gratifying to find you as a supplier who stocks electronic components we often find difficult to obtain . . . we will surely look on you as a preferred supplier.

— C. K. Fulton





DB25S RS232 FEMALE SOLDER CUP 2.25   DB25P RS232 MALE SOLDER CUP 1.90

BARGAIN HUNTERS CORNER

DYNAMIC RAMS

41256	256K	200ns	$10.95
4164	64K	200ns	9/$19.95

STATIC RAMS

HM6264	8Kx8	150ns	CMOS	$17.95
TMM2016	2Kx8	200ns		$3.25
HM6116	2Kx8	200ns	CMOS	$3.69

EPROMS

27128	16Kx8	250ns	$13.95
2764	8Kx8	450ns	$4.95
2732	4Kx8	450ns	$4.25

MATH CO-PROCESSOR CHIPS

8087-3	INTEL	$129.00
8087-6	INTEL	$119.00

SPECIALS ENDS 4/30/85

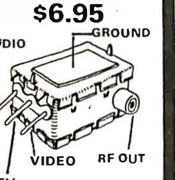
RF MODULATOR

(ASTEC UM1082)

QUANTITIES LIMITED

- PRESET TO CHANNEL 3
- USE TO BUILD TV-COMPUTER INTERFACE
- +5 VOLT OPERATION

$6.95



EMI FILTER

- MAJOR MANUFACTURER
- LOW COST
- FITS LC-HP BELOW

$4.95

LINE CORDS

LC-2	2 CONDUCTOR	6 ft	.39
LC-3	3 CONDUCTOR	6 ft	.99
LC-HP	3 CONDUCTOR WITH STANDARD FEMALE SOCKET	6 ft	1.49
LC-CIR	CIGARETTE LIGHTER PLUG WITH 6 ft COILED CORD		2.95

MUFFIN FANS

4.68" SQUARE	14.95
3" SQUARE	14.95

RESISTORS

¼ WATT 5% CARBON FILM
ALL STANDARD VALUES
FROM 1 OHM TO 10 MEG OHM

50 PIECES SAME VALUE	.025
100 PIECES SAME VALUE	.02
1000 PIECES SAME VALUE	.015

CAPACITORS

TANTALUM

1.0µf	15V	.40	.47µf	35V	.50
6.8	15V	.70	1.0	35V	.45
10	15V	.80	2.2	35V	.65
22	15V	1.35	4.7	35V	.85
.22	35V	.40	10	35V	1.00

DISC

10pf	50V	.05	560	50V	.05
22	50V	.05	680	50V	.05
25	50V	.05	820	50V	.05
27	50V	.05	.001µf	50V	.05
33	50V	.05	.0015	50V	.05
47	50V	.05	.0022	50V	.05
56	50V	.05	.005	50V	.05
68	50V	.05	.01	50V	.07
82	50V	.05	.02	50V	.07
100	50V	.05	.05	50V	.07
220	50V	.05	.1	12V	.10

MONOLITHIC

.01µf	50V	.14	.1µf	50V	.18
.047µf	50V	.15	.47µf	50V	.25

ELECTROLYTIC

RADIAL			AXIAL		
1µf	25V	.14	1µf	50V	.14
2.2	35V	.15	4.7	16V	.14
4.7	50V	.15	10	16V	.14
10	50V	.15	10	50V	.16
47	35V	.18	22	16V	.14
100	16V	.18	47	50V	.20
220	35V	.20	100	15V	.20
470	25V	.30	100	35V	.25
2200	16V	.60	220	25V	.30
			330	16V	.40
			500	16V	.42
			1000	16V	.60
			2200	16V	.70
			6000	16V	.85

COMPUTER GRADE
44,000µf 30V 3.95

HARD TO FIND "SNAPABLE" HEADERS

Can easily be snapped apart to make any size header, all with .1" centers

1x40	STRAIGHT LEAD	1.99
1x40	RIGHT ANGLE	1.49
2x40	STRAIGHT LEAD	2.49
2x40	RIGHT ANGLE	2.99

SHORTING BLOCKS

SPACED AT .1" CENTERS
IDEAL FOR DISK DRIVES
OR ANY .1" HEADER

5/1.00

DIP SWITCHES

4 POSITION	.85
5 POSITION	.90
6 POSITION	.90
7 POSITION	.95
8 POSITION	.95
10 POSITION	1.29

EDGECARD CONNECTORS

S-100 ST	S-100	3.95
S-100 WW	S-100	4.95
72 PIN ST		6.95
72 PIN WW		7.95
62 PIN ST	IBM PC	4.95
50 PIN ST	APPLE	4.95
44 PIN ST		2.95
44 PIN WW		4.95

BYPASS CAPS

.01 µf DISC	100/$6.00
.01 µf MONOLITHIC	100/$12.00
.1 µf DISC	100/$8.00
.1 µf MONOLITHIC	100/$15.00

DIODES

1N751	5.1 VOLT ZENER	.25
1N759	12.0 VOLT ZENER	.25
1N4148	(1N914)SWITCHING	25/1.00
1N4001	50PIV 1A	12/1.00
1N4004	400PIV RECTIFIER	10/1.00
1N5402	200PIV 3A	.25
KBP02	200PIV 1.5A BRIDGE	.45
KBP04	400PIV 1.5A BRIDGE	.55
MDA801	50PIV 12A BRIDGE	1.39
MDA980-1	50PIV 12A BRIDGE	1.95
MDA980-2	100PIV 12A BRIDGE	2.25
VM48	DIP-BRIDGE	.35

36 PIN CENTRONICS

IDCEN36	RIBBON CABLE MALE	8.95
IDCEN36/F	RIBBON CABLE FEMALE	8.95
CEN36	SOLDER CUP MALE	7.95

LED DISPLAYS

HP5082-7760	CC	.43"	1.29
MAN-72	CA	.3"	.99
MAN-74	CC	.3"	.99
FND-357(359)	CC	.375"	1.25
FND-500(503)	CC	.5"	1.49
FND-507(510)	CA	.5"	1.49
TIL-311 4x7 HEX W/LOGIC		.270"	9.95

DIP CONNECTORS

DESCRIPTION	ORDER BY	CONTACTS 8	14	16	18	20	22	24	28	40
HIGH RELIABILITY TOOLED ST IC SOCKETS	AUGATxxST	.99	.99	.99	1.69	1.89	1.89	1.99	2.49	2.99
HIGH RELIABILITY TOOLED WW IC SOCKETS	AUGATxxWW	1.30	1.80	2.10	2.40	2.50	2.90	3.15	3.70	5.40
COMPONENT CARRIES (DIP HEADERS)	ICCxx	.49	.59	.69	.99	.99	.99	.99	1.09	1.49
RIBBON CABLE DIP PLUGS (IDC)	IDPxx	---	.95	.95	---	---	---	1.75	---	2.95

FOR ORDERING INSTRUCTIONS SEE IDC CONNECTORS BELOW

HEAT SINKS

TO-220	SCREW ON	.35
TO-220	CLIP ON	.35
TO-3	SCREW ON	.95
TO-220	INSULATOR	10/1.00
TO-3	INSULATOR	10/1.00

SWITCHES

SPDT MINI-TOGGLE ON-ON	1.25
DPDT MINI-TOGGLE ON-ON	1.50
DPDT MINI-TOGGLE ON-OFF-ON	1.75
SPST MINI-PUSHBUTTON N.O.	.39
SPST MINI-PUSHBUTTON N.C.	.39
BCD OUT 10 POSITION 6 PIN DIP	1.95

DIFFUSED LEDS

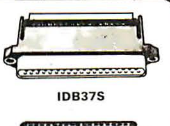
		1-99	100-up
JUMBO RED	T1¾	.10	.09
JUMBO GREEN	T1¾	.18	.15
JUMBO YELLOW	T1¾	.18	.15
MOUNTING HDW	T1¾	.10	.09
MINI RED	T1	.10	.09
MINI GREEN	T1	.18	.15
MINI YELLOW	T1	.18	.15
RECT RED	2x5mm	.25	.22
RECT GREEN	2x5mm	.30	.27
RECT YELLOW	2x5mm	.30	.27

D-SUBMINIATURE

DESCRIPTION		ORDER BY	CONTACTS 9	15	25	37	50
SOLDER CUP	MALE	DBxxP	1.19	1.59	1.90	2.85	4.25
	FEMALE	DBxxS	1.50	1.85	2.25	3.90	5.25
RIGHT ANGLE PC SOLDER	MALE	DBxxPR	1.65	2.20	3.00	4.83	---
	FEMALE	DBxxSR	2.18	3.03	3.00	6.19	---
WIRE WRAP	MALE	DBxxPWW	1.69	2.56	3.89	5.60	---
	FEMALE	DBxxSWW	2.76	4.27	6.84	9.95	---
IDC RIBBON CABLE	MALE	IDBxxP	2.95	3.90	4.75	6.95	---
	FEMALE	IDBxxS	3.25	4.29	5.25	7.95	---
HOODS	BLACK	HOOD-B	---	---	.99	---	---
	GREY	HOOD	.89	.99	.99	1.09	1.19

MOUNTING HARDWARE-$1.00

FOR ORDERING INSTRUCTIONS SEE IDC CONNECTORS BELOW



DB37S

DB25SR

TEXTOOL ZERO INSERTION FORCE SOCKETS AND RECEPTACLES



SCREWDRIVER CLAMP ECONO ZIF — LEVER CLAMP ZIF SOCKET — WW RECEPTACLES ZIF RECEPTACLE

TYPE	CONTACTS 14	16	24	28	40
ECONO ZIF	---	4.95	6.75	7.75	9.95
ZIF SOCKET	4.95	4.95	5.95	6.95	9.95
ZIF RECEPTACLE	8.25	8.75	9.75	10.50	12.75

IDC CONNECTORS

DESCRIPTION	ORDER BY	CONTACTS 10	20	26	34	40	50
SOLDER HEADER	IDHxxS	.82	1.29	1.68	2.20	2.58	3.24
RIGHT ANGLE SOLDER HEADER	IDHxxSR	.85	1.35	1.76	2.31	2.72	3.39
WW HEADER	IDHxxW	1.86	2.98	3.84	4.50	5.28	6.63
RIGHT ANGLE WW HEADER	IDHxxWR	2.05	3.28	4.22	4.45	4.80	7.30
RIBBON HEADER SOCKET	IDSxx	.79	.99	1.39	1.59	1.99	2.25
RIBBON HEADER	IDMxx	---	5.50	6.25	7.00	7.50	8.50
RIBBON EDGE CARD	IDExx	1.75	2.25	2.65	2.75	3.80	3.95

ORDERING INSTUCTIONS: INSERT THE NUMBER OF CONTACTS IN THE POSITION MARKED "xx" OF THE "ORDER BY" PART NUMBER LISTED. EXAMPLE: A 10 PIN RIGHT ANGLE HOLDER STYLE WOULD BE IDH10SR

IDH20W

IDE50

RIBBON CABLE

CONTACTS	SINGLE COLOR 1'	10'	COLOR CODED 1'	10'
10	.18	1.60	.83	7.30
16	.28	2.50	1.00	8.80
20	.36	3.20	1.25	11.00
25	.45	4.00	1.32	11.60
26	.46	4.10	1.32	11.60
34	.61	5.40	1.65	14.50
40	.72	6.40	1.92	16.80
50	.89	7.50	2.50	22.00

JDR Microdevices

1224 S. Bascom Avenue, San Jose, CA 95128
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FAX (408) 275-8415 • Telex 171-110

RETAIL STORE - 1256 S. BASCOM AVENUE
HOURS: M-W-F, 9-5 TU-TH, 9-9 SAT, 10-3

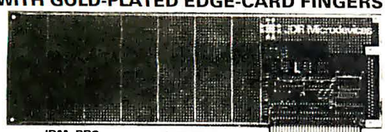
PLEASE USE YOUR CUSTOMER NUMBER WHEN ORDERING

TERMS: Minimum order $10.00. For shipping and handling include $2.50 for UPS Ground and $3.50 for UPS Air. Orders over 1 lb. and foreign orders may require additional shipping charges - please contact our sales department for the amount. CA. residents must include 6% sales tax. Bay Area and LA residents include 6½%. All merchandise is warranted for 90 days unless otherwise stated. Prices are subject to change without notice. We are not responsible for typographical errors. We reserve the right to limit quantities and to substitute manufacturer. All merchandise subject to prior sale.

IBM PC PROTOTYPE CARD WITH DECODING CIRCUITRY $29.95

WIRE WRAP PROTOTYPE CARDS

FR-4 EPOXY GLASS LAMINATE WITH GOLD-PLATED EDGE-CARD FINGERS



IBM-PR2

IBM

BOTH CARDS HAVE SILK SCREENED LEGENDS AND INCLUDES MOUNTING BRACKET

IBM-PR1	WITH +5V AND GROUND PLANE	$27.95
IBM-PR2	AS ABOVE WITH DECODING CIRCUITRY	$29.95

S-100

P100-1	BARE - NO FOIL PADS	$15.15
P100-2	HORIZONTAL BUS	$21.80
P100-3	VERTICAL BUS	$21.80
P100-4	SINGLE FOIL PADS PER HOLE	$22.75

APPLE

P500-1	BARE - NO FOIL PADS	$15.15
P500-3	HORIZONTAL BUS	$21.75
P500-4	SINGLE FOIL PADS PER HOLE	$21.80
7060-45	FOR APPLE IIe AUX SLOT	$30.00

GENERAL PURPOSE

22/44 PIN EDGE-CARD (.156" SPACING)

P441-1	BARE - NO FOIL PADS 4.5" x 6.0"	$9.45
P441-3	VERTICAL BUS 4.5" x 6.0"	$13.95
P441-4	SINGLE FOIL PADS 4.5" x 6.0"	$14.20
P442-1	BARE - NO FOIL PADS 4.5" x 9.0"	$10.40
P442-3	VERTICAL BUS 4.5" x 9.0"	$14.20
P442-4	SINGLE FOIL PADS 4.5" x 9.0"	$13.50

36/72 PIN EDGE-CARD (.1" SPACING)

P721-1	BARE - NO FOIL PADS 4.5" x 6.0"	$9.45
P721-3	VERTICAL BUS 4.5" x 6.0"	$13.25
P721-4	SINGLE FOIL PADS 4.5" x 6.0"	$14.20
P722-1	BARE - NO FOIL PADS 4.5" x 9.0"	$10.40
P722-3	VERTICAL BUS 4.5" x 9.0"	$14.20
P722-4	SINGLE FOIL PADS 4.5" x 9.0"	$15.15

BARE GLASS BOARDS

NO EDGE-CARD FINGERS OR FOIL

P25x45	2.5" x 4.5"	$2.40
P45x65	4.5" x 6.5"	$4.70
P45x85	4.5" x 8.5"	$6.20
P45x170	4.5" x 17.0"	$11.35
P85x170	8.5" x 17.0"	$18.95

EXTENDER CARDS

IBM	$45.00
APPLE	$45.00
MULTIBUS	$86.00

DISK DRIVES

TANDON

TM 100-1 5¼" (FOR IBM) SS/DD	$139.95
TM 100-2 5¼" (FOR IBM) DS/DD	$159.95

MPI

MPI-B52 5¼" (FOR IBM) DS/DD	$109.95

TEAC

FD-55B ½ HEIGHT DS/DD	$129.95
FD-55F ½ HEIGHT DS/QUAD	$139.95

SHUGART

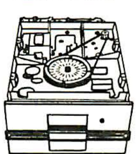
SA 400L 5¼" (40 TRACK) SS/DD	$199.95
SA 460 5¼" (80 TRACK) DS/QUAD	$199.95

8" DISK DRIVES

FD100-8 BY SIEMENS, SHUGART 801 EQUIV. SS/DD	$129.00
FD200-8 BY SIEMENS, SHUGART 851 EQUIV. DS/DD	$180.00

JFORMAT-2 $49.95
SUPPORT FOR QUAD DENSITY DRIVES FROM TALL TREE SYSTEMS


TEAC FD-55B


TANDON TM100-2

PLEASE INCLUDE SUFFICENT AMOUNT FOR SHIPPING ON ABOVE ITEMS

DISK DRIVE CABINETS

CABINET #1 $29.95
* Fits one full height 5¼" disk drive
* Color matches Apple

CABINET #2 $79.00
* Fits one full height 5¼" disk drive
* Complete with power supply, switch, line cord, fuse and standard power connector
* Please specify Grey or Tan

CABINET #3 $89.95
* Fits two half height 5¼" disk drives
* Complete with power supply, switch, line cord, fuse and standard power connectors

8" DISK DRIVE CABINETS ALSO AVAILABLE-PLEASE CALL

PLEASE INCLUDE SUFFICIENT AMOUNT FOR SHIPPING ON ABOVE ITEMS

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PS-IBM $175.00
* FOR IBM PC-XT COMPATIBLE
* 130 WATTS
* +5V @ 15A, +12V @ 4.2A -5V @ .5A, -12V @ .5A
* ONE YEAR WARRANTY

PS-A $49.95
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* +5V @ 4A, +12V @ 2.5A -5V @ .5A, -12V @ .5A
* APPLE POWER CONNECTOR

PS-3 $39.95
* AS USED IN APPLE III
* +5V @ 4A, +12V @ 2.5A -5V @ .25A, -12V @ .30A,
* 15.5" x 4.5" x 2", .884 LBS.

PS-ASTEC $19.95
* CAN POWER TWO 5¼" FDDS
* +5V @ 2.5A, +12V @ 2A -12V @ .1A
* +5V @ 5A IF +12V IS NOT USED
* 6.3" x 4.0" x 1.9"

OK INDUSTRIES

EX-1 IC EXTRACTION TOOL
* ONE PIECE METAL CONSTRUCTION
* EASILY EXTRACTS 8-24 PIN DEVICES
* LOW COST $2.19

EX-1

EX-2 IC EXTRACTION TOOL
* EXTRACTS 24-40 PIN DEVICES
* HEAVY DUTY METAL CONSTRUCTION
* GROUND LUGS FOR MOS EXTRACTIONS
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INS-1416	for 14-16 pin IC's	$5.15
MOS-1416	for 14-16 pin IC's	$10.92
MOS-2428	for 24-28 pin IC's	$10.92
MOS-40	for 40 pin IC's	$12.43

MOS series insertion tools have metal constuction and include grounding lug for CMOS applications.

INS-1416 INS-2428

BW-630 WIRE WRAP GUN
* BATTERY POWERED-USES 2 NI-CAD C CELLS (NOT INCLUDED)
* POSITIVE INDEXING
* ANTI-OVERWRAP DEVICE $41.55

BW-630

WSU-30 WIRE WRAP TOOLS
* WRAPS, STRIPS, AND UNWRAPS
* WSU-30M WRAPS AN EXTRA TURN OF INSULATION

WSU-30 $8.84/WSU-30M $10.14

WSU-30/30M

WIRE WRAP TERMINALS

WWT-1	SLOTTED	25/$7.06
WWT-2	SINGLE SIDED	25/$4.25
WWT-3	IC SOCKET	25/$7.06
WWT-4	DOUBLE SIDED	25/2.80
INS-1	INSERTION TOOL	$3.64

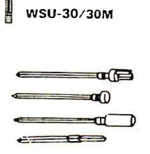
WIRE DISPENSER
* WITH 50' ROLL OF WIRE
* BUILT IN PLUNGER CUTS WIRE
* BUILT IN STRIPPER STRIPES 1"
* REFILLABLE

WD-30 $6.50 Specify Blue, white, Yellow or Red
WD-30TRI $9.50 With 50' of each: Red, Blue and White

SOCKET-WRAP I.D.™
* SLIPS OVER WIRE WRAP PINS
* IDENTIFIES PIN NUMBERS ON WRAP SIDE OF BOARD
* CAN WRITE ON PLASTIC; SUCH AS IC #

PINS	PART#	PCK. OF	PRICE
8	IDWRAP 08	10	1.95
14	IDWRAP 14	10	1.95
16	IDWRAP 16	10	1.95
18	IDWRAP 18	5	1.95
20	IDWRAP 20	5	1.95
22	IDWRAP 22	5	1.95
24	IDWRAP 24	5	1.95
28	IDWRAP 28	5	1.95
40	IDWRAP 40	5	1.95

PLEASE ORDER BY NUMBER OF PACKAGES (PCK. OF)



WIRE WRAP WIRE

PRECUT AND STRIPPED

Note: 1 inch of insulation is stripped on each end. A 3.5" wire has only 1.5" of insulation.

LENGTH (INCHES)	QUANTITY 100	500	1000
2.5	1.60	4.70	8.20
3	1.60	4.70	8.20
3.5	1.65	5.00	8.90
4	1.75	5.40	9.60
4.5	1.80	5.75	10.30
5	1.85	6.10	11.00
5.5	1.90	6.50	11.75
6	2.00	6.85	12.50
6.5	2.30	7.80	14.30
7	2.40	8.20	15.05
7.5	2.50	8.55	15.85
8	2.60	8.95	16.60
8.5	2.65	9.30	17.40
9	2.70	9.80	18.15
9.5	2.80	10.00	18.95
10	2.90	10.50	19.70

PRECUT ASSORTMENT IN ASSORTED COLORS $27.50

100ea: 5.5", 6", 6.5", 7"
250ea: 2.5", 4.5", 5"
500ea: .3", 3.5", 4"

SPOOLS

100 feet	$4.30	250 feet	$7.25
500 feet	$13.25	1000 feet	$21.95

Please specify color: Blue, Black, Yellow or Red

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12.6V AC	2 AMP	4.95
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12V AC	2 AMP	6.95

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6, 9, 12V DC SELECTABLE WITH UNIVERAL ADAPTER 8.95

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Over 800 pages of manufacturer's data sheets on the most commonly used IC's
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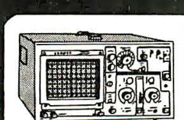
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UNSURPASSED QUALITY AT AN UNBEATABLE PRICE

* BAND WIDTH- DC: DC TO 20MHz (-3db) AC: 10Hz TO 20MHz (-3db)
* SWEEP TIME- .2 μSEC TO .5 SEC/DIV ON 20 RANGES
* VERT./HORZ. DEFLECTION: 5mVTO 20V/DIV ON 20 RANGES
* COMPLETE MANUAL AND HIGH QUALITY HOOK-ON PROBES INCLUDED
* INPUT IMPEDANCE: 1 MEG OHM
* TV VIDEO SYNC FILTER
* X, Y AND Z AXIS OPERATION
* 110/220 VOLT 50/60Hz OPERATION
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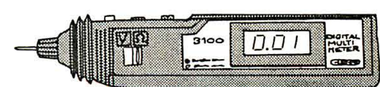
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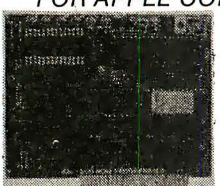
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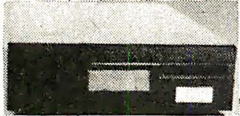
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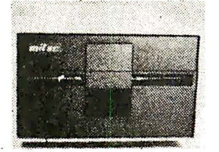
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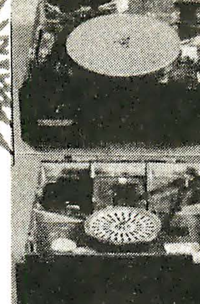
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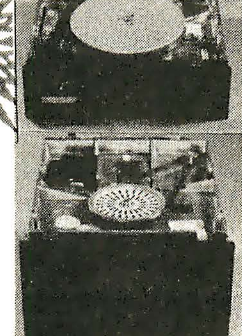
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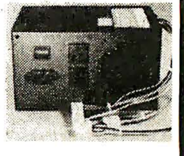
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WANTED: Children's Service Society of Wisconsin seeks tax-deductible donation of Apple IIe or II+ for information management. Carole Montemayor, Children's Service Society, 2059 Atwood Ave., Madison, WI 53704, (608) 249-8506.

WANTED: Charitable nonprofit organization seeks donation of computers, peripherals, printers, monitors, terminals, disk drives, memory expansion, etc. Certified receipts furnished; will pay reasonable shipping. Holdeman International, POB 329, West Point, MS 39773.

WANTED: Donations of any personal computer, peripherals, and supplies to advance work of stuttering self-help organization. Tax-deductible; will pay shipping. Speak Easy Int'l. Foundation, 233 Concord Dr., Paramus, NJ 07652, (201) 262-0895.

WANTED: A group of Malaysian students in Fresno would like advice and support from experienced IBM PC users. Hasnul Hashim, Apt. D, 2127 East Shaw Ave., Fresno, CA 93710, (209) 229-1214.

AVAILABLE: Free to all MS-DOS, PC-DOS, and Z-DOS users: disk containing 55-page book about techniques for structured programming, plus demo programs. Send disk, mailer, and stamps to Dennis Baer, 25 Miller Rd., Farmingdale, NY 11735, (516) 694-5872.

WANTED: Nonprofit antiabortion group needs computer equipment and peripherals for national office. The Pro-Life Brotherhood, 350 South Orchard Dr., Park Forest, IL 60466, (312) 747-0348.

NEEDED: Information about Systems Engineering Enterprise (SEE) Corp., their users, technicians, or employees. My SEE 6684 System lost IPL PROM information. Last address was in Rockville, MD; telephone disconnected. Miguel Martinez, Puerto Rico 419B, León, Guanajuato, Mexico 37360.

WANTED: Implementation of Kevin Weiler's Hidden Surface algorithm ("Hidden Surface Removal Using Polygon Area Sorting," *SIGGRAPH*, August 1977). Ernie Pyle, Apt. I, Building 38, 2147 Linton Blvd., Delray Beach, FL 33445, (305) 272-1744 or 998-1259.

WANTED: College student requests any information on catastrophe theory and/or fractals and their implementation on a computer. Chris Mathews, 416 Redondo N, Litchfield Park, AZ 85340.

NEEDED: Information on programs involving concept of "Music of the Spheres." Has anyone composed music using sound analogs of planetary orbits, etc., as themes? Musicological research paper in progress needs references. Tom Shinnick, Apt. 3, 1905 Brunson, Houston, TX 77030.

FOR SALE: IMSAI—original, unassembled, mint condition. J. J. Haugh, 3970 North Oakland Ave., Milwaukee, WI 53211, (414) 962-5022, 9 a.m.–5 p.m.

FOR SALE: C. Itoh F10-40 printer: $899; Qume QVT102: $438; Morrow MP100 printer: $308; TI 855 with tractor: $698; Morrow MDT60 video terminal: $278; Morrow MD2 (new): $798; Liberty 100: $318. All near new, original packing. G. S. Schacter, POB 1002, South Gate, CA 90280, (213) 567-8758.

FOR SALE: Intel 8087 for IBM ceramic chips: $175. Steve Rank, 1260 Monument Blvd., Concord, CA 94518.

FOR SALE: SD Systems S-100 board set, including SBC 200 Z80 CPU/IO, Versafloppy II 5- and 8-inch controller, ExpandoRAM II 64K memory fully populated, all manuals: $500 or best offer. Isaac Davidian, 2329 East Ashlan, Fresno, CA 93726, (209) 227-2005 or 224-9212.

FOR SALE: S-100 boards, CompuPro CPU 8085/8088: $200; CompuPro *CPU Z80*: *$150*; Vector Bitstreamer 3 serial 2 parallel I/O: $75; two 32K dual-memory boards: $75. Bob Lankford, 4117 Spruce Hills Dr., Cedar Falls, IA 50613, (319) 277-2424.

WANTED: Information or instructions on building a heat laser. I pay all postage and handling. Tom Chrisman, Rt 3, Box 194, Hamburg, AR 71646.

NEEDED: Correspondence with Victor 9000 users, groups, clubs, or newsletters. John Howard, POB 712, North Haven, CT 06473.

WANTED: Other HX-20 owners to form a U.S.-based club. James Stensrud, 26 East Superior St., Duluth, MN 55802.

FOR SALE: Two 8-inch Qume disk drives in Vista cabinet, DS/DD, hardly used. Includes manual, Scotch disks, head-cleaning kit, two cables: $700. Ellis King, 6520 Selma #209, Los Angeles, CA 90028, (213) 467-3000, or Dick Myers, (213) 652-4071, 8–9 a.m.

NEEDED: Epson QX-10 people interested in sharing information and resolving application problems. Patric Lee Howley, 454 Barcelona Dr., Satsuma, AL 36572.

FOR SALE: Z-100 computer, two drives, 192K plus color video RAM, 8-MHz, etc: $2195. Also twin Siemens 8-inch drives with power and enclosure: $200 (need adjustment). George Tucker, 11615 Mississippi, Los Angeles, CA 90025, (213) 473-7691.

FOR SALE: Hewlett-Packard equipment: IDS 560G 200-cps, wide-forms printer: $750; 9130A disk drive (for 86A): $450. HP41C calculator with statistics, time, HPIL interface, and quad memory modules: $285; 82161 HPIL tape drive: $285; both for $580. Randy Webb, 622 East 11th St., Bloomington, IN 47401, (812) 335-1858 or 339-7661.

NEEDED: Dr. *Dobb's Journal* issues 57, 58, 59, 62, 63, and 64; any reasonable price paid. Also I have spare copies of issues 48, 49, 51, 53, and 55. David Millne, c/o NVR, Front St. W, Bedlington, Northumberland, NE22 5UB, England.

FOR TRADE: Our small public-domain users group for Apple II and TRS-80 Model III disk systems is expanding its software database. Send your public-domain software list or disk(s) and we'll return them. Arthur Hamlyn, Twillingate, Newfoundland A0G 4M0, Canada.

FOR SALE: Sabtronics LCD digital multimeter (bench type): $85. Sabtronics functional generator (bench type): $85. Heathkit 10-4235 35-MHz, dual-trace, delayed-sweep oscilloscope: $685. All like new. Tom Lee, Apt. 240, 100 North Whisman St., Mountain View, CA 94043, (408) 946-3000 or (415) 969-5734.

FOR SALE: BYTE volume 2, numbers 5, 11, 12; volume 3, numbers 1, 2, 3, 4, 5, 6. Like-new condition: $5 each or $37.50 for all. *Kilobaud* numbers 1–22, like-new condition: $90. Numbers 14, 15, 16, 17, like-new condition: $5 each or $17.50 for set. J. C. Arquette, 218-B Marshall St., Princeton, NJ 08540, (609) 924-8919.

FOR SALE: Radio Shack Model 100, 32K (factory installed), case, AC adapter, GE Computer Data Recorder, modem-phone and parallel-printer (Centronics-type) cables: $1395 value for $899. First certified check takes it. M. Neidich, 18 Hillside Lane, Syosset, NY 11791, (516) 921-3603 for UPS collect shipment.

FOR SALE: Quay 520 desktop computer. Includes 64K RAM, parallel-printer port, RS-232C serial port; asynchronous communications software, owner-written: $900 plus shipping. Bill Connor, 6 Schooner's Cove, East Setauket, NY 11733, (516) 231-0333.

WANTED: Tomy Tutor–compatible cassette recorder; will pay up to $150 for new, or patch cord for regular recorder and information on start-up. Bruce Turner, 353 Wisteria, Las Vegas, NV 89107.

WANTED: Contact with HP 85/86/87 users for club. Andre Lechat, case postale 3, CH-1510 Moudon, Switzerland.

NEEDED: Any information on a Measurement Systems and Controls Inc. 64K dynamic RAM board, Model DMB-6400, Rev. B. Hal Arthurs, Bloomfield Station, Prince Edward Island C0B 1E0, Canada, (902) 882-2746.

WANTED: BYTE August 1980 for articles on FORTH. Charlie Hottel, 5900 Kentucky Ave., Forestville, MD 20747, (301) 735-7495.

UNCLASSIFIED ADS MUST *be noncommercial, from readers who have computer equipment to buy, sell, or trade on a one-time basis. All requests for donated computer equipment must be from nonprofit organizations. Programs to be exchanged must be written by the individual or be in the public domain. Ads must be typed double-spaced, contain 50 words or less, and include full name and address. This is a free service; ads are printed as space permits.* BYTE *reserves the right to reject any unclassified ad that does not meet these criteria. When you submit your ad* (BYTE, *Unclassified Ads,* POB 372, *Hancock,* NH 03449), *allow at least four months for it to appear.*

WANTED: SYM-1, KIM-1, and accessories. Send specifics, SASE, and price. Brian Jacoby, RR 1, Box 157, Vesta, MN 56292.

FOR SALE: Two IBM SS/DD 5¼-inch disk drives, perfect condiditon: $100 each, both for $150, or best offer. A. Neil Hermanson, 2039 Parkdale, Kingwood, TX 77339, (713) 358-9153 after 6 p.m.

FOR SALE: Sony Typecorder with serial communications module and microcassette storage unit: $500. Also, Olivetti model 231 word processor with wafer-tape storage unit and many spin-wheel type elements: $1500. Lee D. Miller, 932 North Lakeshore Dr., Lincoln, NE 68528 (402) 435-3864.

FOR SALE: 8-slot S-100 bus system, includes Z80 B, serial and parallel, 64K; Qume DS/DD 8-inch floppy, Ampex 20-megabyte hard disk with Monitor Dynamics controller card, TeleVideo 925 terminal, Daisywriter printer, and more: $4500 for all, negotiable. Kirk Turner, 22054 DeBerry, Grand Terrace, CA 92324, (714) 783-0636.

WANTED: Omron 12SR, Pickett N4ES, Corvus 500. State condition and price in letter. William B. Adams, POB 1467, Springfield, VA 22151.

FOR SALE: IBM-compatible with 8088 and Z80 processors; runs PC-DOS, MS-DOS, CP/M-86, CP/M-80; two disk drives; 128K memory; serial port; parallel port, portable with 9-inch green monitor; RGB and composite color outputs: $1500. Cory Barker, 1715 East 1750 N, Layton, UT 84041, (801) 546-2084.

FOR SALE: Onyx C8002 computer with 40-megabyte hard disk, 512K main memory, and peripherals. Wallace Landholm, 320 Superior Ave. #350, Newport Beach, CA 92663, (714) 631-4780.

NEEDED: Computer-controlled auto-dial unit that uses a serial RS-232C port. Have Bell 212AR 300/1200-bps modem. Would like circuit diagram and parts list for building, or company address. $50 or less. Tom Brown, 65 Hillside Ave., Berkeley Heights, NJ 07922.

NEEDED: Correspondence with other HP 75 users who want to exchange ideas. Letters received will be copied or digested and sent to others who write, but this is not a newsletter per se. Particularly interested in business and financial applications. Patrick Cully, 77 Labau Ave., Staten Island, NY 10301.

WANTED: I need information on starting a BBS. Any help appreciated: tips, public-domain or user-written software for the Apple II, articles, etc. Will pay postage and expenses. Paul Allen, POB 29874, 65th Infantry Station, San Juan, Puerto Rico 00929.

WANTED: Will buy used Digicomp DR70, Astrion System 30, and/or Epson QX-10, Kaypro 4, or Apple IIc. Also system with dot-matrix and letter-quality printer. Need a user group on the central Oregon coast and astrological software sources. J. Robindottir, Venus, POB 2435, Lincoln City, OR 97367, (503) 996-3665.

FOR SALE: Quantel Color Frame Grabber: system includes NTSC decoder and encoder, 16-bit CPU, two 8-inch floppy-disk drives, documentation, source code, bit pad, terminal, and 19-inch Tektronix 670 color monitor. Dave Sieg, 7232 Leota Lane, Canoga Park, CA 91304, (818) 883-4853.

FOR SALE: Two S-100 boards, 16K dynamic RAM, 32K static RAM, video interface, three parallel and serial ports, 2K PROM, and music boards. Jim Heires, 5104 South 79th Ave., Ralston, NE 68127, (402) 331-6749 or 345-8400.

FOR SALE: Texas Instruments Professional computer, desktop model. Almost new. 13-inch hi-res color monitor; 3-plane (8-color) graphics card; 256K; two disk drives; documentation and instructions. $2900 or best offer. Elizabeth Peterson, 240 North Oak St., Janesville, IA 50647, (319) 987-2286.

FOR SALE: Two IBM 5¼-inch 160K disk drives in original cartons. Excellent condition, practically new. Were $578, asking $260 or $140 each. With documentation. E. V. Allegretti, RD 3, Lois Lane, Katonah, NY 10536, (914) 232-4470.

FOR SALE: Assorted S-100 boards: SD Systems ExpandoRAM II 64K: $175; Jade Big Z Z80 CPU: $50; Z80B CPU: $175; SSM VB3A 80-character by 50-line video board and 160 by 200 matrix graphics: $350; CCS 2422 floppy-disk controller: $250. Dale Barrett, 16544 San Jacinto Ave., Fontana, CA 92335, (714) 822-2511.

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Readers voted most favorably for "Understanding Linear Power Supplies," Steve Ciarcia's Circuit Cellar project appearing in January. In second place is the second part of the interview with Steve Wozniak: "The Apple Story: More History and the Apple III," conducted by BYTE senior technical editor Gregg Williams and Rob Moore. Rob wins $100. Jerry Pournelle's whirlwind tour in "The Fast Lane" of Computing at Chaos Manor wound up winning third place. "A Glimpse into Future Television" placed fourth in the survey; Joseph Nadan earns $50. And fifth mention goes to an article written about a tool for thinking: "The Visual Mind and the Macintosh" by Bill Benzon.

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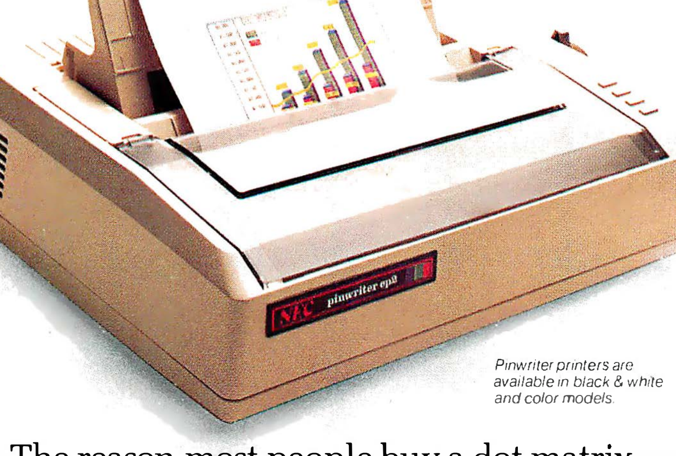
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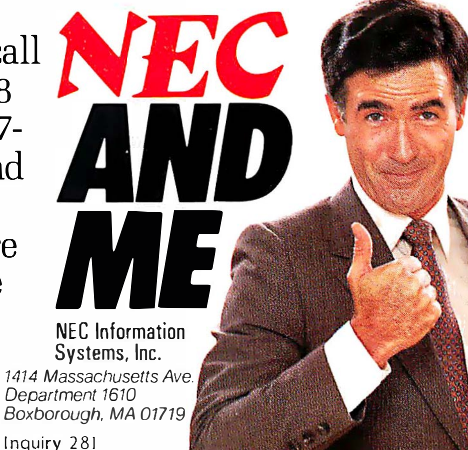
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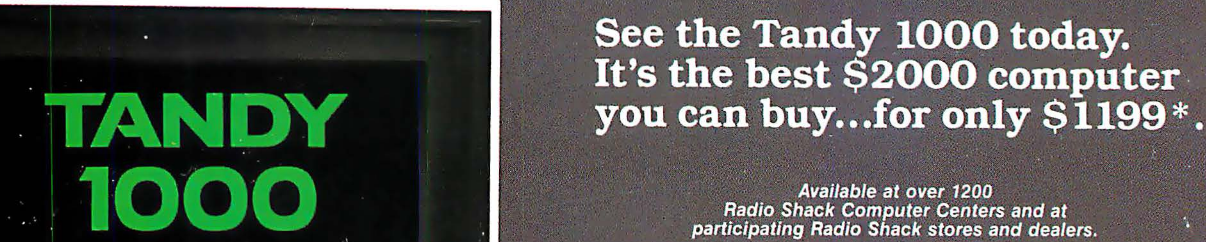
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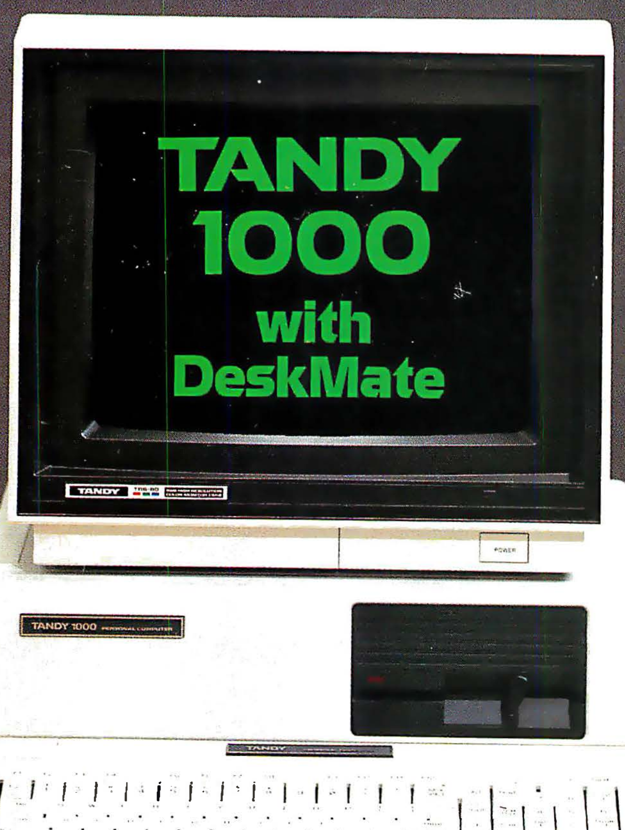
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